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Comparative Analysis of Different levels in Multilevel PUC Topology for PV Applications

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Abstract: **Multilevel inverters have created a new interest in the world of research and industry. This concept is used to achieve medium voltage and high power control applications. This paper presents the most advanced multilevel converter topology compared to all the existing concepts which is called packed u cells (PUC).The main concentration of this topology is to reduce the circuit complexity and cost with respective to high conversion quality by reducing the device count and low switching disturbances. In the point of Total Harmonic Distortion (THD) the analysis of transformer-less seven, fifteen, thirty-one levels are performed in this paper. The Simulation is to be carried out by using MATLAB/Simulink software in R2009b.**

Keywords— Multilevel Inverter, Packed U Cell (PUC), Harmonic Analysis (THD)

I. INTRODUCTION

Multilevel Converters (MLC) are prominently increasing the demand in industry because of their effective applications in medium voltage and high power operations. MLC are placed an vital part due to their low harmonic content in output. By varying the switching states of MLC it produces various output voltage levels. In multilevel concept as increasing the voltage levels the THD % in output waveform reduces. Existing concepts of multilevel topologies are following: neutral point-clamped topology (NPC) proposed by Nabae *et al.* [1]; flying capacitor topology (FC) proposed by Meynard *et al.* [2]; and classic cascaded H-bridges proposed by Peng *et al.* [3], in these topologies many draw backs are occurring if voltage levels are increased. Generally multilevel comprises of number of switches, capacitors and DC voltage sources by increasing the voltage level the device count also increased, results in more cost and it is difficult in implementation.

So researchers are focused in developing the new concepts in multilevel converters with more merits in all aspects. In existing concepts, such as Cascaded H-bridge topology had more dc voltage sources it may result in the more no of transformers [4]-[8]. So in view of all these, a transformer less converter configuration is designed, in this paper which is called Packed U Cell (PUC) [9]; topology. It achieves high power conversion quality by reducing the device count and low switching disturbances with respective to decreased in cost, circuit complexity at higher voltage levels there by avoids in bulky installations compared to existing topologies.

II. OPERATION OF PACKED U CELL TOPOLOGY

It contains of packed u cells (PUC). Each U cell has an arrangement of two switches and one capacitor. It offers high-energy conversion quality using a small number of capacitors and power devices, and consequently they have low production cost. It is very simple in terms of construction and interconnection of components. In this topology number of levels can be identified by using the following equation:

$$2^{n+1}-1 = \text{Number of levels} \quad (1)$$

where n=1,2,3…

No of capacitors can be identified by using the following equation:

$$N = 2^{Nc+1}-1 \quad (2)$$

where N is the no of voltage levels, Nc is the number of capacitors. In the same way the number of voltage levels N with respective to the number of switches Nsw is given by following equation:

$$N = 2^{\frac{Nsw}{2}}-1 \quad (3)$$

In fact, that above equations shows the advantages of this topology not only utilizing single DC source but also the

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reduced number of power switches used to generate the desired voltage levels.

III. SEVEN LEVEL PUC OPERATAION

The output voltage levels are recorded in Table.1. It should be described [10] that Sd, Se and Sf are working in complementary of Sa, Sb and Sc. So each brace of (Sa, Sd), (Sb, Se) and (Sc, Sf) cannot conduct at the same time. The switching voltage sequence can be given in Table 2. From the table the voltages are as V1, V1-V2, V2, 0, -V2, V2-V1, -V1 and the voltage values are 150 and 50. Here IGBT switches are used because it is a sort of transistor which works with a greater amount of power transfer and contains a higher switching speed with high efficient. 6 IGBT switches are utilized in 7level PUC topology and it can be divided into 2 legs, hence three switches from one leg which is as show in Fig.1.

Table I
Possible switching combinations of 7-level inverter

State	Sa	Sb	Sc	Voltage
1	On	Off	Off	V1
2	On	Off	On	V1-V2
3	On	On	Off	V2
4	On	On	On	0
5	Off	Off	Off	0
6	Off	Off	On	-V2
7	Off	On	Off	V2-V1
8	Off	On	On	-V1

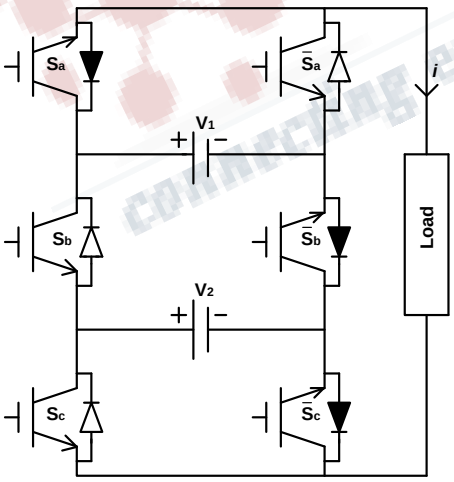

Fig.1. Seven level converter

Table.2 give the comparison for seven levels of Neutral Point Converter topology (NPC), Flying Capacitor (FC), Cascaded H-bridge (CHB), and Hybrid Cascaded H-bridge towards PUC topology.

Table II
Comparison of 7 levels PUC topology with existing topologies

	NPC	FC	CHB	HCHB	PUC
Capacitor	6	6	3	2	2
Diodes	10	0	0	0	0
Switches	12	12	12	8	6

Fifteen Level PUC Operation

Table.3 shows the switching sequence of the fifteen level operation operated in case of $\frac{V1}{V2}=\frac{3}{7}$ and $\frac{V2}{V3}=3$ and design [11] is shown in Fig.2. Switches S_a and $\overline{S}_a$ are operated as complimentary, but only S_a switch is considered in table. Here we have taken the values as V1=420V, V2=180V and V3=60V. Schematic diagram shown in Fig.2.

Table III
Possible switching combinations of 15-level inverter

States	Sa	Sb	Sc	Sd	Voltage
1	On	Off	Off	Off	V1
2	On	Off	On	Off	V1-V2+V3
3	On	Off	Off	On	V1-V3
4	On	Off	On	On	V1-V2
5	On	On	Off	Off	V2
6	On	On	Off	On	V2-V3
7	On	On	On	Off	V3
8	On	On	On	On	0
9	Off	Off	Off	On	-V3
10	Off	Off	On	Off	V3-V2
11	Off	Off	On	On	-V2
12	Off	On	Off	Off	V2-V1
13	Off	On	On	Off	V3-V1
14	Off	On	Off	On	V2-V1-V3
15	Off	On	On	On	-V1

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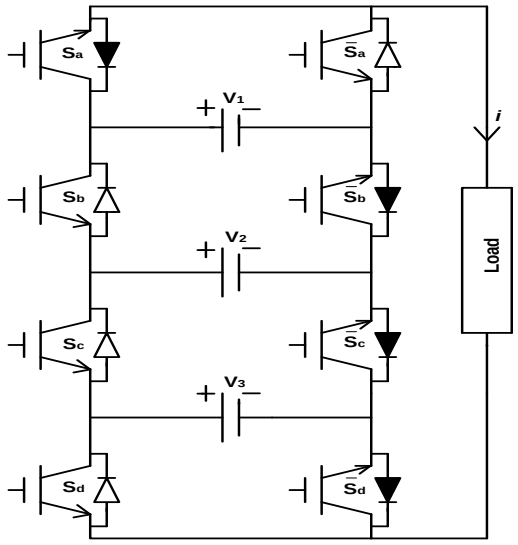

Fig.2. Fifteen level converter

Table.4 gives the comparison for fifteen levels of Neutral Point Converter topology (NPC), Flying Capacitor (FC), Cascaded H-bridge (CHB), and Hybrid Cascaded H-bridge towards PUC topology.

Table IV
Comparison of 15 levels PUC topology with existing topologies

	NPC	FC	CHB	HCHB	PUC
Capacitor	14	14	7	3	3
Diodes	26	0	0	0	0
Switches	28	28	28	12	8

Thirty-One Level PUC Operation

The switching Table.3 shows the analysis of switching operation for thirty-one level and Fig.3 shows the topology of 31 level inverter [12]. The pure sinusoidal waveform can be obtained by increasing the voltage levels hence the input voltages are

$$V1 = Vdc, V2 = Vdc\frac{7}{15}, V3 = Vdc\frac{3}{15}, V4 = Vdc\frac{1}{15}$$

Table V
Possible switching combinations of 31-level inverter

State	Sa	Sb	Sc	Sd	Se	Voltage
30	On	Off	Off	Off	Off	V1
29	On	Off	Off	On	Off	V1-V4
28	On	Off	Off	Off	On	V1-V3+V4
27	On	Off	Off	On	On	V1-V3
26	On	Off	On	Off	Off	V1-V2+V3
25	On	Off	On	On	Off	V1-V2+V3+V4
24	On	Off	On	Off	On	V1-V2+V4
23	On	Off	On	On	On	V1-V2
22	On	On	Off	Off	Off	V2
21	On	On	Off	On	Off	V2-V4
20	On	On	Off	Off	On	V2-V3+V4
19	On	On	Off	On	On	V2-V3
18	On	On	On	Off	Off	V3
17	On	On	On	On	Off	V3-V4
16	On	On	On	Off	On	V4
15	On	On	On	On	On	0
14	Off	Off	Off	On	Off	-V4
13	Off	Off	Off	Off	On	-V3+V4
12	Off	Off	Off	On	On	-V3
11	Off	Off	On	Off	Off	-V2+V3
10	Off	Off	On	On	Off	-V2+V3-V4
9	Off	Off	On	Off	On	-V2+V4
8	Off	Off	On	On	On	-V2
7	Off	On	Off	Off	Off	-V1+V2
6	Off	On	Off	On	Off	-V1+V2-V4
5	Off	On	Off	Off	On	-V1+V2-V3+V4
4	Off	On	Off	On	On	-V1+V2-V3
3	Off	On	On	Off	Off	-V1+V3
2	Off	On	On	On	Off	-V1+V3-V4
1	Off	On	On	Off	On	-V1+V4
0	Off	On	On	On	On	-V1

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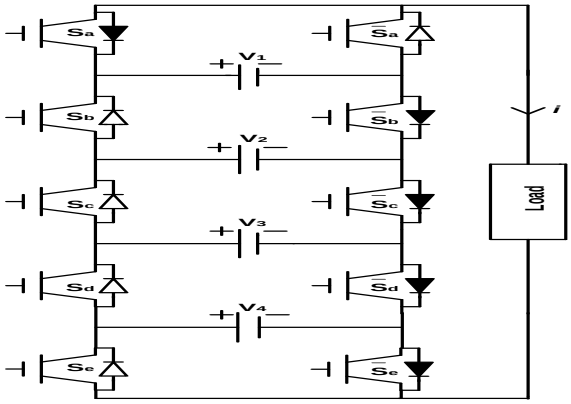

Fig.3. Thirty-one level converter

Table 6 give the comparison for thirty-one levels of Neutral Point Converter topology (NPC), Flying Capacitor (FC), Cascaded H-bridge (CHB), and Hybrid Cascaded H-bridge towards PUC topology.

Table VI
Comparison of 15 levels PUC topology with existing topologies

	NPC	FC	CHB	HCHB	PUC
Capacitor	30	30	15	4	4
Diodes	58	0	0	0	0
Switches	60	60	60	16	10

IV. SIMULATION ANALYSIS

A comparative analysis is done for seven, fifteen, and thirty-one level of PUC (packed u cell) converter to show the clear performance of Harmonic Analysis (THD),so from this analysis it is clear that by increasing the levels THD% value minimizes which is shown in Table 7.

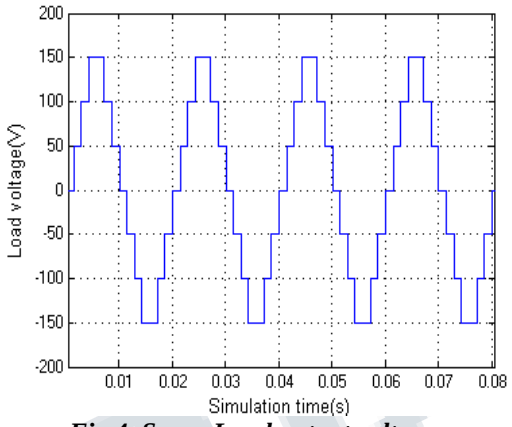

Fig.4. Seven Level output voltage

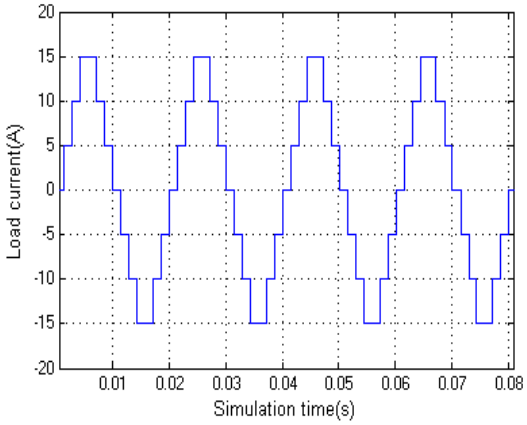

Fig.5. Seven Level output current

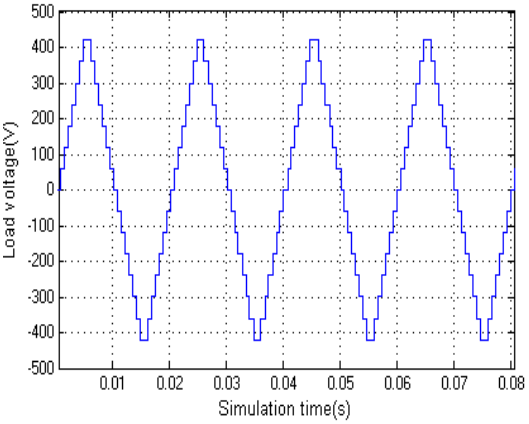

Fig.6. Fifteen Level output voltage

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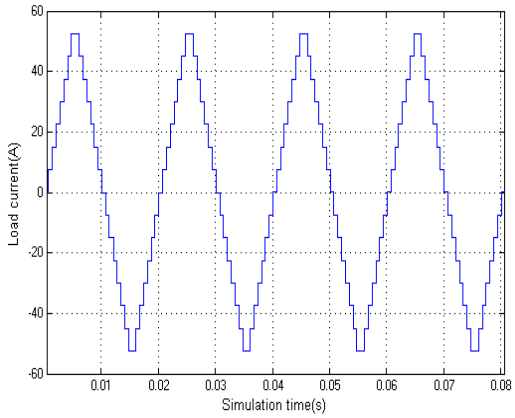

Fig.7. Fifteen Level output current

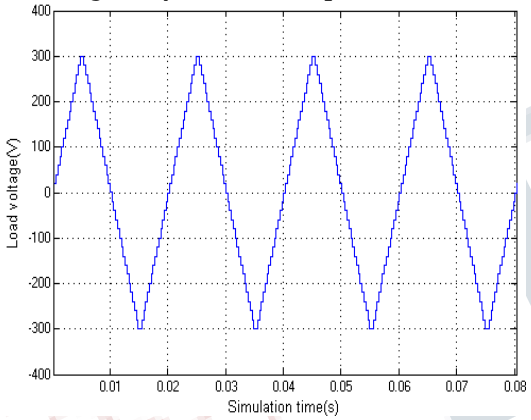

Fig.8. Thirty-one Level output voltage

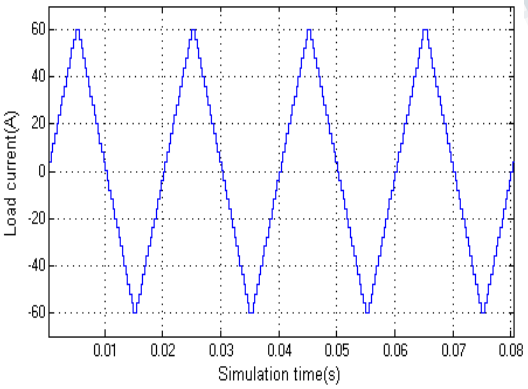

Fig.8. Thirty-one Level output current

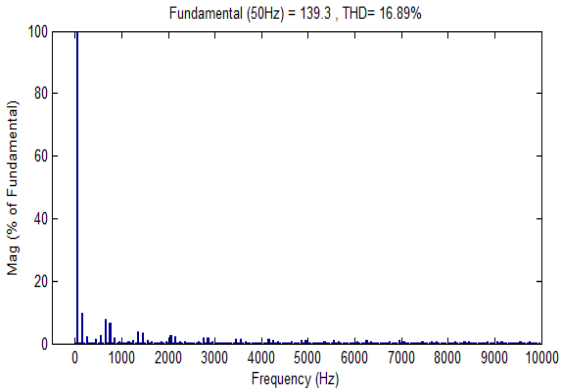

Fig.9. THD of Seven Level output voltage

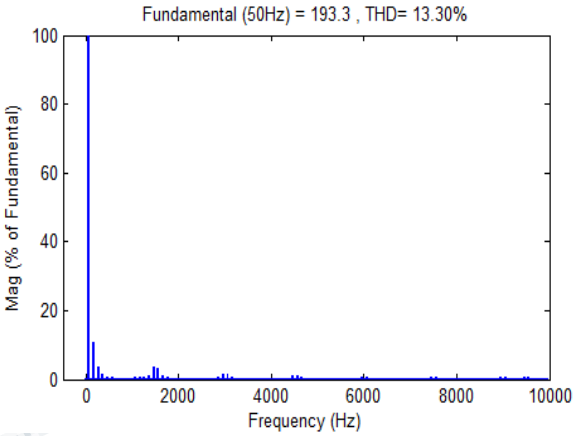

Fig.10. THD of Fifteen Level output voltage

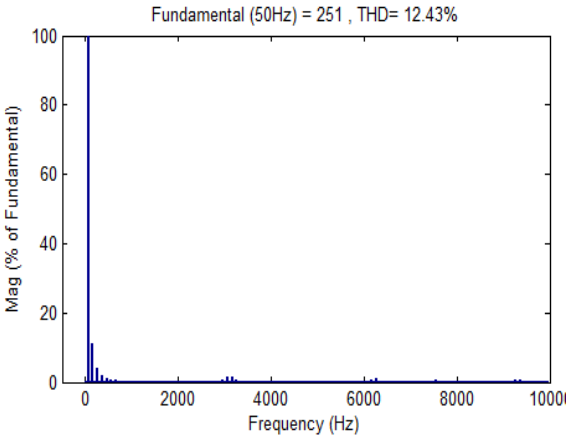

Fig.11. THD of Thirty-one Level output voltage

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Table VII
Results Analysis

Levels	THD%
7-level	16.89
15-level	13.30
31-level	12.43

V. CONCLUSION

This paper demonstrates the comparative study on THD of output voltage waveform of seven-level, fifteen-level and thirty one-level of PUC multi-level inverter has shown in this paper. In the exiting topologies by increasing the levels simultaneously device count also increases but in this PUC converter device count is very less compared to existing ones hence in the same time the harmonics also reduced. Simulation results show the performance of this converter at various levels.

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