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Fuzzy Based Current Source Modular Multilevel Converter and Application as Statcom

[1] Devender Reddy Konathala, [2] Goparaju Kranthi Kumar, [3] Srikanth.S
[1][3] Assistant professor, Dept. of EEE, Institute of Aeronautical engineering college, Dundigal, India
[2] Assistant professor, Dept. of EEE, Chaitanya Institute of Technology and sciences, India

Abstract: **- In this paper a Multilevel current source converters is utilized for the high power applications with high current low and voltage requirements. Therefore we can totally analysis of a current source modular multilevel converter (CSMMC) with its application such as STATCOM. There are different properties of CSMMC which are correlated with the voltage source modular multilevel converter (VSMMC). There are two method for inductor current balancing they are sub module inductance selection method and a sorting based algorithm which are proposed for CSMMC. Moreover for the switching technique we are implementing the carrier phase shifted sinusoidal pulse width modulation. Here the performance of a converter can be analyzed under non-interleaved and interleaved carrier signals during the upper and lower arms. Here we are using the fuzzy controller compared to other controllers i.e. The fuzzy controller is the most suitable for the human decision-making mechanism, providing the operation of an electronic system with decisions of experts. Simulation Results will show that CSMMCs which is corresponding VSMMCs have analogous features. Hence, for the reference of CSMMCs and vice versa we are using the developed VSMMCs. Furthermore, the control satergy for CSMMC which is depend upon the STATCOM are presented and also proven by using simulations. The proposed STATCOM will display that the transient and steady state performance of the system are satisfactory.**

***Index Terms*—Current balancing, current source modular multilevel converter (CSMMC), Fuzzy logic controller, HVDC transmission, STATCOM**

I. INTRODUCTION

The main objective of this paper is to analyzed in detail the operation of a CSMMC, a dual of VSMMC, and to investigate its feasibility as a STATCOM. In CSMMC, a variable current source in each converter arm is created using parallel connected inductor SMs. Voltage source modular multilevel converters are used for high power applications. Main features of the VSMMCs include reduced harmonics, lower switching frequency, and reduced stress on each device, amongst others [1]. Moreover, because of modular structure, scalability to various power and voltage levels is easily achieved and reliability can be improved by including redundant sub modules in each phase [2]. These features make the VSMMCs more attractive and competitive for HVDC and FACTS applications [3]. The CSCs using fully controllable switches have many advantages than LCCs. The main features of CSCs using self-commutating devices are: 1) independent control of the active and reactive power, 2) it can be operated in weak grids or with passive loads, and 3) relatively small footprint because the ac side filters can be eliminated due to low harmonic distortion [10].

An MMC topology using a modified current source H-bridge cell is proposed, to address the voltage scaling problem. In this paper, detail theoretical analysis of CSMMC is presented and various parameters of the converter are correlated with VSMMC. SM inductance selection method and SM inductor current balancing strategy are presented for CSMMC. Furthermore, equations are developed in dq frame to design a controller for CSMMC based STATCOM. Dynamic performances of the STATCOM during step change in capacitive mode to inductive mode and vice versa, and during ac and dc faults are evaluated.

CSMMC STRUCTURE AND OPERATION

Fig. 1 shows one phase of a three phase CSMMC. Each phase of a converter consists of two arms and each arm consists of N parallel connected half bridge SMs and the arm capacitor. The inductors of the SMs act as current sources that can be inserted or bypassed in each arm of the CSMMC. This way the ac output current can be controlled by varying the number of inserted SMs in the upper and lower arms by using appropriate modulation technique

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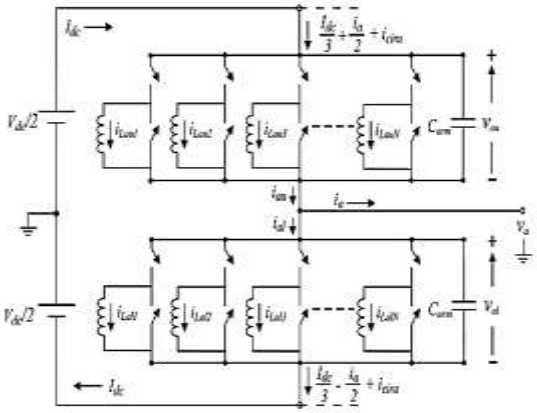
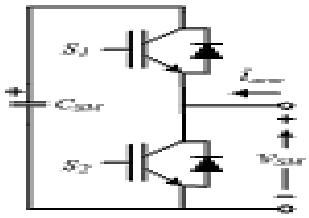


Fig. 1. Configuration of phase-a of a three phase CSMMC.

Fig. 1 shows one phase of a three phase CSMMC. Each phase of a converter consists of two arms and each arm consists of N parallel connected half bridge SMs and the arm capacitor. The inductors of the SMs act as current sources that can be inserted or bypassed in each arm of the CSMMC. This way the ac output current can be controlled by varying the number of inserted SMs in the upper and lower arms. The arm capacitor, Carm, is dual to the arm inductance of a VSMMC.

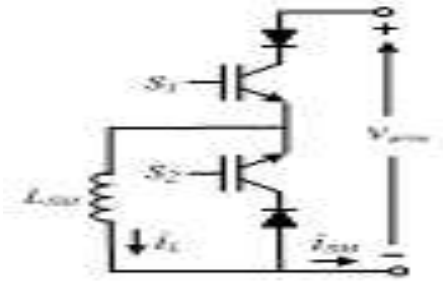
SM Structure and Operation

A half bridge SM of a VSMMC is shown in Fig. 2(a). This is the basic building block of a VSMMC which consists of two bidirectional switches and a capacitor.



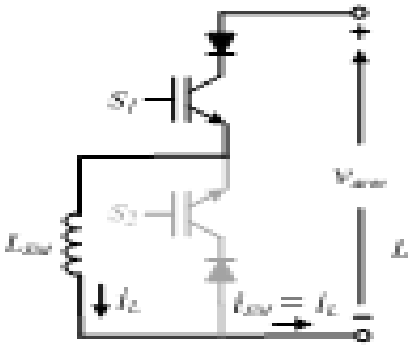
(a)

The corresponding dual, a half bridge inductor SM for a CSMMC is shown in Fig. 2(b).



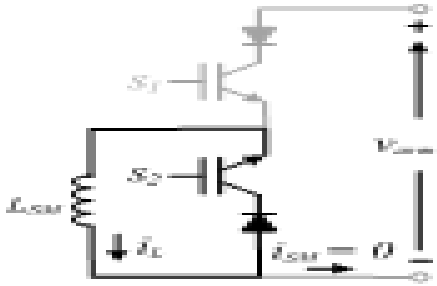
(b)

The controlled bidirectional switches and a capacitor are replaced with controlled reverse voltage blocking switches and an inductor respectively. In Fig. 2(b), two switches S1 and S2 are complimentary and their switching states are decided by using appropriate modulation technique to get the desired output current from the SM.



(c)

In Fig. 2(c), S1 is ON (S2 is OFF), hence, the SM is inserted in the arm and the output current of the SM is effectively the inductor current.

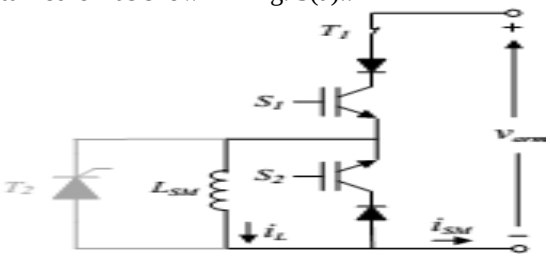


(d)

Fig. 2. (a) Half bridge capacitor SM (b) Half bridge inductor SM (c) SM inserted (d) SM bypassed.

In Fig. 2(d), S1 is OFF (S2 is ON), hence, the SM is bypassed and the output current of the SM is zero. Nevertheless, the inductor current remains continuous through switch S2. Hence the output current of the converter can be controlled by inserting or bypassing the SMs connected in parallel.

In normal operation, switch T1 is closed and thyristor T2 is turned-off as shown in Fig. 3(a)..



(a)

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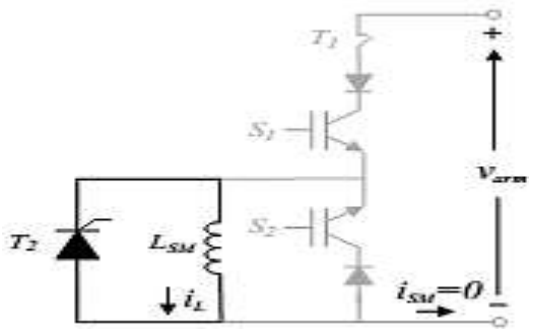

(b)

Fig. 3. Submodule open-circuit protection using thyristor (a) normal operation (b) operation during fault.

When the fault is detected in the SM, thyristor T2 is turned-on and switch T1 is opened to bypass the faulty SM from the system as shown in Fig. 3(b). The SM inductor current remains continuous through thyristor T2 and thus protects the SM from possible damage. Simultaneously, if the redundant SM is available then the switch T1 of a redundant SM is closed to replace the faulty SM with a redundant SM. Hence, continuous operation of the CSMMC is ensured with increased safety and availability.

Assumptions

In order to simplify the mathematical analysis, some assumptions are made. These assumptions are as follows:

1) Only fundamental frequency component in the ac output waveforms is considered. This is a reasonable assumption because the number of levels in the output or the switching frequency is generally high.

2) It is assumed that the SM inductor currents are balanced at all times to ensure stable operation of the CSMMC.

3) For circulating current analysis, only 2nd harmonic component is considered. Aside from the 2nd harmonic component, there may be other harmonics in the circulating current.

4) For simplicity, balanced grid voltages have been assumed and hence only positive sequence components of the three phase voltages and currents are considered.

Analysis and Operation of CSMMC

To analyze the operation of a converter, phase-a of a three phase CSMMC, shown in Fig. 1, is considered. If the upper switch in an SM is ON, the output of the SM is equal to the corresponding inductor current; otherwise, it is zero. The ac output current ia and phase voltage va are defined as

$$i_a = \hat{I}_a \sin \omega_0 t, \qquad v_a = \hat{V}_a \sin(\omega_0 t + \emptyset) \quad (1)$$

Here, ˆIa and ˆ Va are the peak values of the output current and voltage respectively, ω0 is the fundamental frequency and ϕ is the load phase angle. The effective inductances of upper and lower arms of phase-a, are given by

$$L_{au} = {}^{L_{SM}}/_{N_{au}}, \qquad L_{al} = {}^{L_{SM}}/_{N_{al}} \quad (2)$$

Here, Nau and Nal are the number of SMs inserted in upper and lower arms respectively and LSM is the SM inductance. Using KCL, the total output currents of upper and lower arm SMs of phase-a in Fig. 1 can be expressed by

$$i_{Lau} = \sum_{j=1}^{N_{au}} i_{Lauj}, \qquad i_{Lau} = \sum_{j=1}^{N_{al}} i_{Lalj}, \quad (3)$$

Note that iLauj, j = 1, ..,Nau and iLalj , j = 1, ..,Nal, are the currents of inserted SMs in upper and lower arm respectively. Using (3), the upper and lower arm currents iau and ial in Fig. 1 are defined by

$$i_{au} = C_{arm} \frac{dv_{au}}{dt} + i_{Lau}, \quad i_{al} = C_{arm} \frac{dv_{al}}{dt} + i_{Lal} \quad (4)$$

where, vau and val are the upper and lower arm voltages respectively. The arm currents, iau and ial, consists of three components: 1) the dc current, Idc/3, which is responsible to keep the arm energized or to maintain the SM inductor currents around their reference value; 2) half of the ac side current; and 3) the circulating currents which circulate within the three phases of the converter. Hence, iau and ial can also be written as

$$i_{au} = \frac{I_{dc}}{3} + \frac{i_a}{2} + i_{cira}, \quad (5)$$

$$i_{al} = \frac{I_{dc}}{3} - \frac{i_a}{2} + i_{cira}, \quad (6)$$

where icira is the circulating current in phase-a. Depending upon the switching technique, the circulating current contains any number of harmonic components. Therefore, in steady state, icira can be given by the general expression

$$i_{cira} = \sum_{n=1}^{\infty} i_{ciran} \sin(n\omega_o t + \emptyset_n) \quad (7)$$

If the circulating currents, icirp, p = a, b, c, of the three phases have equal magnitude and phase difference of 2π/3, then,

$$i_{cira} + i_{cirb} + i_{circ} = 0 \quad (8)$$

.Therefore, the circulating currents have no effect outside the converter either on the ac or dc side. However, they have a significant impact on the rating of converter components and the losses of the converter. Hence, they should be kept as close to zero as possible.

The ac side current of phase-a can be obtained by subtracting (5b) from (5a), that is

$$i_a = i_{au} - i_{al} \quad (9)$$

Using KVL, the ac voltage of phase-a in Fig. 1 is defined by

$$v_a = -v_{au} + {}^{V_{dc}}/_{2} \quad (10)$$

$$v_a = v_{al} - {}^{V_{dc}}/_{2} \quad (11)$$

$$v_a = (v_{al} - v_{au})/2 \quad (12)$$

The dc link voltage is then derived from (9) and (10)

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$V_{dc} = v_{au} + v_{al}$

Using (5a) or (5b) for all the three phases, the total dc link current in terms of ipu or ipl, p = a, b, c is expressed as

$I_{dc} = i_{au} + i_{bu} + i_{cu}$ or $I_{dc} = i_{al} + i_{bl} + i_{cl}$ (13)

Substituing (4) in (8) yields

$i_a = C_{arm}\frac{d}{dt}(v_{au} - v_{al}) + i_{Lau} - i_{Lal}$ (14)

Inserting (11) in (14) gives

$i_a = -2C_{arm}\frac{dv_a}{dt} + i_{Lau} - i_{Lal}$ (15)

It is clear from (15) that iLau and iLal should be controlled to get the desired output current. To specify the reference currents iLau and iLal, the harmonic and circulating currents are ignored. Hence, using (1a) and (4)-(5), the reference currents of the upper and lower arms of phase-a in time domain are expressed as

$i_{Lau} = \frac{I_{dc}}{3} + \frac{\hat{I}_a}{2}\sin\omega_0 t = \frac{I_{dc}}{3}[1 + m_i \sin\omega_0 t]$ (16)

$i_{Lal} = \frac{I_{dc}}{3} + \frac{\hat{I}_a}{2}\sin\omega_0 t = \frac{I_{dc}}{3}[1 - m_i \sin\omega_0 t]$ (17)

where mi is the modulation index, defined by mi = 3^Ia 2Idc. Similarly, substituting (1b) in (9) and (10), the voltages in each arm of phase-a in time domain are given by

$v_{au} = \frac{V_{dc}}{2}[1 - m_v \sin(\omega_0 t + \emptyset)]$ (18)

$v_{al} = \frac{V_{dc}}{2}[1 + m_v \sin(\omega_0 t + \emptyset)]$ (19)

Where mv is defined by mv = 2 ^ Va Vdc .

The internal energy of phase-a can be calculated by summing and integrating (20) and (21), that is,

$E_a = \frac{V_{dc}I_{dc}}{6}\left[2t - m_i m_v \cos\emptyset t + \frac{m_i m_0}{2\omega_0}(\sin(2\omega_0 t + \emptyset))\right]$ (20)

In steady state, if the losses in the converter are neglected then the dc component of the energy should not appear in the arms. Otherwise the energy in the SM inductors will increase or decrease continuously. Hence,

$2t - m_i m_V \cos\emptyset t = 0$ or $m_i m_V = {}^{2}/_{\cos\emptyset}$ (21)

Substituting mimv from (23) in (22), one get the alternating energy in the converter phase

$E_a = \frac{V_{dc}I_{dc}}{6\omega_0 \cos\emptyset}\sin(2\omega_0 t + \emptyset)$ (22)

Eq. (24) shows that the energy in the converter arms fluctuates at twice the fundamental frequency. This is in line with the 2nd harmonic current in circulating current of VSMMC.

Circulating current analysis

To solve for the amplitude and phase of this 2nd harmonic circulating current, the early assumptions of the arm currents are revised and the 2nd harmonic circulating component is supposed to exist in the arm currents. That is,

$i_{au} = \frac{I_{dc}}{3} + \frac{I_a}{2}\sin\omega_0 t + \hat{I}_{2f}\sin(2\omega_0 t + \emptyset_2)$ (23)

$i_{al} = \frac{I_{dc}}{3} - \frac{I_a}{2}\sin\omega_0 t + \hat{I}_{2f}\sin(2\omega_0 t + \emptyset_2)$ (24)

Where, ˆI2f and ϕ2 denote the amplitude and phase of the 2nd harmonic circulating current. Using (18)-(19), the expressions for the revised instantaneous power delivered to the upper and lower arms of phase-a are derived as

$P'_{au} = P_{au} + \frac{\hat{I}_{2f}V_{dc}}{2}\sin(2\omega_0 t + \emptyset_2)[1 - m_v \sin(\omega_0 t + \emptyset)]$ (25)

$P'_{au} = P_{au} + \frac{\hat{I}_{2f}V_{dc}}{2}\sin(2\omega_0 t + \emptyset_2)[1 + m_C \sin(\omega_0 t + \emptyset)]$ (26)

The alternating energy in phase-a is then obtained by summing and integrating (27) and (28), and inserting (23). That is,

$E_a = \frac{V_{dc}I_{dc}}{6\omega_0 \cos\emptyset}\sin(2\omega_0 t + \emptyset) - \frac{V_{dc}\hat{I}_{2f}}{2\omega_0}\cos(2\omega_0 t + \emptyset_2)$ (27)

If the upper and lower arms of CSMMC with N SMs per arm, are controlled such that at any instant Nau + Nal = N, and the SM inductor currents are balanced, then the average SM inductor current iL is expressed as

$i_L = (i_{au} + i_{al})/N$ (28)

SM inductance selection

The stored energy EL in an inductor of each SM of CSMMC changes with time because the energy in the arm is fluctuating as shown. This results in the current ripples in SM inductors. The current ripple in SM inductors depends on the size of the SM inductor LSM and the energy power ratio E(S). Here, E(S) signifies the energy storage requirements in the converter in terms of total energy storage per transferred MVA.

The stored energy, EL, in an SM inductor is expressed as

$E_L = \frac{1}{2}L_{SM}i_L^2$ (29)

CSMMC CONTROL

In CSMMC multiple SMs are connected in parallel in each arm. Hence to get the desired output current, it is required to insert or bypass a certain number of SMs in each arm at any point of time and the current through all the SMs should be balanced.

Switching technique

In this paper, the carrier phase shifted sinusoidal pulse width modulation (CPS-SPWM) scheme is used, to synthesize a multi-level output current waveform at the ac side of the CSMMC. The SM is inserted or bypassed based on the switching state produced from the intersection of sinusoidal modulating signal and triangular carrier signal. Moreover, two options exists with CPS-SPWM: 1) non-interleaved switching; and 2) interleaved switching.

Inductor current balancing

A block diagram of the SM inductor current balancing algorithm in a CSMMC for phase-a is shown in Fig. 4.

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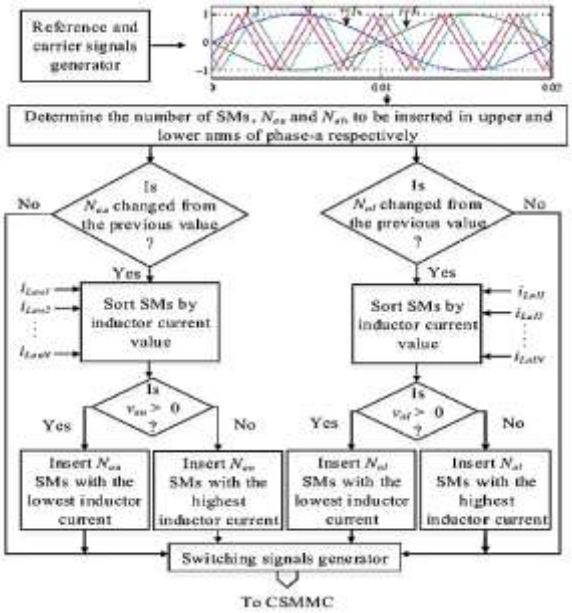

Fig. 4. Block diagram of the indicator current balancing algorithm including CPS-SPWM for phase-a of a three phase CSMMC.

The number of SMs to be inserted in upper and lower arms of phase-a are determined by the comparison of the sinusoidal modulating signals and triangular carrier signals, as shown in Fig. 4. Moreover, as can be observed in the diagram of Fig. 4, sorting is done only when the SM is to be inserted or bypassed to reduce the switching losses.

CSMMC BASED STATCOM

The circuit configuration of a CSMMC based STATCOM is shown in Fig. 5. The STATCOM is connected to the grid through a coupling transformer.

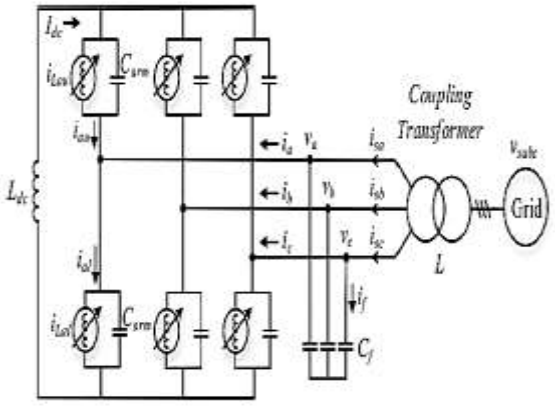

Fig. 5. Configuration of CSMMC based STATCOM

In Fig. 5, iLau and iLal represent controllable current sources, whose instantaneous value depends on the number of inserted and bypassed SMs in each arm. Cf is the capacitance of the harmonic filter. Ldc is the dc link reactor used to reduce the dc current ripple. Table I describes one of the possible switching states with non-interleaved switching for each current level in phase-a of three phase five level CSMMC.

TABLE I
ONE OF THE POSSIBLE SWITCHING STATES FOR EACH CURRENT LEVEL IN PHASE-a OF A THREE PHASE FIVE LEVEL CSMMC

SM_{au1}	SM_{au2}	SM_{au3}	SM_{au4}	i_{au}	i_{al}	i_a
1	1	1	1	$2I_{dc}/3$	0	$2I_{dc}/3$
1	1	1	0	$I_{dc}/2$	$I_{dc}/6$	$I_{dc}/3$
1	1	0	0	$I_{dc}/3$	$I_{dc}/3$	0
1	0	0	0	$I_{dc}/6$	$I_{dc}/2$	$-I_{dc}/3$
0	0	0	0	0	$2I_{dc}/3$	$-2I_{dc}/3$

Controller design

The control objectives for the system of Fig. 5 are to provide the required reactive power compensation Qref to the grid and to regulate the dc-link current Idc. The controller is implemented based on current mode control in synchronous dq frame as shown in Fig. 6. In this approach, the CSMMC line current is regulated by the inner current control loop. The reactive power and dc link current are controlled by the outer current control loop.

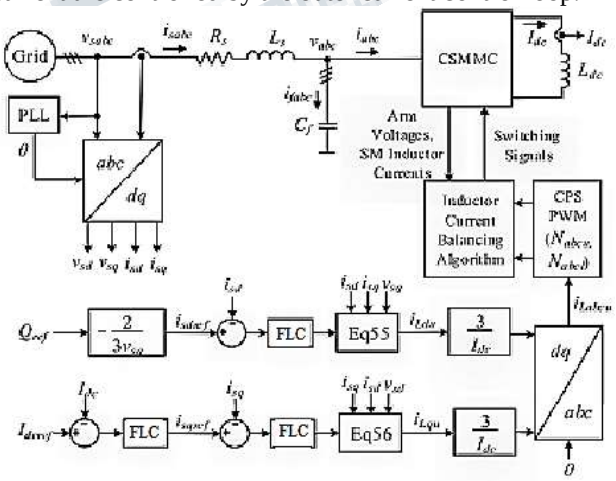

Fig. 6. Diagram of CSMMC based STATCOM control system.

The dynamic equations of phase-a in abc frame for the system of Fig. 6 are expressed as

$$i_a = 2C_{arm}\frac{dv_a}{dt} - i_{Lau} + i_{Lal}$$

$$i_{sa} = i_a + C_f\frac{dv_a}{dt}$$

$$v_{sa} = v_a + R_s i_{sa} + L_s\frac{di_{sa}}{dt} \qquad (30)$$

Ls and Rs represent the leakage inductance and resistance

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of the coupling transformer. These equations are valid for all the three phases. The upper or lower arm current is selected to be the output of the controller because the upper and lower arm currents are phase shifted by π radians. The converter line current in terms of the upper arm current is expressed as

$$i_a = 2C_{arm}\frac{dv_a}{dt} - 2i_{Lau} + \frac{2I_{dc}}{3} \quad (31)$$

Eqs. (45), (46) and (47) are transformed to the synchronous dq frame using the transformation T given by

$$T = \frac{2}{3}\begin{bmatrix} \cos(\theta) & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ \sin(\theta) & \sin\left(\theta - \frac{2\pi}{3}\right) & \sin\left(\theta + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \quad (32)$$

Here, the d-axis is aligned to the grid voltage vector such that the d-axis component of grid voltage vsd = 0. The phase locked loop (PLL) is used to detect the phase θ of the grid voltage.

FUZZY LOGIC CONTROLLER

In FLC, basic control action is determined by a set of linguistic rules. These rules are determined by the system. Since the numerical variables are converted into linguistic variables, mathematical modeling of the system is not required in FC.

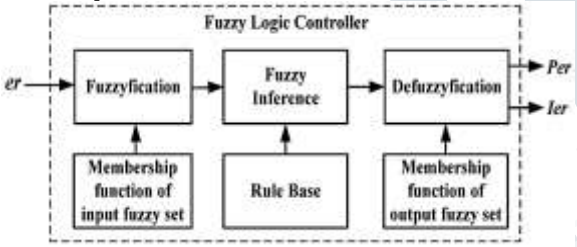

Fig.7.Fuzzy logic controller

The FLC comprises of three parts: fuzzification, interference engine and defuzzification. The FC is characterized as i. seven fuzzy sets for each input and output. ii. Triangular membership functions for simplicity. iii. Fuzzification using continuous universe of discourse. iv. Implication using Mamdani's, 'min' operator. v. Defuzzification using the height method.

TABLE III: Fuzzy Rules

e / ė	NB	NM	NS	ZE	PS	PM	PB
NB	NB	NB	NB	NB	NM	NS	ZE
NM	NB	NB	NB	NM	NS	ZE	PS
NS	NB	NB	NM	NS	ZE	PS	PM
ZE	NB	NM	NS	ZE	PS	PM	PB
PS	NM	NS	ZE	PS	PM	PB	PB
PM	NS	ZE	PS	PM	PB	PB	PB
PB	ZE	PS	PM	PB	PB	PB	PB

Fuzzification: Membership function values are assigned to the linguistic variables, using seven fuzzy subsets: NB (Negative Big), NM (Negative Medium), NS (Negative Small), ZE (Zero), PS (Positive Small), PM (Positive Medium), and PB (Positive Big). The Partition of fuzzy subsets and the shape of membership CE(k) E(k) function adapt the shape up to appropriate system. The value of input error and change in error are normalized by an input scaling factor.In this system the input scaling factor has been designed such that input values are between -1 and +1. The triangular shape of the membership function of this arrangement presumes that for any particular E(k) input there is only one dominant fuzzy subset. The input error for the FLC is given as

$$E(k) = \frac{P_{ph(k)} - P_{ph(k-1)}}{V_{ph(k)} - V_{ph(k-1)}} \quad (33)$$

$$CE(k) = E(k) - E(k\text{-}1) \quad (34)$$

Inference Method: Several composition methods such as Max–Min and Max-Dot have been proposed in the literature. In this paper Min method is used. The output membership function of each rule is given by the minimum operator and maximum operator. Table 1 shows rule base of the FLC.

Defuzzification: As a plant usually requires a non-fuzzy value of control, a defuzzification stage is needed. To compute the output of the FLC, „height" method is used and the FLC output modifies the control output. Further, the output of FLC controls the switch in the inverter. In UPQC, the active power, reactive power, terminal voltage of the line and capacitor voltage are required to be maintained. In order to control these parameters, they are sensed and compared with the reference values. To achieve this, the membership functions of FC are: error, change in error and output

The set of FC rules are derived from

$$u=-[\alpha E + (1-\alpha)*C] \quad (35)$$

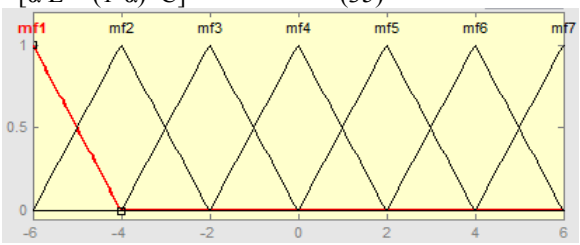

Fig 8 input error as membership functions

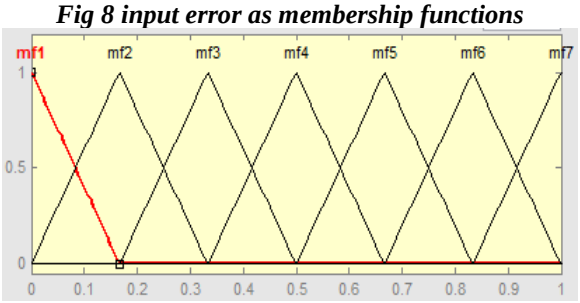

Fig 9 change as error membership functions

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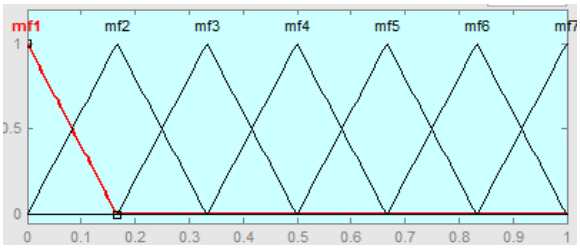

Fig.10 output variable Membership functions

SIMULATION RESULS

To demonstrate the operation of the CSMMC, the simulation of a three phase CSMMC is carried out. Moreover, to verify the operation and control of CSMMC as a STATCOM, simulation results of a grid connected CSMMC of Fig. 5 are presented.

Standalone CSMMC

Parameters of a converter used for the simulation of a standalone CSMMC are shown in Table II. The SM inductance of CSMMC is evaluated using (39) for energy power ratio E(S) = 30 kJ/MVA and the rated power S = 10 MVA. This ensures the ripple of the SM inductor current within the rage of 10%.

TABLE II
CSMMC PARAMETERS FOR SIMULATION

Grid Voltage/Frequency	$V_p = 115$ kV (line-line RMS), $f_0 = 50$ Hz
Coupling Transformer	115/11 kV, 50 MVA, $L_s = 0.16$ pu
Converter Parameters	$N = 4$, $S = 50$ MVA, $L_{SM} = 281$ mH, $C_{arm} = 15$ μF, $f_{sw} = 1$ kHz
DC-link reactor	$L_{dc} = 50$ mH
Filter Capacitance	$C_f = 75$ μF

Simulation results of phase-a of a standalone CSMMC are shown in Fig. 11. CPS-SPWM switching from interleaved to non-interleaved is done at t = 1 s. Fig. 11(a) shows the differential current and the ac side current. It can be seen that the ac side current does not have a dc component.

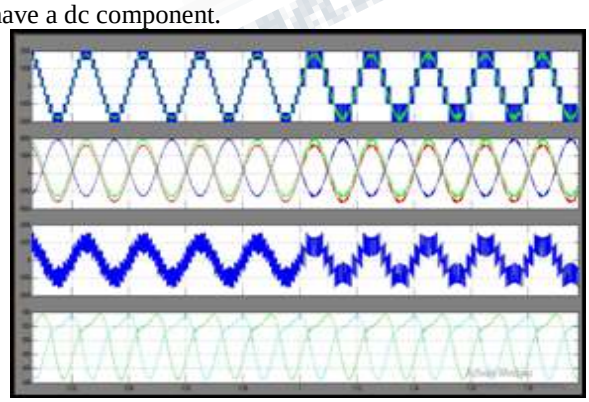

Fig. 11. Simulated waveforms of phase-a of a standalone CSMMC with interleaved switching for t < 1 s, and non-interleaved switching for t 1 s. (a) Calculated iLa and output current (b) Arm voltages and output voltage (c) Circulating current (d) Inductor currents in upper and lower arms.

Fig. 11(b) shows the arm voltages and ac side voltage which are analogous to the arm currents and ac side current in VSMMC. Fig. 11(c) shows the circulating current between the phases. Since the circulating current cannot be measured directly, it is calculated using (5). It can be observed that the 2nd harmonic component in circulating current is predominant. Fig. 11(d) also shows that the proposed inductance selection method ensures the ripple of the SM inductor current within the range of 10%.

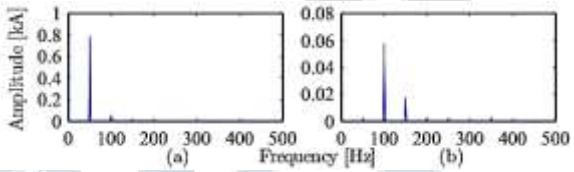

Fig. 12. Spectrum of (a) arm current and (b) circulating current.

Fig. 12 shows the spectrum of the arm current and the circulating current with non-interleaved switching. Fig. 13 shows the comparison of simulation results with the analytically calculated results of 2nd harmonic circulating current with different values of SM inductance.

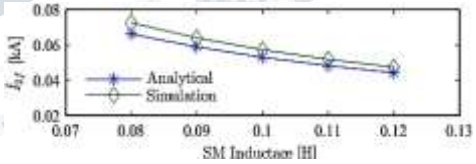

Fig. 13. Comparison between the simulated and analytically calculated values of 2nd harmonic circulating current with different values of SM inductance.

CSMMC BASED STATCOM

System parameters for the simulation of CSMMC based STATCOM are shown in Table III. The SM inductance of CSMMC is evaluated using (39) for energy power ratio E(S) = 30 kJ/MVA and the rated power S = 50 MVA

TABLE III
SYSTEM PARAMETERS FOR CSMMC BASED STATCOM

Grid Voltage/Frequency	$V_p = 115$ kV (line-line RMS), $f_0 = 50$ Hz
Coupling Transformer	115/11 kV, 50 MVA, $L_s = 0.16$ pu
Converter Parameters	$N = 4$, $S = 50$ MVA, $L_{SM} = 281$ mH, $C_{arm} = 15$ μF, $f_{sw} = 1$ kHz
DC-link reactor	$L_{dc} = 50$ mH
Filter Capacitance	$C_f = 75$ μF

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Simulation results during transition from capacitive to inductive mode of operation are shown in Fig. 14. It can be seen from the results that the settling time of the control system is less than 50 ms. The voltage waveform of phase-a and associated line current waveform on the secondary side (11 kV) of a coupling transformer are shown in Fig. 14(d). These waveforms show the transient free and fast response of the control system. Fig. 14(e) and Fig. 14(f) show the output line current of converter and the filter capacitor current respectively.

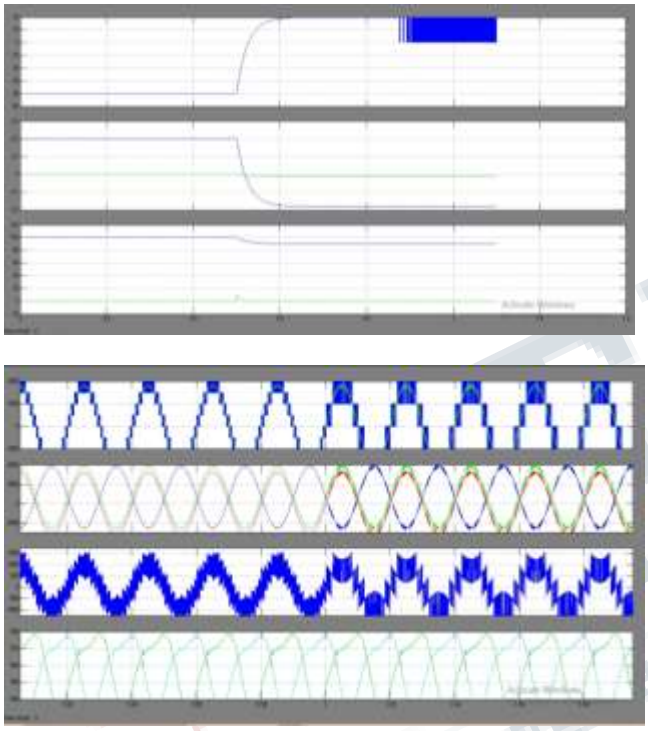
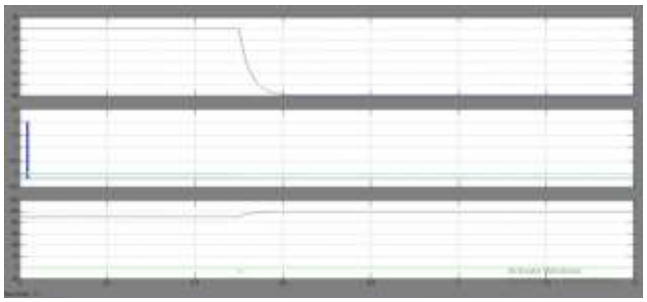


Fig. 14. Simulation results of STATCOM during transition from capacitive to inductive mode of operation at t = 5 s. (a) Reactive power (b) dq components of a gird current (c) dq components of a gird voltage (d) Phase voltage and current (11kV side) (e) Output current of converter (before filter) (f) Filter current.



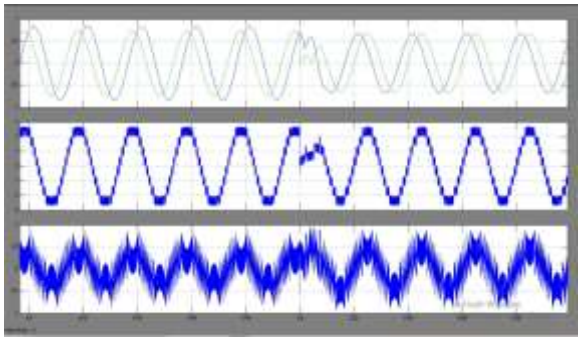


Fig. 15. Simulation results of STATCOM during transition from inductive to capacitive mode of operation at t = 6 s. (a) Reactive power (b) dq components of a gird current (c) dq components of a gird voltage (d) Phase voltage and current (11kV side) (e) Output current of converter (before filter) (f) Filter current.

A dc short circuit fault is tested to show the dc fault tolerance capability of the CSMMC and results are presented in Fig..

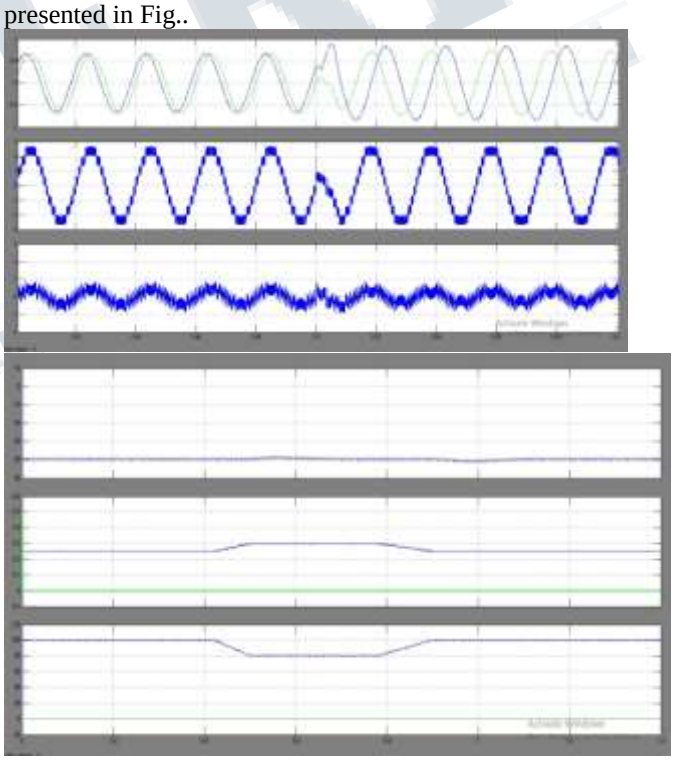


Fig. 16. Simulation results of STATCOM during AC fault on gird side at t = 7 s, for a duration of 0.5 s. (a) Reactive power (b) dq components of a gird current (c) dq components of a gird voltage.

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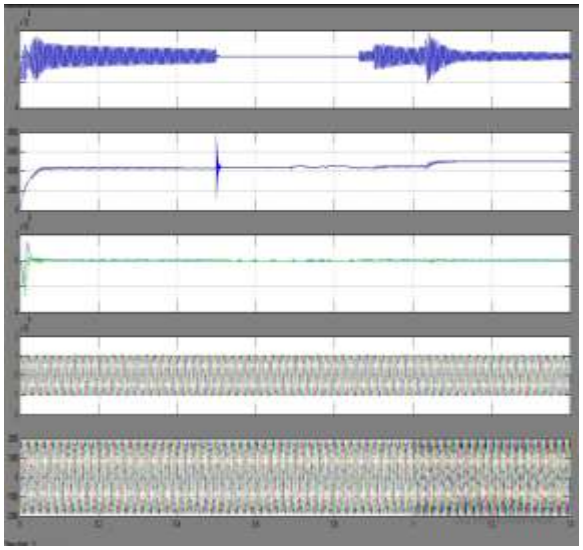

Fig. 17. Simulation results of STATCOM during DC fault at t = 11 s, for a duration of 0.2 s. (a) DC link current and voltage (b) Active and reactive

Power (c) and (d) Three phase voltages and currents (11kV side) The dc link inductor is used to suppress the dc current ripples in normal operation. During the dc fault it is shorted, and hence the dc-current ripples increase slightly.

II. CONCLUSION

The detailed analytical analysis of a CSMMC and its application as a STATCOM have been presented. In CSMMC, it is important to select SM inductance appropriately because it strongly influences the inductor current ripple. Hence, the method for SM inductance selection is proposed. To maintain the SM inductor currents at their reference values, a sorting based algorithm for inductor current balancing has been proposed. The control strategy in dq frame is presented for the CSMMC based STATCOM. The obtained results confirm that the properties of CSMMC correlate with the corresponding VSMMC. Hence the developments on CSMMCs and VSMMCs can be used as reference for each other. The study demonstrates that the proposed inductance selection method ensures the ripple of the SM inductor current within the rage. The study also shows that the proposed inductor current balancing strategy can effectively provide current balancing for the CSMMC inductors. Moreover, it is demonstrated that the CSMMC based STATCOM, using appropriately designed controllers, provides the desired dynamic response under different operating conditions. Hence, CSMMC can be considered as the potential candidate for HVDC and FACTS applications.

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