

# Design of High-Speed Multiplier Architecture Based on Vedic Mathematics

<sup>[1]</sup> Chaitanya CVS, <sup>[2]</sup> Sundaresan C, <sup>[3]</sup> P R Venkateswaran, <sup>[4]</sup> Keerthana Prasad, <sup>[5]</sup> V Siva Ramakrishna  
<sup>[1][2][4][5]</sup> School of Information Sciences, Manipal Academy of Higher Education, Manipal, Karnataka  
<sup>[3]</sup> Bharat Heavy Electricals Limited, Tiruchurapalli, Tamil Nadu

**Abstract-** High speed and efficient multipliers are essential components in today's computational circuits like digital signal processing, algorithms for cryptography and high performance processors. Invariably, almost all processing units will contain hardware multipliers based on some algorithm that fits the application requirement. Tremendous advances in VLSI technology over the past several years resulted in an increased need for high speed multipliers and compelled the designers to go for trade-offs among speed, power consumption and area. Amongst various methods of multiplication, Vedic multipliers are gaining ground due to their expected improvement in performance. A novel multiplier design for high speed VLSI applications using Urdhva-Tiryagbhyamsutra of Vedic Multiplication has been presented in this paper. The multiplier architecture is implemented using Verilog coding and synthesise during Cadence RTL Compiler. Physical design is implemented using Cadence Encounter RTL-to-GDSII System using standard 180nm technology. The proposed multiplier architecture is compared with the conventional multiplier and the results show significant improvement in speed and power dissipation.

**Keywords:** Binary Multiplication, Multiplier Architecture, Vedic Multiplier

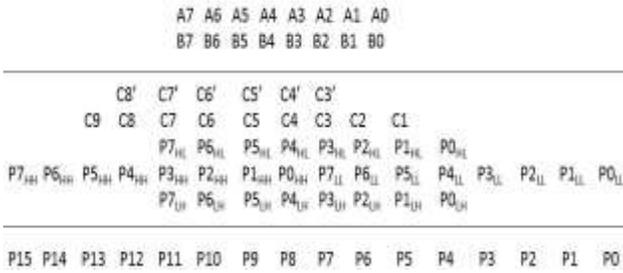
## I. INTRODUCTION

One of the most important classes of integrated circuits is processors. Over the years, the density of integration has grown tremendously and hence, today, it is possible to have large number of functionalities packed in an IC. As the number of functions increases, the need for computation also grows. Also, with the advent of new process technologies, shrinking of feature size coupled with the availability of modern CAD tools we could develop complex integrated circuits for various applications such as digital signal processing, mobile computations and communications, multimedia applications and processing required for scientific computing and applications. One of the main functional blocks in such circuits is arithmetic unit - the most important part of the processors- whose speed and efficiency are very crucial for meeting the requirements of the applications they have to support [1]. Multipliers have become an integral part of modern processors and computation systems. Especially, in digital signal processors speed of the computation is extremely important in addition to low power dissipation. Therefore, there is growing demand for low power and high performance multipliers [2]. As multiplication is a crucial arithmetic operation in processors and digital computer systems, multipliers are the core building block for many algorithms in a wide variety of computing applications [3, 4]. Although multipliers are main arithmetic components used for processing scientific data, the excessive power consumption and delay attracts attention from the research community. The current trends in architectures have been shifting towards multiple

arithmetic cores working in parallel so that they can process large amounts of data with relatively low power and delay. Unfortunately, traditional arithmetic units dissipate large amounts of power [5]. Thus there is a need to look at special multiplier architectures to be designed and implemented in appropriate circuit design styles [6-10] to achieve computation at low power, besides providing high performance. As the complexity of arithmetic core increases, the need for low power multipliers with adequate performance also grows. In order to address the low power computation along with high performance, a new approach to multiplier design based on ancient Vedic Mathematics has been explored. The mathematical operations using Vedic mathematics are very fast and require less hardware. This aspect of Vedic mathematics can be utilised to increase the computational speed of multipliers. This paper describes the design and implementation of an 8 bit Vedic multiplier based on Urdhva-Tiryagbhyam Sutra. The number of steps required to perform a multiplication operation by using Urdhva-Tiryagbhyam Sutra are considerably less compared to the conventional multiplication techniques [11]. In this paper, we have further explored a novel method to enhance the speed of a Vedic multiplier by replacing the existing full adders and half adders with multiplexers. The implementation of pre-computation logic using multiplexer based adder and XOR logic resulted in reduction of delay. Moreover, in this paper, we also propose modifications to the conventional architecture of multiplier so as to reduce the power-delay product.

The structure of the paper is divided as follows: The methodology and the architecture of the proposed Vedic





**Figure 5: 8 bit Vedic Multiplier with expanded 4 bit module**

**IV. RESULTS**

The synthesis of conventional & Vedic multiplier digital circuits was implemented using Verilog coding with the help of Cadence Encounter RTL Compiler in 180nm technology. The physical Design for the multipliers was obtained using Cadence Encounter RTL-to-GDSII System. The input to the tool was the netlist file generated from the Cadence Encounter RTL Compiler. The remaining parameters and specifications used were standard values already specified within the tool. While inputting the Import Design Browser in the Physical Design, the MMMC File is set with both the best and worst case libraries. Delay, Power & Area was estimated from the Physical Designs. The results obtained from the proposed multiplier are given in the table 1 and 2. Cadence Design Compiler was made use of while synthesis and Cadence Encounter RTL-to-GDSII System for obtaining the Physical Layout using standard 180nm technology. The Physical layout of the proposed multiplier has been shown in Figure 6. The Power-Delay Product obtained from the Vedic Multiplier is 29.62 % less than the conventional Multiplier. But, the area is 11.54 % more than the conventional design. The delay was 20.94 % less than the Conventional Multiplier delay which is within the target specification i.e., 10 to 30%. The high speed multiplication is achieved with the overhead in area and power.

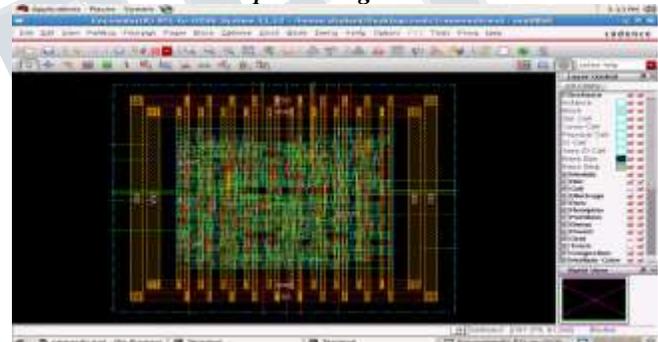
**V. CONCLUSION**

In this paper, a high speed and low power architecture for multiplier was proposed using algorithm based on Vedic mathematics. An 8 bit Vedic Multiplier using Urdhva-Tiryagbhyam Sutra has been designed and implemented. The conventional architecture has been integrated with pre-computation logic in which adders were replaced by multiplexers. The results show that the architecture is 20.94% faster, dissipates 10.99% less power and 29.62 % improvement in terms of power delay product when simulated in 180nm technology. This clearly demonstrates that the primary objective of design of an efficient multiplier

and reduction of power-delay product in comparison with conventional multiplier and divider has been achieved. This will surely help increase the computation speed of MAC and other Arithmetic units in processors, leading to faster execution of instructions.

FACTORS	VEDIC MULTIPLIER	CONVENTIONAL MULTIPLIER	PERCENTAGE CHANGE
DELAY(ns)	4.029	5.967	32.48%
LEAKAGE POWER( $\mu$ W)	6.79	7.43	8.66%
DYNAMIC POWER( $\mu$ W)	95.20	86.59	- 9.94%
TOTAL POWER( $\mu$ W)	101.99	94.02	- 8.47%
TOTAL AREA	1667	1516	- 9.96%
POWER DELAY PRODUCT	410.92	561.04	26.75 %

**Table 1: Summary of Post Synthesis Layout Results for Multiplier using Cadence**



**Figure 6: Physical Design Layout of Vedic Multiplier**

FACTORS	VEDIC MULTIPLIER	CONVENTIONAL MULTIPLIER	PERCENTAGE CHANGE
DELAY(ns)	7.578	9.585	20.94 %
LEAKAGE POWER( $\mu$ W)	0.2678	0.4075	34.28 %
SWITCHING POWER( $\mu$ W)	233.8	188.4	- 24.10 %
INTERNAL POWER( $\mu$ W)	292.7	402.9	27.35 %
TOTAL POWER( $\mu$ W)	526.7	591.7	10.99 %
TOTAL AREA( $\mu$ m <sup>2</sup> )	25,642.5	22,989.69	-11.54 %
POWER DELAY PRODUCT	3,991.33	5,671.44	29.62 %

**Table 2: Summary of Post Physical Design Results for Multiplier using Cadence**

The power dissipation can be further reduced by employing existing low power techniques like Dynamic Voltage Scaling, operand isolation, use of Multiple Vth devices etc., in the design of multiplier. Reduction of delay can be further improved by designing the pre-computation logic using

**International Journal of Science, Engineering and Management (IJSEM)**  
**Vol 3, Issue 4, April 2018**

---

Quine McCluskey solver in such a way that the number of carries generated in each column will be reduced.

**REFERENCES**

- [1] Subhendu Kumar, Abhijit Ashati, Rasmita Sahoo and Chandra Shekhar, "A High-Speed Radix-64 Parallel Multiplier using A Novel Hardware Implementation Approach for Partial Product Generation based on Redundant Binary Arithmetic", First International Conference on Emerging Trends in Engineering and Technology, Proceedings published by IEEE Computer Society, 2008.
- [2] S.Karthik and Priyanka Udayabhanu, "FPGA Implementation of High Speed Vedic Multipliers", International Journal of Engineering Research & Technology, Volume I, Issue-10, December 2012.
- [3] IsraekKoren, "Computer Arithmetic Algorithms", 2nd ed., Universities Press, 2003.
- [4] Mohamed Raffiquzzaman, Chandra Rajan, "Modern Computer Architecture", 1st ed., Galgotia Publication pvt.Ltd., 2008.
- [5] U.G. Nawathe, M. Hassan, K.C. Yen, and A. Kumar, "Implementation of an 8-Core, 64-Thread, Power-Efficient SPARC Server on a Chip", IEEE Journal of Solid-State Circuits, vol. 43, no. 1, pp. 6-20, January, 2008.
- [6] Varsharani V H, Prabha S K, B.P. Patil, "Performance Evaluation of Proposed Vedic Multiplier inMicrowind", International Journal of Communication Engineering Applications, Vol. 3, Issue. 3, pp. 498-502, July 2012.
- [7] R. K. Bathija, R. S. Meena, S. Sarkar, Rajesh Sahu, "Low Power High Speed 16x16 Multiplier Using Vedic Mathematics", International Journal of Computer Applications, Vol. 59, No. 6, pp. 41-44, December, 2012.
- [8] Premananda B. S, Samarth S. Pai, Shashank B, Shashank S. Bhat, "Design and Implementation of 8-bit Vedic Multiplier", International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering, Vol. 2, Issue 12, pp. 5877-5882, December, 2013.
- [9] Sowmiya M, Nirmal Kumar R, S Valamathy, Karthick, "Design of Efficient Vedic Multiplier By The Analysis Of Adders", International Journal of Emerging Technology and Advanced Engineering, Vol. 3, Issue 1, pp. 396-403, January, 2013.
- [10] Ramesh Pushpangadan, VineethSukumaran, Rino Innocent, Dinesh Sasikumar, VaisakSundar, "High Speed Vedic Multiplier for Digital Signal Processors", IETE Journal of Research, Vol. 55, Issue 6, pp. 282-286, November-December, 2009.
- [11] P. Mehta, D. Gawali, Conventional versus Vedic mathematical method for hardware implementation of a multiplier, in: Proceedings of the IEEE International Conference on Advances in Computing, Control, and Telecommunication, Trivandrum, Kerala, December 2009, pp. 640-642
- [12] SreechhariVeeramachaneni M.B. Srinivas, "Novel High-Speed Architecture for 32-Bit Binary Coded Decimal (BCD) Multiplier", International Symposium on Communication and Information Technologies (ISCIT), 21 - 23 October, 2008.
- [13] J. Rabaey, A. Chandrakasan, and B. Nikolic, "Digital Integrated Circuits", 2nd ed., Prentice Hall Pears.