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A Survey on CORDIC algorithm and its Implementation

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Abstract: COordinate Rotation DIgital Computer(CORDIC) is an uncomplicated and efficient algorithm for performing mathematical tasks such as the calculation of trigonometric, hyperbolic and logarithmic functions, real and complex multiplications, division, square-root and many more using simple add, subtract and shift operations. Rectangular to polar conversion is an imperative operation in ALU, DSP processors, wireless communication, multimedia etc.To achieve this conversion there is a need of squaring, square root and arctangent circuits, which make it complex with high area and power requirement. To compensate this, rectangular to polar conversion is carried out using CORDIC architecture. This paper presents a survey on pipelined CORDIC architecture for rectangular to polar conversion.

Keywords: CORDIC algorithm, pipelining, VHDL, XILINX ISE.

1. INTRODUCTION

CORDIC is acronym for COordinate Rotation DIgital Computer. Two dimensional geometry forms the basis of CORDIC arithmetic but the iterative method of a computational algorithm to implement this was first given by Jack E. Volder to compute multiplication, division and trigonometric functions in 1959[1], [2].

The key concept of coordinate rotation digital computer (CORDIC) algorithm revolves around a simple shift-add iterative procedure. This shift-add iterative achieves computing tasks by functioning in either vectoring-mode or rotation-mode following any one among linear, hyperbolic, and circular trajectories [3]. CORDIC functionality is workable in rotation as well as vectoring-modes for applications such as synchronization in digital receivers, 3-D graphics processor, phase and frequency estimations, eigen value estimations, QR decomposition, interpolators, singular value decomposition etc. CORDIC operates in both circular and hyperbolic trajectories for 3-D structures such as hyperboloids, paraboloids and ellipsoids. To realise these application in hardware there is a need to use multiple CORDIC processors for operation in different modes and trajectories. Multiple CORDIC processors are replaced by a reconfigurable CORDIC, which can operate in rotation and vectoring-modes, for both circular and hyperbolic trajectories. A reconfigurable CORDIC finds usage in communication systems, signal processing, 3-D graphics, multimedia etc.

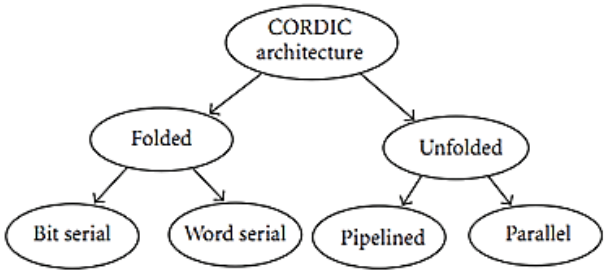

Figure 1: Classification of CORDIC architecture

Figure1 above gives us an idea of classification of CORDIC architectures., This classification is based on three iterative equations . Folded architectures is realised by duplicating each of the difference equations of the CORDIC algorithm into hardware and time multiplexing all the iterations into a single functional unit. Folding gives an option of trading area for time in signal processing architectures. The folded architectures are further subdivided into bit-serial and word-serial architectures on the basis of functional unit implemented. The CORDIC algorithm conventionally has been implemented using bit serial architecture with all iterations executed within same hardware [3] and this slows down the computational device rendering it unsuitable for high speed implementations. The word serial architecture [7, 48] is an iterative CORDIC architecture obtained by realizing the iteration equations and employs the modified shifters in each iteration to cause the desired shift for the iteration. The lookup table provides the appropriate elementary angles. The major burden is enforced by borrow propagat addition/

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subtraction and variable shifting operations, forcing the conventional CORDIC [7] implementation slow for high speed applications. Unfolding scheme helps to rectify this such that each of the processing elements always perform the same iteration as shown in Figure 5.The unfolded pipelined architecture scores over the folded architecture in terms of high throughput which is achievable due to the hard- wired shifts rather than time and area consuming barrel shifters and elimination of ROM. The pipelined architecture delivers throughput improvement by a factor of n for n-bit precision at the price of increasing the hardware by a factor less than n.

II. BRIEF LITERATURE SURVEY

COordinate Rotation DIgital Computer is shortened as CORDIC. Two-dimensional geometry forms the basis of CORDIC arithmetic however the iterative method of a computational algorithm to implement this was presented by Jack E. Volder to compute multiplication, division and trigonometric functions in 1959[1], [2].

Concept, Design, and Implementation of Reconfigurable CORDIC Supriya Aggarwal, Pramod K. Meher, and Kavita Khare IEEE Transactions On Very Large Scale Integration (VLSI) Systems 2016.

The proposed scheme allows CORDIC to work in different modes and trajectories of operations. It is employed in synchronizers, waveform generators, low-cost scientific calculators with almost no effect on the maximum operating frequency. This presented scheme save approximately 60% of the area compared to the conventional CORDIC architecture.

Implementation of a Fast Hybrid CORDIC Architecture Bhawna Tiwari, Nidhi Goel 2016 Second International Conference on Computational Intelligence & Communication Technology IEEE 2016.

In this work the authors have shown that the proposed architecture is faster in execution at expense of reduced accuracy and high power consumption as compared to the reference architecture.

CORDIC-based FFT Real-time Processing Design and FPGA Implementation Aimei Tang*, Li Yu, Fangjian Han, Zhiqiang Zhang, 2016 IEEE 12th International Colloquium on Signal Processing & its Applications (CSPA2016), 4 - 6 March 2016, Melaka, Malaysia.

The proposed method minimizes the hardware complexity of the system sue to the usage of pipelined structure, the dual-port RAM, butterflies of the radix-2Decimation-In-Time (DIT) algorithm.It also improves the Signal Noise Ratio.

CORDIC II: A New Improved CORDIC Algorithm Mario Garrido, Member, IEEE, Petter Källström, Martin Kumm and Oscar Gustafsson, Senior Member, IEEE Ieee Transactions On Circuits And Systems Part Ii: Express Briefs 2016.

With lots of versions of CORDIC algorithm being available the authors have presented a scheme for substitution of CORDIC micro-rotation and have proposed a new algorithm called CORDIC II which uses minimum number of adders as compared with the other CORDIC algorithm as it uses new variety of rotators.

CORDIC Architectures: A Survey B. Lakshmi and A. S. Dhar, Hindawi Publishing Corporation VLSI Design Volume 2010, doi:10.1155/2010/79489

This paper does a brief survey and classifies different CORDIC algorithm and also focuses on algorithm that pre compute the direction of rotations. Special focus and more stress have been given on higher radix and redundant algorithms.

III PROBLEM DEFINITION

For FPGAs are implemented using DSP algorithm, which employs algebraic function, like square, square root, adder, and arctangent which are approximated using Taylor series rendering the problem to a sequence of multiply and adds operations. However an alternate scheme based on the Coordinate Rotation Digital Computer (CORDIC) algorithm can also be considered. This algorithm employs simple add, subtract and shift operations, reducing the hardware complexity and improving the throughput by pipelined CORDIC resulting in small, cheap, fast in calculation and reconfigurable hardware.
Rectangular to polar conversion is a prime operation in ALU and DSP processors wireless communication, multimedia etc. The conversion need hardware implementation of squaring, square root, adder, and arctangent circuits which results in hardware complexity, large area requirement and high power consumption. Various implementation of CORDIC algorithm are available with its own pros and cons. So various existing

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methods have been studied and compared. From the study it is concluded that amongst all architectures the pipeline CORDIC algorithm can turn out to be the best suited algorithm to implement rectangular to polar conversion.

V CORDIC Implementation

Figure 2 shows the block diagram of CORDIC processor. Three fundamental blocks of CORDIC Processor are the pre-processor, the post-processor and the actual CORDIC core.

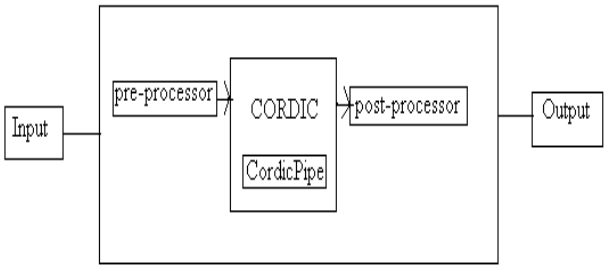

Figure 2: Block Diagram of CORDIC processor

1.Pre-Processors and Post-Processors

The arctan table used in the CORDIC algorithm allows it to converge in the range of –1(rad) to +1(rad). To use the CORDIC algorithm over the entire 2π range the inputs need to be manipulated to fit in the –1 to +1 rad. range. The pre-processor handles this manipulation. The post-processor corrects this and places the CORDIC core's results in the correct quadrant.

2. CORDIC

The actual CORDIC algorithm is performed by CORDIC Processor, therefore CORDIC core is considered as the heart of the CORDIC Processor Core. A pipeline of CordicPipe blocks are used to make the CORDIC and each CordicPipe block represents a single step in the iteration processes. For each iteration and the logic, the a tan table is employed. Pipelined structure achieve the iterations. Pipelined structure modifies the CORDIC transformation in every clock cycle enabling it to give a high throughput.

3. CORDIC Pipeline

A pipeline of CordicPipe blocks are employed to achieve the CORDIC and the CordicPipe core performs each iteration step to manipulate the values as shown in the figure 3.

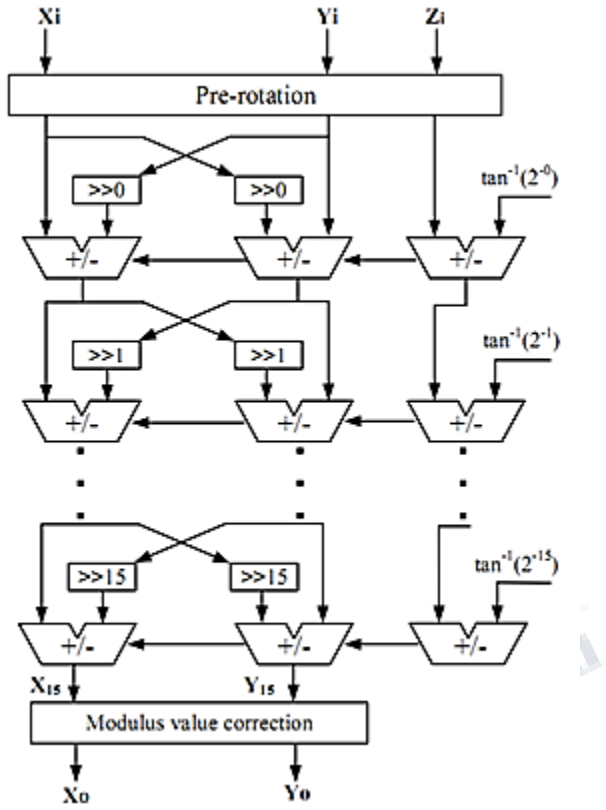

Figure 3: CORDIC Pipeline

VI. CONCLUSIONS

Rectangular to polar conversion is an important operation in many applications, which uses complex hardware. We conclude that we have been able to study different approaches with their pros and cons .We have been able to discuss the CORDIC concept which uses simple add, subtract and shift operations. The CORDIC algorithm can be coded in VHDL language and simulation can be done on XILINX ISE software.

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