ISSN (Online) 2394-2320

International Journal of Engineering Research in Computer Science and Engineering (IJERCSE)
Vol 8, Issue 6, June 2021

Design and Optimization of Reversible Binary to Gray and Gray to Binary Code Converter with Power Dissipation Analysis using QCA

[1] Aamir Suhail Taray, [2] Purnima Hazra, [3] Satyendra Kumar Singh
[1][2] SMVDU, Katra , J&K
[3]MIET, JAMMU, J&K

Abstract: Whenever an evolving technology approaches a dead end, a new technological revolution is needed. "The present" VLSI technology is based on the technology of CMOS. Due to the new challenges in the existing technology, the advanced technology based on quantum-dot cellular automata (QCA) has been introduced.QCA is an interesting area in nano-computing technology, providing an alternative approach to resolve the physical limitations faced by CMOS systems during further down scaling of their significant sizes. At nanometer scale, QCA offers powerful features like higher packaging density, minimized area, much lesser power consumption and better operating speed. Current logic gates really aren't power saving or energy efficient because they are not inherently reversible in nature and thus results in the dissipation of energy. Therefore, a serious effort is required to provide an effective model for the design of circuits that do not dissipate energy and hence preserve information. Power-efficient circuits can be constructed with more precision which ultimately increase the lifetime and speed of the circuit using this technique. The successful design of the Feynman gate-based reversible Binary to Gray and Gray to Binary code converter using QCA is presented in this paper. The proposed design proves to be efficient in terms of cell size, cell count, overall area, latency and complexity. The outcome shows that the configuration of the design is territory proficient and has a lower clock delay. Besides, the circuit setup is extremely clear and did not use any flipped, translated QCA cells, and offers single-layer access to their information sources and outcomes. This encoder circuit using reversible logic gates can be further explored for the designing of other low power loss devices"."In addition to this for the first time energy dissipation analysis for different scenarios is also done on all the designs using QCA Pro-tool and it is observed that the proposed designs dissipate minimum energy thereby making them suitable for Ultra-low power designs. All the proposed reversible code converter prototypes have been simulated and the QCA Designer tool has checked their credibility successfully".

Keywords: Meta- Binary Code, Energy estimation, Feynman Gate ,Gray Code, , Latency, QCA Designer, QCA Pro tool, Ultra Low Power.

I. INTRODUCTION

In the VLSI domain, the CMOS created a new era in IC technology with an optimized " form of digital circuits. "It was as early as 1965, when Gordon Moore, wrote a paper entitled "Cramming more Components onto Integrated Circuits", where he first predicted that the number of transistors that can be integrated on to a single chip will be double in every18months"[1].This trend results in decreased feature size and power dissipation with higher device densities. "However, when scaling comes down to submicron level in C-MOS many problems have started" to occur [2]. The challenges like un-deterministic leakage current, quantum tunneling, power dissipation and short channel effects hinder the further scaling down process of CMOS circuits [3]. Hence the performance of CMOS circuits degrades at such smaller scales. As an alternative to CMOS-VLSI which causes serious limitations at the nano level, there is a need to devise an alternating approach that could overcome the above said" shortcomings. Dr. Criag S. Lent has proposed one of the nanotechnologies called as Quantum-dot Cellular Automata (QCA) at the "University of Notre Dame" [4-5]. QCA is an alternative technique for current CMOS technology."It is predicted as one of the future nanotechnology in the report of Semiconductor Industries Association's International Roadmap for Semiconductors" (ITRS)[6]."Because of its high

ISSN (Online) 2394-6849

International Journal of Engineering Research in Computer Science and Engineering (IJERCSE)
Vol 8, Issue 6, June 2021

density of devices, exceptionally low power consumption and very high operating speed, QCA has gained considerable attention in recent years. The QCA is a new technology for nano-scale circuits with efficiency in structure and power consumption that can play influential role in next generation computing systems. In terms of future size, it is predicted that QCA cells of few nano-meter (nm) would be possible candidate in near future. The primary unit of this nanotechnology is a QCA cell and its size is much smaller than the size of the smallest transistor".

"The efficient design of the Feynman gate-based reversible Binary to Gray and Gray to " Binary code converter using QCA has been proposed in this paper which proves to be effective in terms of cell size, cell count, overall area, latency and complexity"."In addition to this energy dissipation analysis for different scenarios is also done on all the designs using QCA Pro tool and it is observed that the proposed designs dissipate minimum energy thereby making them suitable for ultra-low power designs". The remaining portion of the article is arranged as:"The description of each and every element of the QCA is found in Section II. It offers details on QCA, its cell functioning and all other essential information on the fundamentals of QCA. Proposed work is included in Section III. The prototypes of proposed designs are also shown in this section and contains outcomes, which are" the outcomes of the simulation."In addition to this energy dissipation analysis for different scenarios is given in section IV and essentially in the last section; that is, Section V; concludes conclusion and possible scope in future".

qca background

In 1993, C. S. Lent introduced "Quantum dot Cellular Automata as an alternative of " CMOS technology [4]. It has been accepted as one of the most innovative nano-scale computing methods. A major benefit of QCA over other nano-electronic architectural styles is that it is possible to create wires carrying logic signals using the identical cells that are used for producing logic gates. QCA enables operating frequencies in the THz range and the density of system integration is around 900 times greater than the existing end of CMOS scaling limits, which is not feasible in present CMOS technology. The basic unit of QCA circuit is QCA cell which consists of four quantum dots which are arranged in a square pattern as shown in Figure 1."Zhang et al. " have stated the cell is charged with two excess electrons which can be allowed to tunnel between the different quantum dots by a clocking mechanism [7]. As a result of their mutual electrostatic repulsion, these electrons appear to occupy the antipodal sites. The movement of information from one cell to an adjacent cell is the duty of columbic repulsion. Therefore there are two energy-minimal equivalent arrangements of the two electrons in the QCA cell, as shown in Figure1.These two mechanisms are known as cell polarization P = +1 and P = -1, where P= +1 represents logic "1" and P= -1 represents logic "0". Binary information is encoded in a QCA cell using this polarized charge configuration. Also there are special purpose rotated cells. The standard cell and the rotated cell do not interact with one another while they are aligned, so rotated cells can be used for coplanar wire crossings. One of the most significant feature of the QCA cell is that both functions can be performed, i.e., it can be used both for the design of logic structure, as well as for interconnections".

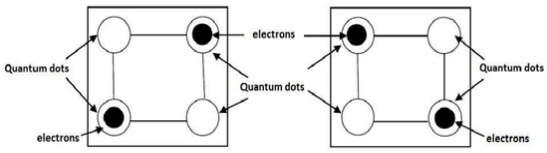


Fig 1: Basic QCA cell with two possible polarisations.

"In any QCA cell, the two electrons will occupy diagonal direction because of the force " of repulsion between them. If one electron switches its position, the other electron will automatically switches its position within the cell to achieve P = +1 or P = -1 polarization state. Now if both QCA cells are adjacent to each other, the second cell will match its configuration with the first QCA cell. For example, if the first QCA cell is at P = +1 polarization state, then the second adjacent QCA cell will also be at the P = +1 polarization state because of the columbic force between them. The polarity of cell 2 is activated by the polarity of neighboring cell 1 as shown in Figure 2."

ISSN (Online) 2394-6849

International Journal of Engineering Research in Computer Science and Engineering (IJERCSE)
Vol 8, Issue 6, June 2021

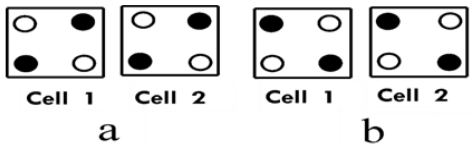


Fig 2: Cell to Cell Response

QCA Based Logic Devices

"The details of QCA logic devices were given by Walus et al. (2004) [10]. The QCA logic primitives include QCA cable/wire, QCA inverter, and QCA majority gate as mentioned below".

QCA Wire

As in Figure 3 QCA has two kinds of wires, 90^0 QCA wire and 45^0 QCA wire. "The QCA wire (90^0) is formed by connecting the cells in a cascade [10] as shown in Fig 3 a. The Binary logic state propagates from the left hand side to the right hand side via columbic interactions between QCA cells. The QCA cells connected in cascade will follow the charge configuration of their previous adjacent cell. Hence this creates a Binary logic state at the output cell. The QCA wire (45^0) having an orientation of 45^0 [11] can transfer the logic state which switches alternatively between P = "+1" and P = "-1" polarization for every QCA cell connected in cascade as shown in Fig 3 b. The main advantage of QCA 45^0 wire is that it transfers the logic state without the use of an inverter circuit." Also QCA wires have the peculiar property that " they can pass through the plane without the destruction of the value being transmitted on either wire [12]. But this property holds only if the QCA wires have different orientations".

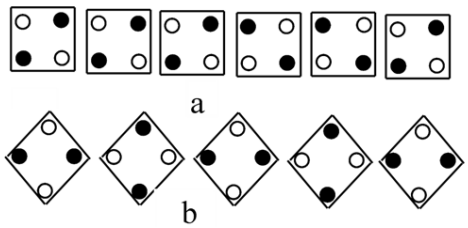


Fig 3: (a) 90^0QCA wire (b) 45^0 QCA wire

QCA Inverter

"An Inverter is a gate which inverts the signal at the output. The three different QCA Inverter designs are half-cell inverter, robust inverter and rotated cell inverter as shown in Fig 4(a), (b) and (c). The Half-Cell inverter uses diagonally placed QCA cells along with "IN" and "OUT" cells [13]. The major drawback of such type of cell arrangement is that the diagonal cell will not be able to get fully polarized in the opposite direction than the preceding QCA cell. Another robust inverter design in [14] has properly aligned input and output QCA cells." The major drawback of such design is that it increases " the occupational area. The rotated cell inverter in [15] is the most robust design which gives stable polarization state at the output. Also this design Utilizing only four QCA cells, hence occupies the less area in comparison to the other two designs"

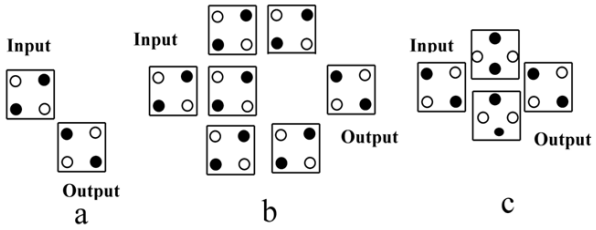


Fig 4: Types of QCA Inverters

Majority Gate

"The QCA equivalent of 3-input majority gate is formed by joining five cells i.e. 3 input cells, 1 device cell and 1 output cell as shown in Fig 5. The cells A, B and C are the input QCA cells and the OUT is an output cell. The working of 3-Input majority Gate is based upon the principle that the majority of the inputs wins at the output" [16].

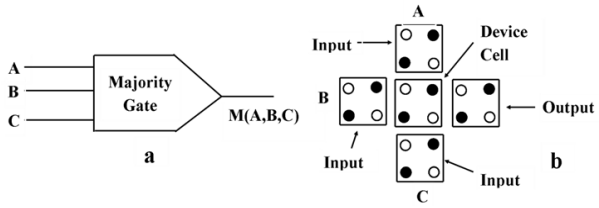


Fig 5: Structure of 3 input majority gate

"The logic function of 3-input Majority Gate (MG) is expressed in terms of Boolean functions as:"

$$M(A, B, C) = AB + BC + AC \quad (1)$$

"The three input MG can be used to construct both AND gate and OR gate. The logic gates are designed by fixing one of the input of 3-input MG to either 1 or 0. For designing AND gate, the third input is fixed at logic 0 and for designing OR gate, the 3rd input cell is fixed at logic 1. Both the AND

ISSN (Online) 2394-6849

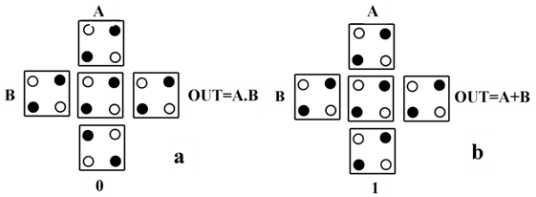
International Journal of Engineering Research in Computer Science and Engineering (IJERCSE)
Vol 8, Issue 6, June 2021

gate and OR gate designs are presented in Fig 6 (a) and (b) [16]."

"The Logic expression of AND gate and OR gate is given by:"

$$AND(A, B) = M(A, B, 0) = A.B \quad (2)$$

$$OR(A, B) = M(A, B, 1) = A + B \quad (3)$$



"Fig 6: (a)AND Gate (b) OR Gate Using 3-input MG"

QCA Clock Theory

"The synchronization of information in a QCA circuit is controlled by a clocking mechanism [17].A QCA clock has 4 clock phases: Switch, Hold, Release and Relax phase as shown in Fig 7"

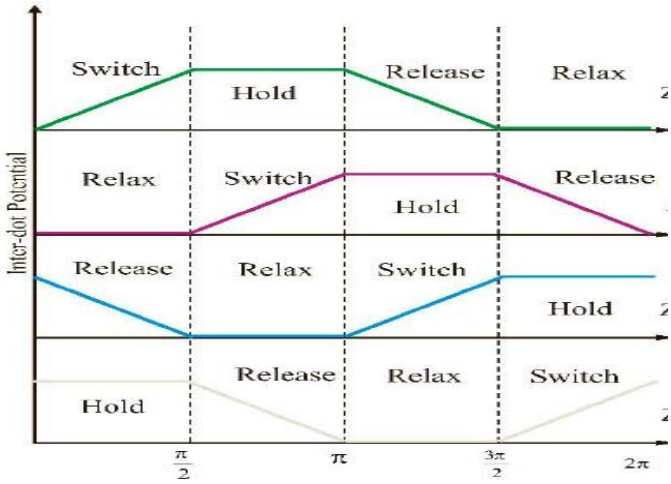


Fig 7: Four stages of QCA clocking [18]

When the clock signal is applied to a QCA cell, it " undergoes all the four phases of a clock. When QCA cell is in switch phase, the clock field strength starts increasing and the cell starts polarizing. When the QCA cell is in hold phase, the field strength is maximum and the cell gets fully polarized. In this phase, the QCA cell will attain its logic state '0'or'1'.In release phase, the clock field strength starts decreasing and the QCA cell will start depolarizing. In relax phase, field strength is minimum and QCA cell gets fully depolarized [19]".

IV Proposed Work

"The researchers have already documented a lot of work on reversible logic circuit design based on QCA. The proposed FG is used in QCA to construct reversible Binary to Gray and Gray to Binary code converter circuits. With the assistance of the majority gate, the suggested Feynman gate is intended. The Feynman [20] gate is a 2x2 reversible gate and is also known as CNOT (Controlled NOT) gate is of considerable importance in quantum computing. The implementation of the QCA circuit and the simulation performance of the proposed Feynman gate is shown in Fig. 8 and 9 respectively".

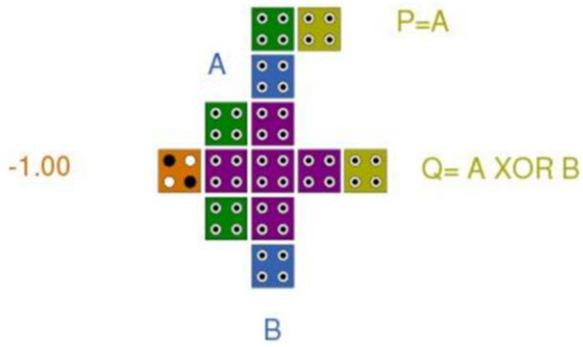


Fig 8: (a) QCA implementation of Feynman gate

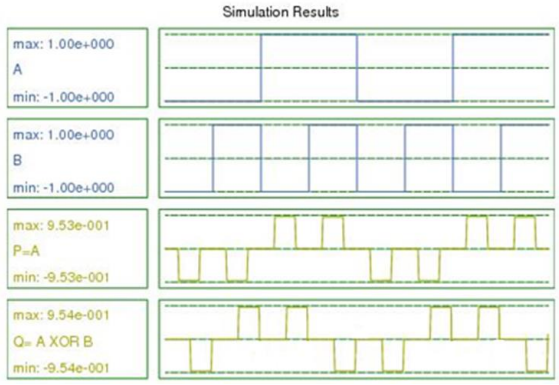


Fig 9: Simulation result of suggested gate

A. Proposed Design of 3-bit Reversible Binary to Gray Code Converter

"Coding is used in data communication to transmit information between computers for accurate and secure information transmission. A code converter is a

ISSN (Online) 2394-6849

International Journal of Engineering Research in Computer Science and Engineering (IJERCSE)
Vol 8, Issue 6, June 2021

logical circuit that converts one kind of code into another. To secure private information from spies, code converters are used. Code converters have also found applications in algorithm generation and communication [21-22]." "Thus, in the first step, a new well-optimized conversion technique like Binary-to-Gray and Gray-to-Binary converter is explored for implementation using QCA. Consider a 3-bit reversible code converter with an X(A,B,C) Binary input vector and an Y(P,Q,R) Gray output vector. Table 1 shows truth table of 3-bit reversible Binary to Gray code."

Table 1: Truth table of 3-bit reversible Binary to Gray code converter

X(Binary Code)			Y(Gray Code)		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	1
0	1	1	0	1	0
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

"Table 1, illustrates that the outputs are related to input with the following equations:"

$$P = A \quad (4)$$

$$Q = A \oplus B \quad (5)$$

$$R = B \oplus C \quad (6)$$

"It is clear from the above equations that only two XOR operations are needed to create Gray code. Thus, the 3-bit Binary to Gray code converter can easily be implemented with only one garbage value using the special feature of reversible FG, as shown in Fig 10".

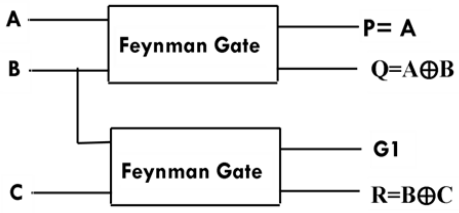
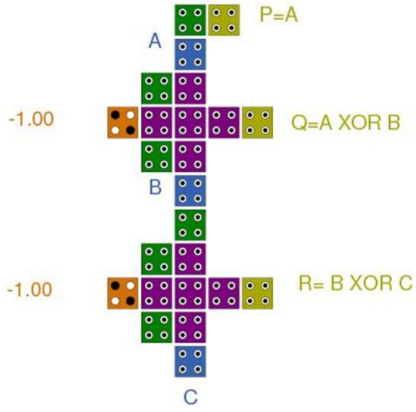
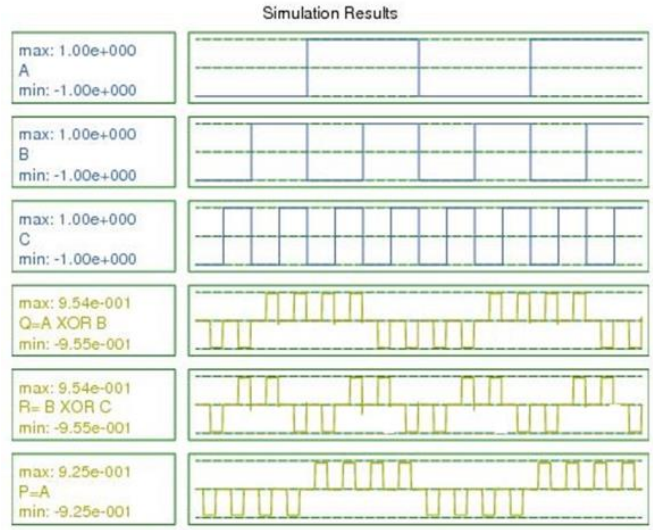


Fig 10: Schematic representation of 3 bit binary to gray code

"Fig.11and12 demonstrate the suggested Feynman gate-based 3-bit Binary to Gray Code Reversible Converter with Implementation and outcome of simulation using QCA"



"Fig 11: Proposed Feynman gate-based 3-bit Binary to Gray code reversible converter"



""Fig 12: Simulation result of suggested converter

Table 2:Comparative analysis of different Reversible Feynman Gates and Binary to Gray Code converter.

ISSN (Online) 2394-6849

International Journal of Engineering Research in Computer Science and Engineering (IJERCSE)
Vol 8, Issue 6, June 2021

GATE	Refrences	CELL COUNT	AREA (μm²)	DELAY
F	[23]	75	0.08	1.25
E	[24]	54	0.038	0.50
Y	[25]	53	0.07	0.75
N	[26]	43	0.038	0.75
M	[27]	34	0.036	0.75
A	**In this work**	**13**	**0.00972**	**0.50**
n				
Binary	[28]	108	0.0751	3
to	[29]	75	0.0554	2
Gray	[30]	56	0.0427	NA
Converter	[31]	29	0.0275	0.5
	IN THIS WORK	**24**	**0.0178**	**0.5**

B Proposed Design of 3-bit Reversible Gray to Binary Code Converter

"Consider a 3-bit Gray to Binary code converter that represents X (A,B,C) as the input vector and Y(P,Q,R) as the output vector. Figure 15 displays schematic diagram of the 3-bit Gray to Binary code converter".

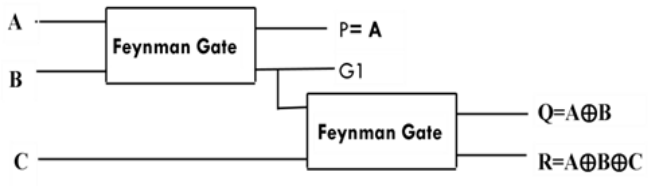


Fig 13: Schematic representation of 3 bit gray to binary code converter using Feynman Gate.

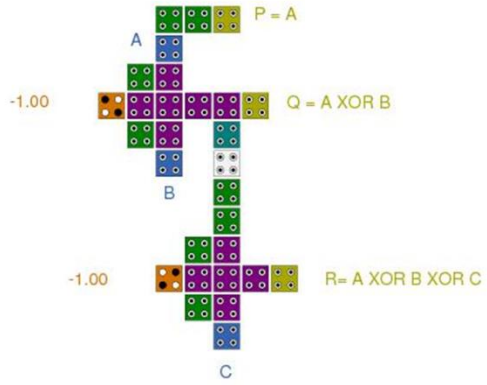
"With the equations given, the input output relationship can be expressed as:"

$$P = A \quad (7)$$

$$Q = A \oplus B \quad (8)$$

$$R = A \oplus B \oplus C \quad (9)$$

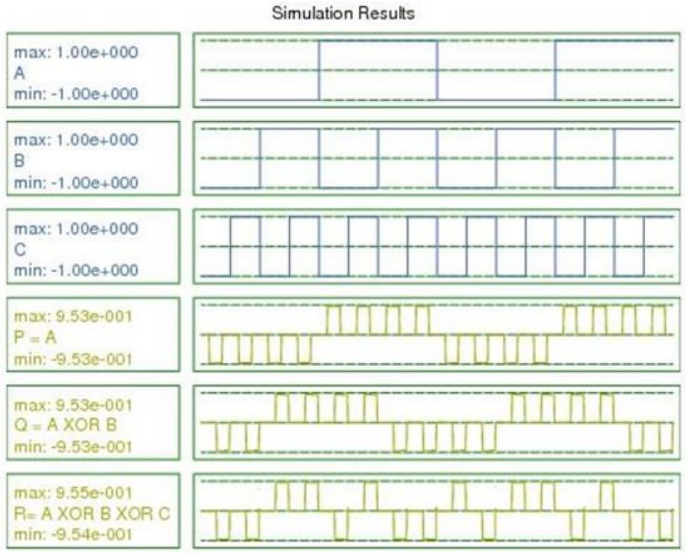
"Figures 14 and 15 display the proposed Feynman gate based 3bit reversible Gray to Binary code converter along with QCA implementation and simulation result. For the configuration of the reversible Gray to Binary code converter, the same Feynman gate is used. Table 3 shows the comparative analysis of various Gray to Binary code converters".



"Fig 14: Proposed Feynman gate-based 3-bit Gray to Binary code reversible converter"

Table3:Comparative analysis of different Reversible Gray to Binary Code converter.

Gate	References	Cell Count	Area (μm²)	Delay
Gray To Binary Code Converter	[28]	108	0.0178	NA
	[29]	114	0.1169	4
	[32]	112	0.069	4
	[33]	194	0.2844	NA
	Proposed Work	**29**	**0.0233**	**1**



"Fig 15: Simulation result of suggested converter

V Power dissipation analysis

ISSN (Online) 2394-6849

International Journal of Engineering Research in Computer Science and Engineering (IJERCSE)
Vol 8, Issue 6, June 2021

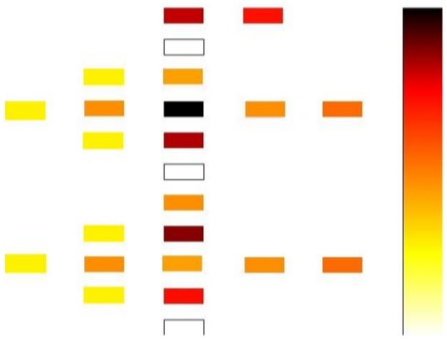
""QCA Pro tool, a probabilistic modeling tool [28] has been used for energy dissipation analysis. The total energy and power of a QCA cell can be measured using a Hamiltonian matrix .The Hamiltonian for an array of QCA cells using Hartree–Fock approximation [34] and by considering the Coulombic interaction between them by a mean- field approach is exposed as" [35].

$$H = \begin{pmatrix} -0.5E_K\sum_i P_iF_i & -\gamma \\ -\gamma & 0.5E_K\sum_i P_iF_i \end{pmatrix} = \begin{pmatrix} -0.5E_K\bar{P} & -\gamma \\ -\gamma & 0.5E_K\bar{P} \end{pmatrix} \quad (10)$$

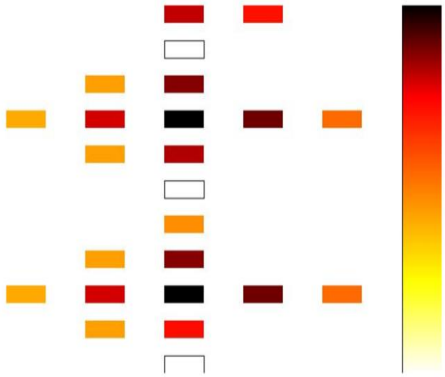
"According, to the upper bound power dissipation model [36], the power dissipation of a QCA cell is calculated as:"

$$P_{diss} = \frac{E\ diss}{Tcc} < \frac{\hbar}{2Tcc}\vec{\Gamma}^{+} x\left\{ -\hat{\Gamma}^{+}\tanh\left(\hbar\frac{|\Gamma+|}{KBT}\right) + \Gamma^{-}\tanh\left(\hbar\frac{|\Gamma-|}{KBT}\right)\right\} > \quad (11)$$

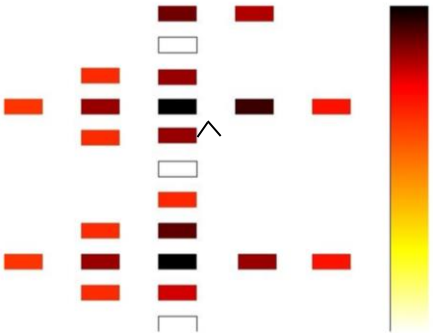
"Here, T is the temperature and k_B denotes the Boltzmann constant and Γ represents Hamiltonian normalised vector. The total dissipated energy ('leakage' and 'switching') of all equivalent QCA cells can be determined using the above equation. The power dissipation map of the proposed converters are produced at T=2 K for tunneling energy levels of $0.5E_k$, 1 E_k and 1.5 E_k as shown in Fig 16,17 ,18,19, 20 & 21 respectively".



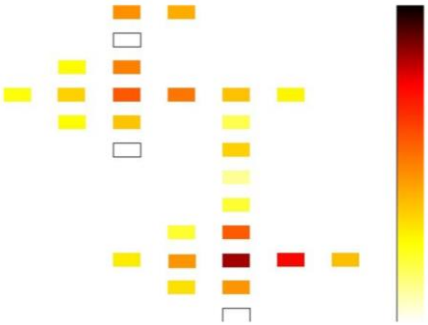
"Fig 16: Power dissipation map of the proposed Binary to Gray code converter at T = 2 K temperature and $0.5E_k$ tunneling energy level"



"Fig 17: Power dissipation map of the proposed Binary to Gray code converter at T = 2 K temperature and $1E_k$ tunneling energy level"



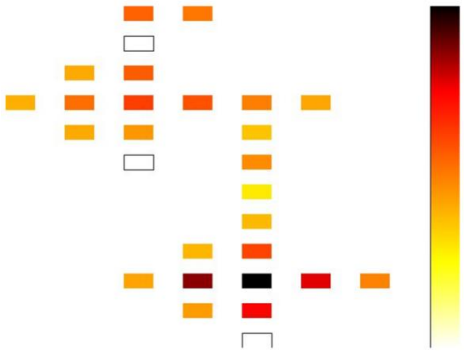
"Fig 18: Power dissipation map of the proposed Binary to Gray code converter at T = 2 K temperature and $1.5E_k$ tunneling energy level"



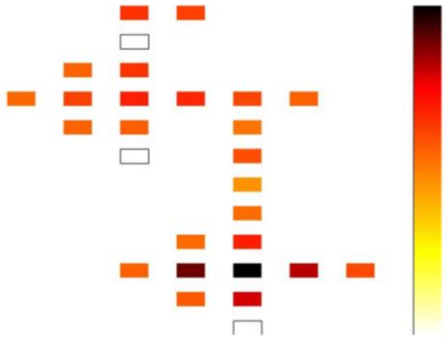
"Fig 19: Power dissipation map of the proposed Gray to Binary code converter at T = 2 K temperature and $0.5E_k$ tunneling energy level"

ISSN (Online) 2394-6849

International Journal of Engineering Research in Computer Science and Engineering (IJERCSE)
Vol 8, Issue 6, June 2021



"Fig 20: Power dissipation map of the proposed Gray to Binary code converter at T = 2 K temperature and $1E_k$ tunneling energy level"



"Fig 21: Power dissipation map of the proposed Gray to Binary code converter at T = 2 K temperature and $1.5E_k$ tunneling energy level"

Table3:Power dissipiation analysis of proposed design.

Proposed design	Depletion energy at T=2K					
	Average leakage energy dissipiation (eV)			Average switching energy dissipiation (eV)		
	γ=0.5E_K	γ= 1 E_K	γ= 1.5 E_K	γ=0.5E_K	γ= 1 E_K	γ= 1.5 E_K
Binary to Gray code converter	0.00786	0.02196	0.03773	0.02143	0.01767	0.01465
Gray to Binary code converter	0.00986	0.02666	0.04534	0.02745	0.02327	0.01971

"It is observed from the power dissipation maps that as the tunneling energy is increased from 0.5Ek to 1.5Ek, the average switching energy dissipation of the gate and adder decreases whereas the average leakage energy dissipation increases thereby resulting in the increase in the total energy consumption. The darker cells in the power dissipation maps indicate that the cell is dissipating high energy. On the other hand, input cells do no dissipate any power and hence are depicted in white (~zero power)".

Conclusion

"In this article, we proposed a new reversible Binary to Gray and Gray to Binary code converter using FG in the QCA architecture. The design and simulation of a QCA Binary to Gray and vice versa code converter circuits has been presented. The operation of these converters has been analyzed using QCA simulation designer. This" QCA based design approach opens a wider path for digital circuit designs with microscopic dimensions. Power-efficient circuits can be constructed with more precision which ultimately increase the lifetime and speed of the circuit using this technique. "The proposed circuits have been found to be more effective in terms of cell size, total area, latency, complexity, use minimum clock phases and have significantly less number of cells and minimum wire length which causes to trouble-free operation at higher temperature."In addition to this energy dissipation analysis for different scenarios is also done on all the designs using QCA Pro tool and it is observed that the proposed designs dissipate minimum energy thereby making them suitable for ultra-low power designs. These encoder circuits using reversible logic gates can be further explored for the designing of other low power loss devices. We believe that the present research work will be of great interest to the future computations".

REFERENCES

[1] G. E. Moore, "Cramming more Components onto Integrated Circuits, Electronics," 38, 1965.
[2]"International Technology Roadmap for Semiconductors." [Online].Available:http://www.itrs.net/links/2010itrs/2010Update/ToPost/2010_Update_Overview.pdf.[Accessed: 08-May-2011].
[3] H. Iwai, "CMOS Technology after Reaching the Scale Limit," *Junction Technology*, IEEE, Shanghai, pp. 1-2, May 2008.
[4] C. S. Lent, P. D. Tougaw, W. Porod, and G. H. Bernstein, "Quantum Cellular Automata," *Nanotechnology*, Vol. 4, No. 1, pp. 49- 57, 1993.
[5] C. S. Lent, G. L. Snider, G. H. Bernstein, W.

Porod,, A. Orlov, M. Lieberman, T. Fehlner, M. Niemier, P. Kogge, Quantum-dot cellular automata. In Electron Transport in Quantum Dots, 397-431, 2003, Springer, Boston, MA.
[6] "International technology roadmap for semiconductors", 2001, Semiconductor Industries Association, San Jose, CA, http //public itrs net.
[7] R. Zhang, K. Walus, W. Wang, and G. A. Jullien, "A method of majority logic reduction for quantum cellular automata", IEEE Trans.Nano. 3, 443, 2004.
[8] P. D. Tougaw and C. S. Lent, "Logical Devices Implemented Using Quantum Cellular Automata," Journal of Applied Physics, 75, 1818, 1994.
[9] K. Kim, K. Wu, R. Karri, "Quantum-dot cellular automata design guideline", IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences 89, 1607, 2006.
[10] K. Walus, T. Dysart, G. Jullien, and R. Budiman, "QCA Designer: A rapid design and simulation tool for QCA", IEEE Trans. Nanotechnol. 3, 26, 2004.
[11] A. M. Pintus, Gabrieli A., Pazzona F., Pireddu G., Demontis P., "Molecular QCA embedding in micro porous materials", Phys. Chem. Chem. Phys. 21, 7879, 2019.

[12]. K. Kim, K. Wu and R. Karri, "The Robust QCA Adder Designs using Composable QCA Building Blocks," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol.26, pp. 176-183, 2007.
[13] I. Amlani, A. O. Orlov, G. Toth, G. H. Bernstein, C. S. Lent and G. L Snider, "Digital logic gate using quantum-dot cellular automata", Science, vol. 284, no. 5412, **(1999)**, pp. 289-291.
[14] S. Erniyazov, J. C. Jeon, "Carry save adder and carry look ahead adder using inverter chain based coplanar QCA full adder for low energy dissipation", Microelectronic Engineering. 211, 37, 2019.
[15] Fijany A., Toomarian B. N., New design for quantum dots cellular automata to obtain fault tolerant logic gates. Journal of nanoparticle Research. 3, 27-37, 2001.
[16] Balakrishnan L, Godhavari T, Kesavan S. Effective design of logic gates and circuit using quantum cellular automata (QCA). In 2015 International Conference on Advances in Computing, Communications and Informatics (ICACCI) 2015 Aug 10 (pp. 457-462). IEEE.
[17] M. Goswami, A. Mondal, M. H. Mahalat, B. Sen, B. K. Sikdar, "An efficient clocking scheme for quantum-dot cellular automata", International Journal of Electronics Letters. 6, 1, 2019.
[18] E. Blair, C. Lent, "Clock Topologies for Molecular Quantum-Dot Cellular Automata", Journal of Low Power Electronics and Applications". 8, 31, 2018.
[19] V. Pudi and K. Sridharan, "Low Complexity Design of Ripple Carry and Brent–Kung Adders in QCA," IEEE Transaction on Nanotech., vol. 11, no. 1,pp. 105-119, Jan 2012. [20] R. Feynman, "Quantum Mechanical Computers," Optics News, vol.11, pp. 11–20, 1985.
[21] L. T. Lee, J. Foster, "Gray Code Design for N-Dimensional Signal Sets Using Genetic Algorithm & Binary Search Techniques", Proceedings Of The IEEE Conference, pp. 606, 1992.
[22] K. Takizawa and M. Okada, "High-speed Gray-Binary and Binary-Gray code convertors using electro-optic light modulators," Electronics Letters 14, 708, 1978.
[23] P. Biswas, N. Gupta, N. Patidar, "Basic Reversible Logic Gates and It's QCA Implementation", International Journal of Engineering Research and Applications, vol. 4, no. 6, pp.12-16, 2014.
[24] J. C. Das and D. De, "Reversible Binary to Grey and Grey to Binary Code Converter using QCA" IETE Journal of Research, vol. 61, no. 3, pp. 223–229, May 2015, DOI: https://doi.org/10.1080/03772063.2015.1018845.
[25] M. Abdullah-Al-Shafi, M. Shifatul, and A. N. Bahar, "A Review on Reversible Logic Gates and its QCA Implementation," International Journal of Computer Applications, vol. 128, no. 2, pp. 27–34, Oct. 2015.
[26] J. C. Das and D. De, "Quantum-dot cellular automata based reversible low power parity generator and parity checker design for nanocommunication," Frontiers InfTechnol Electronic Eng, vol. 17, no. 3, pp. 224–236, Mar. 2016.
[27] A. N. Bahar, S. Waheed, and M. A. Habib, "A novel presentation of reversible logic gate in Quantum-dot Cellular Automata (QCA)," in2014 International Conference on Electrical Engineering and

Information Communication Technology (ICEEICT), 2014, pp. 1–6.

[28] Ehsan Taher Karkaj Saeed Rasouli Heikalabad, "A new efficient reversible binary to gray and gray to binary converter in quantum-dot cellular automata" International Journal for Light and Electron Optics http://dx.doi.org/10.1016/j.ijleo.2016.11.087
[29] J. I. Reshi, M. T. Banday, "Efficient Design of Reversible Code Converters Using Quantum Dot Cellular Automata", Journal of Nano- And Electronic Physics 8, 02042, 2017.
[30] Ali H. Majeed *Kufa University, Najaf, Iraq.* A Novel Design "Binary to Gray Converter" with QCA Nanotechnology International Journal of Advance Engineering and Research Development e- ISSN (O): 2348-4470 p-ISSN (P): 2348-6406
[31] Gassoumi, L. Touil and B. Ouni Design of Reversible Binary-to-Gray Code Converter in Quantum-Dot Cellular Automata© Springer Nature Singapore Pte Ltd. 2020 Lecture Notes in Electrical Engineering 577 , https://doi.org/10.1007/978-981-13-8821-7_14

[32] J. C. Das and D. De, "Reversible Binary to Grey and Grey to Binary Code Converter using QCA," *IETE Journal of Research*, vol. 61, no. 3, pp. 223–229, May 2017.
[33] Ehsan Taher Karkaj Saeed Rasouli Heikalabad, "A new efficient reversible binary to gray and gray to binary converter in quantum-dot cellular automata" International Journal for Light and Electron Optics http://dx.doi.org/10.1016/j.ijleo.2016.11.087
[34] P.D. Tougaw, C.S. Lent, Dynamic behavior of quantum cellular automata, J. Appl. Phys. 80 (1996) 4722–4736.
[35] Timler, J., Lent, C.S.: Power gain and dissipation in quantum-dot cellular automata. J. Appl. Phys. 91, 823–831 (2002)
[36]Sen, B., Saran, D., Saha, M., Sikdar, B.K.: Synthesis of reversible universal logic around QCA with online testability. In: 2011 International Symposium on Electronic System Design, pp. 236–241 (2011)