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Implementation Of Low Power Dynamic Logic CMOS Circuits

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***Abstract*— Today in Very Large Scale Integration (VLSI) technology several applications require high speed operation. To achieve this dual output dynamic logic using Source Coupled Logic (SCL) topology was designed and it provides high speed operation with area and power over head. In order to reduce the power in dual output dynamic logic with optimizable speed of operation half swing is introduced. With the help of half swing without altering the operation of the logic function power is reduced. The half swing technique is applied to clock as well as input level. The existing system NMOS (N- type Metal Oxide Semiconductor) differential tree logic is applied to NAND, NOR, Exclusive -NOR (EX-NOR), half adder, and full adder. Due to the usage of NMOS differential tree logic this circuit gives true and complementary outputs. The power dissipation of NMOS differential tree logic is 80% greater than Complementary Metal Oxide Semiconductor (CMOS). Compared to the existing system the power dissipation is reduced by 46% in the proposed half swing. The delay achieved with existing system is 0.2 ns. The delay in the proposed system increases by 33% which is less compared to power dissipation reduction that is achieved. Advantages of dual output dynamic logic circuit is it increases the speed, avoids noise, no charge sharing problem, no short circuit power dissipation and it eliminates monotonicity problem.**

***Index Terms*— Dual output dynamic logic, SCL, NMOS differential tree, Half swing**

I. INTRODUCTION

Among many logic circuit design techniques, CMOS is widely used because of high noise margin and ease of implementation. The conventional static CMOS circuits are intrinsically slow, because each gate must drive both NMOS and PMOS (P-type Metal Oxide Semiconductor) transistors. When the input is high, NMOS transistor will conduct, when the input is low, PMOS transistor will conduct [4]. Domino logic circuits drive only NMOS transistors and thus have the advantage of faster operation and smaller area compared to conventional CMOS circuits. Domino logic circuits have been widely used for high-performance microprocessors and other logic chips. However, their drawbacks include the non-inverting nature, strict timing constraints and charge sharing problems. Several dynamic logic circuits have been proposed for practical applications. Dynamic logic families offer more advantages than the traditional CMOS logic [7].

The main problem with dynamic circuit is its low susceptibility to noise. Dual output dynamic logic using SCL topology was proposed to overcome the noise problem in dynamic logic. It also has the following additional advantages like,

1. Increased speed
2. Low noise due to differential nature
3. No short circuit power dissipation
4. No charge sharing problem
5. No monotonicity problem
6. Dual output (True and complementary outputs)

The drawback of existing system is that it consumes more power. To overcome the drawback three techniques have been proposed. The three techniques are: i) clock half swing ii) input half swing iii) clock and input half swing. In each technique considerable amount of power is reduced maintaining the same area.

II. DIFFERENTIAL NMOS TREE REALIZATION

In Integrated Circuit (IC) design, dynamic logic is a design methodology in combinational logic circuits, particularly those implemented in MOS technology. It is distinguished from the static logic by exploiting temporary storage of information in stray and gate capacitances. Dynamic logic circuits are usually faster than static counterparts, and require less surface area, but are more difficult to design. Dynamic logic is distinguished from static logic in that dynamic logic uses a clock signal in its implementation of combinational logic circuits. The usual use of a clock signal is to synchronize transitions in circuits. For most implementations of combinational logic, a clock signal is not needed. Source coupled logic used in ultra - low power applications [9].

The dynamic logic circuit requires two phases. The first phase, when clock is low, is called the setup phase or the precharge phase and the second phase, when clock is high, is called the evaluation phase. In the setup phase, the output is driven high unconditionally (no matter the values of the inputs). The capacitor, which represents the load

capacitance of this gate, becomes charged. During the evaluation phase, clock is high. The output will be pulled low or high according to the input. Dynamic logic has a few potential problems that static logic does not. For example, if the clock speed is too slow, the output will decay too quickly to be of use. Also, the output is only valid for part of each clock cycle, so the device connected to it must sample it synchronously during the time that it is valid. Dual output dynamic logic consider the two main techniques are: (1) using keeper, (2) precharging internal nodes [8]. Keeper circuit improve the noise immunity of dynamic CMOS logic gates [7]. When all nodes are precharged, able to eliminate the charge sharing problem [3].

The NMOS block used in dynamic logic is based on static CMOS type realization. For which, a new type of realization is used for Boolean function, with which dual output can be obtained. This type of realization is used for SCL based logic gates design. There are several ways of realizing NMOS tree 222network. The most useful is Variable Entered Mapping (VEM) method. SCL topology avoids tedious simulation iterations [1].

It is an efficient manual method for obtaining the most compact form of the subsumptive general solution of a system of Boolean equations. It is an effective combination of mapping and algebraic methods and employs a minimum number of constructions. In addition to being highly economic, the present method is not restricted to two valued Boolean equations and is naturally suitable for big Boolean algebras. This method can be utilized in various application areas of Boolean equations. In particular, an automated version of the present Boolean equations solver can be applied in the simulation of gate level logic. The ideas expressed can also be incorporated in the automated solution of large system of Boolean equations. They can also be extended to handle quadratic Boolean equations, Boolean ring equations and Boolean differential equations.

This technique reduces the input decision tree which gives minimized logic expression for all possible ordering of input variable. It is recommended to choose the realization which gives equal number of branches on the two output (i.e., normal and complementary) terminals. For example, the NMOS tree realization of Boolean function f (A, B) = A.B as shown in Fig. 1.

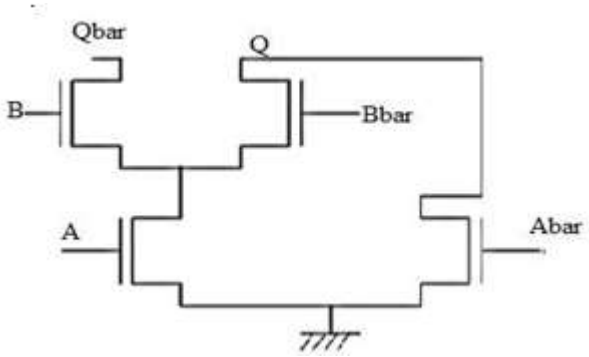

Fig. 1. Differential tree realization of NAND gate

Dual output dynamic logic AND/NAND circuit consists of basic dynamic logic structure with NMOS differential tree and two cross coupled keepers provides dynamic operation. Based on the two cross coupled connections it can operate in two phase.

1. Precharge phase
2. Evaluation phase

During precharge phase the clock signal is always LOW. Therefore both outputs Q and Qbar are always connected to V_{dd} irrespective of the inputs, because there is no path exists between V_{dd} and ground. Since the clock is LOW, the NMOS transistor of the dynamic logic resides in high impedance state.

During evaluation phase the clock signal is HIGH. Therefore the PMOS transistors of dynamic logic turn OFF. The output depends on logical inputs given to the circuits.

Dual output dynamic logic has many advantages like increased speed and avoids noise. The additional advantages are there is no charge sharing problem, no short circuit power dissipation. It also eliminates the monotonicity problem. But due to the usage of NMOS differential tree concept, the number of transistor increases. This in turn increases the area and power. So to reduce the power, half swing technique is introduced.

III. HALF SWING TECHNIQUE

Reducing power consumption without sacrificing processing speed is a critical factor in VLSI design, especially for hand-held devices. In CMOS circuits, dynamic power consumption is proportional to the transition frequency, capacitance and square of supply voltage that is $P = CV^2$. Consequentially, reducing supply voltage provides significant power savings at the expense of speed. This technique employs high performance architectures to achieve the specified speed and is quite effective for Application Specific Integrated Circuits (ASIC). In general purpose processors, however, it is more difficult to employ high performance architectures, because the architecture is already a part of the specifications. It is therefore very important to reduce power consumption without reducing

supply voltage or sacrificing performance.

The drawback of dual output dynamic logic is overcome by the half swing technique. The NMOS and PMOS transistor turns ON when the gate voltage is greater than the threshold voltage. For example if the threshold voltage of NMOS is 0.8 V the transistor starts conduction if the gate voltage is greater than 1V. But 5 V is given to make it ON. So the power consumption increases. To reduce the power the input voltage swing is made half that is instead of 0 V to 5 V, 0 V to 2.5 V is given.

If the swing of the N-transistor input signal is limited from 0 to 2.5 V (half swing) the on-off characteristics of all N-transistors remain digitally identical. Similar observation can be made for clock signal. The input signal feeding p-transistor where the swing limited from 2.5 V to 5 V. The power can be reduced by the following three half swing techniques. They are,

1. Clock half swing
2. Input half swing
3. Clock and input half swing

A. *Clock half swing*

The half swing clock is especially attractive in the two phase non overlapping clocking design where a sequential element requires two out-of-phase clock signals. The power saved from the reduced swing is 75% on the clock signal. The penalty incurred is the reduced speed of sequential element. In general the sequential delay is expressed in terms of propagation delay and setup/hold time delay. This is due to the on resistance of a transistor is inversely proportional to the voltage difference between its gate and source and the reduced clock swing increases the on-resistance of transistors. The clock swing of 5 V is reduced to half that is to 2.5 V and it is shown in Fig. 2.

Fig. 2 Clock half swing

Dual output dynamic logic NOR/OR gate using half swing is shown in Fig. 3.

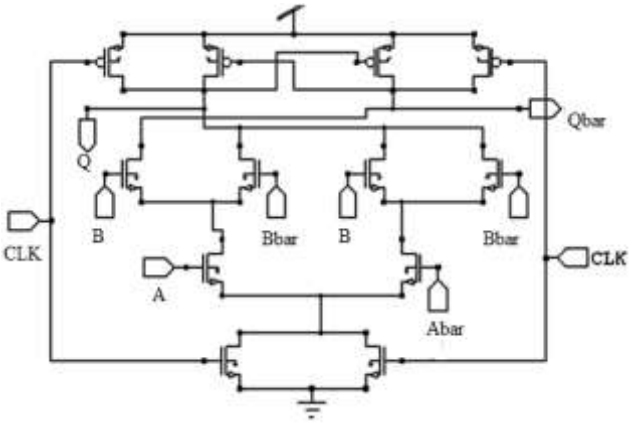

Fig. 3. Dual output dynamic logic NAND/AND gate using half swing

B. *Input half swing*

The input half swing reduces the power around 46%. In this technique input swing is kept from 0 V to 2.5 V instead of 0 V to 5 V. The N-transistor will turn on if the input signal is above 1 V, but in digital CMOS chip 5 V is applied to make the transistor ON. This increases the power dissipation. So to reduce the power, input voltage is made half swing. When compared to clock half swing the input half swing reduces the power more because the clock controls only two PMOS transistor while the dual output dynamic logic consists of many NMOS so more power is reduced. The input swing of 5 V is reduced to half that is 2.5 V and it is shown in the Fig. 4.

Fig. 4. Input half swing

Dual output dynamic logic NOR/OR gate using half swing is shown in Fig. 5.

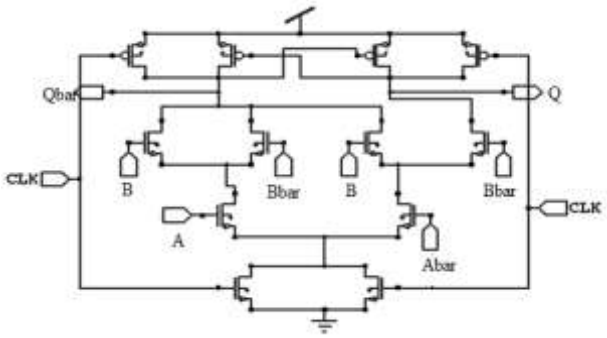

Fig. 5. Dual output dynamic logic NOR/OR gate using half swing

C. *Input and clock half swing*

The input and clock voltage is made half swing to reduce the power. The clock and input half swing is shown in Fig. 6.

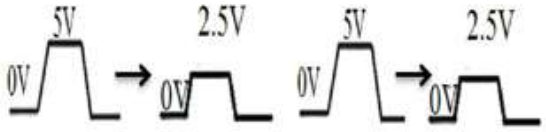

Fig. 6. Input and clock half swing

Dual output dynamic logic EXNOR/EXOR gate using half swing is shown in Fig. 6

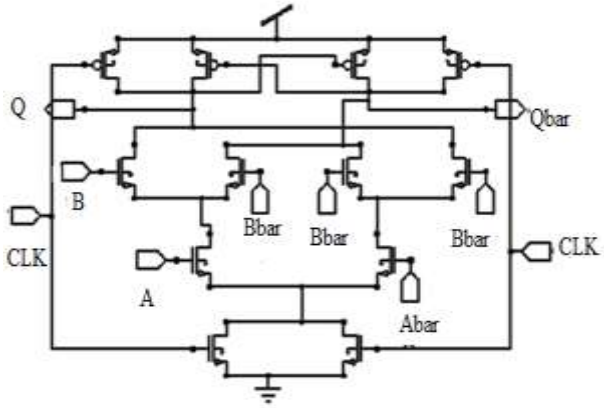

Fig. 6. Dual output dynamic logic EXNOR/EXOR gate using half swing

IV. HALF ADDER

Adder circuit can be implemented using EX-OR, AND gates. While compared to conventional CMOS technique the speed increases in this technique with optimized power and area. The half adder sum using half swing is shown in the Fig. 7.

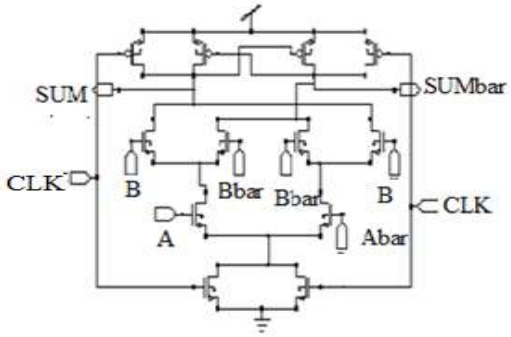

Fig. 7 Dual output dynamic logic half adder sum using half swing

The half adder carry using half swing is shown in the Fig. 8

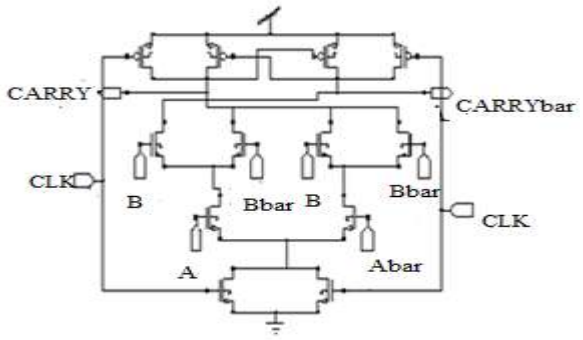

Fig. 8. Dual output dynamic logic half adder carry using half swing

V. FULL ADDER

A half adder has only two inputs and there is no provision to add a carry coming from the lower order bits when multi bit addition is performed. For this purpose a full adder is designed. A full adder is a combinational circuit that performs the arithmetic sum of three inputs (both in true form and in complement form) and the two outputs sum and carry (both also in true form and in complement form). The full adder sum using half swing is shown in the Fig. 9.

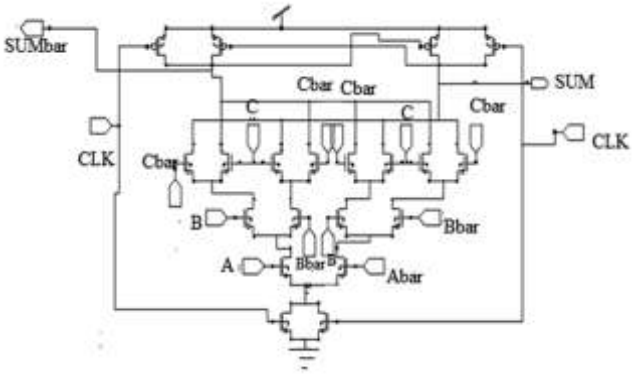

Fig. 9. Dual output dynamic logic full adder sum using half swing

VI. SIMULATION RESULTS

The simulation is performed in Tanner EDA at 250 nm technology. The operating temperature was maintained at 25ºC.The output of NAND gate using clock half swing is shown in Fig. 11.

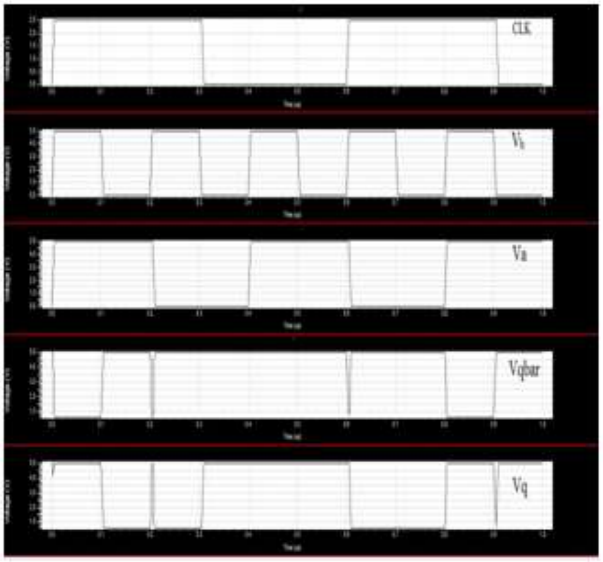

Fig. 11. Output of NAND gate using clock half swing

The clock half swing technique for NAND/AND gate provides the output waveform with the delay of 0.24 ns and the power consumption is 1.08 mW.

Fig. 12. Output of NOR gate using input half swing

The input half swing technique for NOR/OR gate provides the output waveform with the delay of 0.305 ns and the power consumption is 0.684 mW

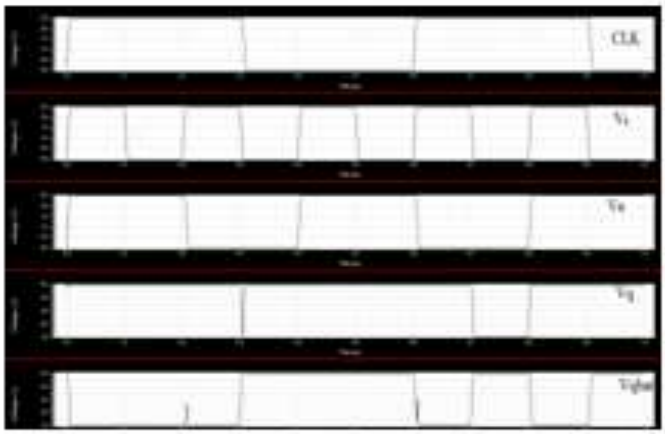

Fig. 13. Output of NOR gate using input and clock half swing

The clock and input half swing technique for NOR/OR gate provides the output waveform with the delay of 0.32 ns and the power consumption is 0.632 mW.

Fig 14. Half adder using clock half swing

Fig 15. Full adder using clock and input half swing

The clock and input half swing technique for full adder provides the output waveform with the delay of 0.9 ns and the power consumption is 1.37 mW

TABLE I
Performance analysis of NMOS differential tree logic with other half swing techniques

Logic Type	NMOS Differential Tree Logic		Clock Half Swing		Input Half Swing		Clock and Input Half Swing	
	Power (mW)	Delay (ns)	Power (mW)	Delay (ns)	Power (mW)	Delay (ns)	Power (mW)	Delay (ns)
NAND	1.33	0.21	1.08	0.24	0.72	0.312	0.6784	0.325
AND	1.33	0.21	1.08	0.24	0.72	0.312	0.6784	0.325
NOR	0.99	0.206	0.73	0.241	0.68	0.305	0.632	0.32
OR	0.99	0.206	0.73	0.241	0.68	0.305	0.632	0.32
EX-NOR	1.36	0.210	1.24	0.23	0.72	0.314	0.684	0.331
EX-OR	1.36	0.210	1.24	0.23	0.72	0.314	0.684	0.331
HALF ADDER	1.77	0.24	1.57	0.262	1.21	0.320	1.105	0.34
FULL ADDER	2.84	0.5	2.18	0.64	1.49	0.75	1.37	0.9

VII. CONCLUSION

Dual output dynamic logic gives two outputs (true and complementary outputs) which is required for both combinational and sequential circuits. Dual output dynamic logic is more suitable for implementing flip-flops and latches The logic gates such as AND/NAND gate, OR/NOR gate, EX-OR/EX-NOR gate and adders are half adder and full adder uses dual output dynamic logic concept. This logic avoids the short circuit power dissipation and eliminates the noise and monotonicity problems. Dual output dynamic logic reduces the delay in circuit but increases the power and area. This increase in power is reduced by half swing technique. Thus this technique reduces the power than dual output dynamic logic with full swing. Future work involves reduction of area in this circuit.

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