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Design of Shift Register Based on Multi bit Flip Flop for Universal Asynchronous Receiver and Transmitter

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Abstract: **In this paper I propose the design and implementation of first in first out shift register based on multi bit flip flop for universal asynchronous receiver and transmitter (UART).UART is a major communication component to interface the microcontroller with the external modules like GSM, GPS etc. One of the problems in embedded systems is the time consuming by the external devices to communicate with the controlling device. Here we are concentrating mainly on fast communication among the devices in embedded applications. Simulation results have been shown that the proposed system is 50% faster than the existing system. Code is written in VHDL and modeled in Xilinx 10.1 ISE, implemented with FPGA Spartan 3E hardware tool.**

Index Terms— **UART, MultiBit flipflop, FIFO, Shift Register, Single bit flip flop**

I. INTRODUCTION

This paper portrays a novel architecture of Universal Asynchronous Receiver Transmitter. UARTs are used for asynchronous serial data communication between remote embedded systems. The UART is for interfacing computers or microprocessors to an asynchronous serial data channel. The receiver converts serial start, data, parity and stop bits. The transmitter converts parallel data into serial form and automatically adds start, parity and stop bits. The data word length can be 5, 6, 7 or 8 bits. Parity may be odd or even. Parity checking and generation can be inhibited. The stop bits may be one or two or one and one-half when transmitting 5-bit code.

The Universal Asynchronous Receiver Transmitter (UART) is a popular and widely-used device for data communication in the fields of telecommunication, embedded systems. There are different versions of UARTs in the industry. Some of them contain FIFOs for the receiver/transmitter data buffering and some of them have the 9 Data bits mode (Start bit + 9 Data bits + Parity + Stop bits). This application note describes a fully configurable UART optimized for and implemented in a variety of Lattice devices, which have superior performance and architecture compared to existing semiconductor ASSPs (application-specific standard products).

This UART reference design contains a receiver and a transmitter. The receiver performs serial-to-parallel conversion on the asynchronous data frame received from the serial data input SIN. The transmitter performs parallel-to- serial conversion onthe 8-bit data received from the CPU. In order to synchronize the asynchronous serial data and to insure the data integrity, Start, Parity and Stop bits are added to the serial data. An example of the UART is shown in Figure 1 below.

The UART can be used in a wide range of applications including modems, printers, peripherals and remote data acquisition systems. Utilizing the Intersil advanced scaled SAJI IV CMOS process permits operation clock frequencies up to 8.0MHz (500K Baud). Power requirements, by comparison, are reduced from 300mW to 10mW. Status logic increases flexibility and simplifies the user interface [1].

The UART protocol [7] is a serial communicationprotocol that takes bytes of data and transmits theindividual bits in a sequential fashion. At the destination, asecond UART re-assembles the bits into complete bytes.The UART usually does not directly generate or receivethe external signals used between different items ofequipment. Separate interface devices are used to convertthe logic level signals of the UART to and from theexternal signaling levels. External signals may be of manydifferent forms. Examples of standards for voltagesignaling are RS-232, RS-422 and RS-485 from the EIA.Typically its a 3-line (transmit, receive, ground)communication. Communication which enables it to be“full duplex” (both send and receive at the same time) or“half duplex” (devices take turns transmitting andreceiving) [1].

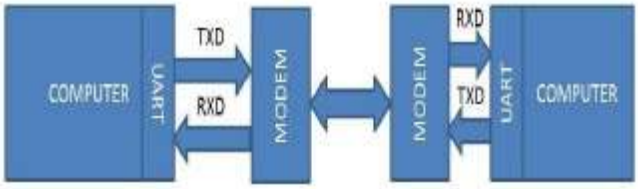


Fig. 1. UART diagram

I. PROPOSED SYSTEM

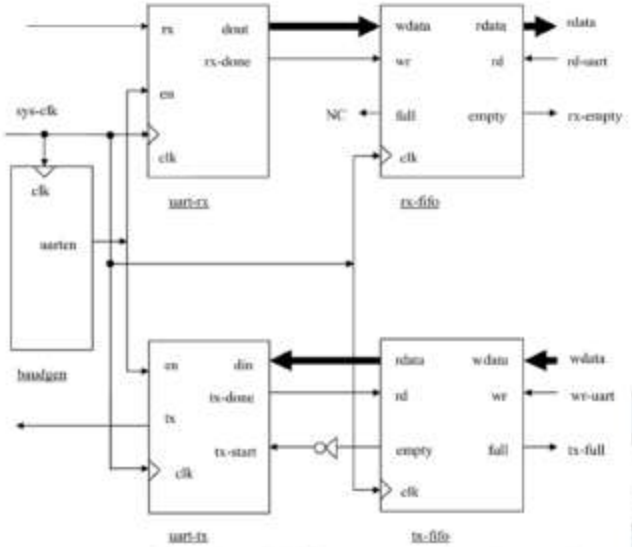


Fig. 2. UART module

The UART module that have been designedtaken from [2] consists of five parts namely (i) “uart-rx”, which takes inthe serial data (as a frame) coming through the ‘rx’ line,retrieves the actual data and converts to parallel form(usually as a byte). (ii) “uart-tx”, which does the oppositefunction of the “uart-rx” module and transmits the framethrough the ‘tx’ line. (iii) “baudgen”, which generates aclock which occurs 16-times(the default over-samplingrate)in one bit-time period. (iv) “tx-fifo”, which storestemporarily the bytes (that usually comes from a fasterprocessor) to send, as the sending process takes sometime. (v) “rx-fifo”, which is the replica of the “tx-fifo” module used to store the received bytes temporarily suchthat the processor may read them at its own pace.The UART-top-module (fig.2) has (i) two data bus(wr-data and rd-data) for data in or out in parallel formfrom or to the processor it is used with. (ii) Two lines(‘tx’ and ‘rx’) through which data comes-in or goes-outserially bit-by-bit from or to the device it iscommunicating. (iii) Four lines (rd-uart, wr-uart, tr-full,rx-empty) are used for handshaking purpose with theprocessor it is used with. (iv) One `system-clk' signal thatcontrols all the activities[2].

II. MULTI BIT FLIP FLOP

Generally for the storage of bits the memory elements are latches and flip flops. The flip flop casually stores a single bit value. Here in our proposed system the flip flop stores the multi bits. Finally we designed a shift register by using the multi bit two flip flops which shifts the four bits. The diagram for the shift register is shown in the figure 2. The multi bit flip flop works under the technique of merging the clock pulses [3]. The timing diagram for multi bit flip flop is shown in figure 3 which is having the same operation as single bit flip flop. D-flip flop latches all the inputs to the output when the clock is high (for active high), or when clock is low (for active low). In an inactive state for both the cases the input holds the data. The proposed shift register is used for the shifting of bits according to the Universal Asynchronous receiver and transmitter[4-6].

Fig. 4. Timing diagram for multi bit flip flop

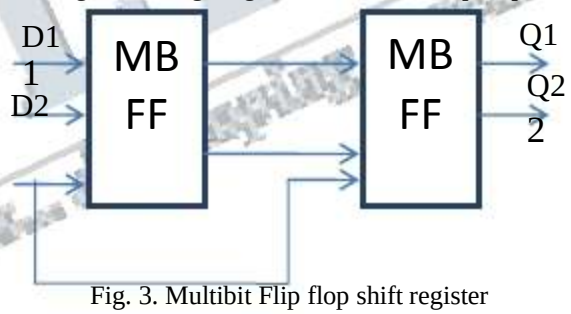


Fig. 3. Multibit Flip flop shift register

III. RESULTS

The proposed system is modeled with Xilinx ISE10.1 version. The Register Transfer Level have been shown in the figure 7. The timing results of figure 4 and figure 5 of single bit flip flop and multi bit flip flop simultaneously. Table I shows the differences of the timing between proposed system and existing system. Figure 8 shows the waveforms generated in the model sim. Code is written in VHDL (Very High Speed Integrated Circuit Hardware Description Language).

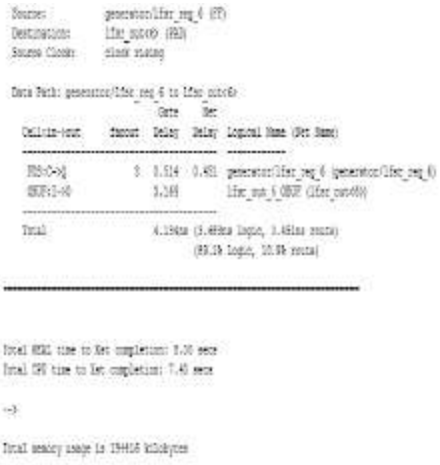


Fig. 5. Timing details of single bit flip flop

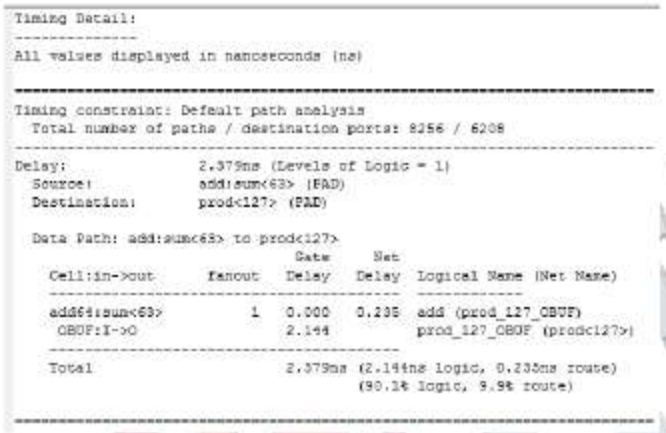
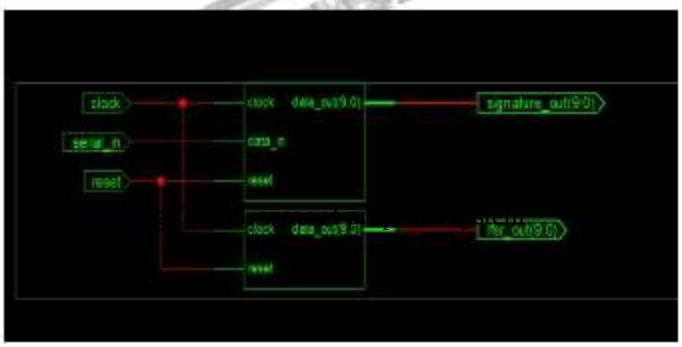


Fig. 6. Timing details on multi bit flip flop

TABLE I. TIMING TABLE

	SBFF	MBFF
TIME (ns)	4.134ns	2.379ns



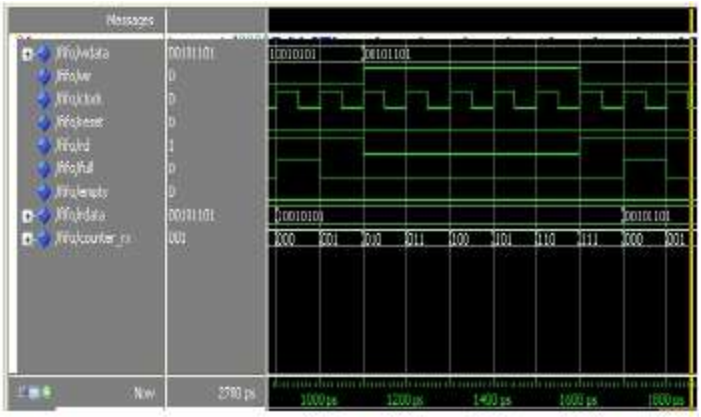


Fig. 8. Wave forms of proposed system

IV. CONCLUSION

I have designed our UART module with multi bit flip shift register in generic formwhich is operating fine with no underrun error and can becustomized to make it free from overrun error with thecapability provided and so can be made available.The results have shown that the time has decreased approximately 50%.

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