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Digital PLL as Frequency Synthesizer

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Abstract: **— The paper describes a digital PLL circuit design as frequency synthesizer and its implementation using MULTISIM, to meet the increasing needs of high speed operation. It includes a Phase-Frequency Detector, a Loop filter, a Voltage Controlled Oscillator and a Divide by N Counter. The main aim is to decrease the power dissipation as compared with the conventional PLL. It ensures better stability, a shorter locking time and as a result, high accuracy as well as a lower sensitivity to power supply variations.**

Keywords: **phase frequency detection, filtering, voltage controlled oscillation, low power dissipation.**

I.INTRODUCTION

Phase locked loop is closed loop feedback control system that compares the output phase with the input phase. Digital systems use clocks to sequence operations and synchronize between functional units and between ics. Clock frequencies and data rates are increasing with each generation of processing technology and processor architecture. In the digital systems, well-timed clocks are generated with phase-locked loops (plls).
A PLL sets fixed phase relationship between its output clock phase and the phase of a reference clock. It tracks the phase changes that are within the bandwidth of the pll [1].

A PLL also multiplies a low-frequency reference clock *ckref*, to produce a high-frequency clock *ckout.* The overall goal of the pll is to match the reference and feedback signals in phase, this is the lock mode [3]. After this, the pll continues to compare the two signals but since they are in lock mode, pll output is constant.

PLL consists of four main blocks:
1. Phase detector or phase frequency detector (pd or pfd)
2. Low pass filter (lpf)
3. Voltage controlled oscillator (vco)
4. Divide by 'n' counter

The phase frequency detector (comparator) produces an error output signal based on the phase difference between the phase of the feedback clock and the phase of the reference clock. Over time, small frequency differences accumulate as an increasing phase error [2]. If there is a phase difference between the two signals, it generates 'up' or 'down' synchronized signals to the low pass filter.

If the error signal from the pfd is an 'up' signal, then the capacitor of the lpf charges which increases the control voltage *v* control [2] . On the contrary, if the error signal from the pfd is a 'down' signal, then the capacitor of the lpf discharges, which decreases *v* control. *V* control is the input to the vco. Thus, the lpf is necessary to allow only dc signals into the vco. The purpose of the vco is to either speed up or slow down the feedback signal according to the error generated by the pfd. If the pfd generates an 'up' signal, the vco speeds up. On the contrary, if a 'down' signal is generated, the vco slows down. The frequency of oscillation is divided down to the feedback clock by a frequency divider. When the feedback clock has a constant phase error and the same frequency as the reference clock, the phase is locked. Since the feedback clock is a divided version of the oscillator's clock frequency, the frequency of oscillation is n times the reference clock.

II. THE PROPOSED METHOD

The phase frequency detector generates the error signal corresponding to the difference between phase or frequency of the reference input and the feedback output. The pfd has two outputs. The output is directly connected to the loop filter. The function of the loop filter is to filter out the high frequency components from the pfd output. The voltage controlled oscillator accepts the control voltage from the loop filter and generates the oscillating output. The vco output is feedback to the input through a

divide by counter. The process is continued until both the input signals are synchronized or locked.

A. Cmos pfd using pass transistor logic

in this we introduce a new cmos pfd with low glitch. The low glitch is achieved by using a pass transistor and gate instead of logical gate. Pass transistor logic (ptl) describes several logic families used in the design of integrated circuits. It will reduce the count of transistors used to make different logic gates, by eliminating redundant transistors. It increases

The speed of the pll by reducing the gate delay, with a slight increase in power dissipation[3]. Since normal and inverted outputs are available in the d flip-flop, effectively only two extra transistors are required for implementing 'and' gate using pass transistor logic [5].

B. Switched capacitor resistor

The loop filter is the center of pll. If the loop filter values are not selected correctly, it will take the loop too long to lock. When it is once locked small variations in the input data may cause the loop to unlock. In order to stabilize the system, we must modify the phase characteristics by adding a resistor in series with the loop filter capacitor. A switched capacitor is an electronic circuit element used for discrete time signal processing. It moves charges into and out of capacitors when switches are opened and closed [2]. Filters implemented with these elements are termed 'switched – capacitor filters' and depend only on the ratios between capacitances [4]. This makes them much more suitable for use within integrated circuits, in which accurately specified resistors and capacitors are not economical to construct. The simplest switched capacitor (sc) circuit is the switched capacitor resistor, made of one capacitor and two switches which connect the capacitor with a given frequency alternately to the input and output of the sc. The use of switched capacitor resistors reduces the area and also enables direct integration.

C. Low power consumption in vco

a voltage v_{ctrl} controls the oscillation frequency of the vco. The use of three stages was chosen to increase the oscillation frequency and reduce power consumption at the same time [1]. In fact, minimizing the number of stages reduces consumption and it increases oscillation frequency. The use of negative feedback improves the speed. 3.7v is used to drive the conventional vco. But the vco presented in this paper requires only 1v for driving. Hence, power consumption can be minimized.

Pll architecture

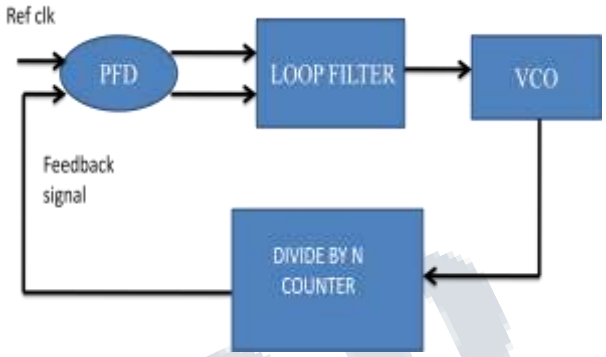

fig 1: block diagram of the proposed system

D.Phase frequency detection

the phase frequency detector detects a difference in phase and frequency between the reference and feedback signals. It responds to only rising edges of the two inputs and it is free from false locking to harmonics. Furthermore, the pfd outputs either a qa or a qb to the lpf. The pfd design uses two flip flops with reset features. The inputs to the two clocks are the reference and feedback signals [4]. The d inputs are connected to vdd—always remaining high. The outputs are either qa or qb pulses. These outputs are both connected to an and gate to the reset of the d-ff's. When both qa and qb are high, the output through the and gate is high, which will reset the flip flops. So both signals cannot be high at the same time which means the output of the pfd is either an up or down pulse—but not both. The difference in phase is measured by whichever rising edge occurs first [2].

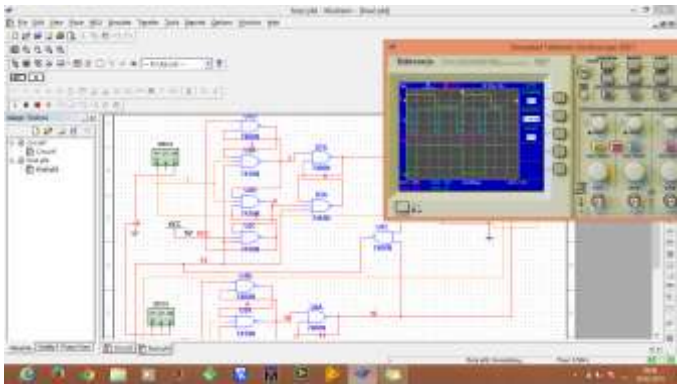

Fig 2: simulated result of pfd

E.low pass filter

the filter used in a pll may be either passive type or active type. Here we are using the passive type. The low pass filter removes the high frequency components and noise, and also controls the dynamic characteristics of pll. These characteristics include capture and lock range, bandwidth and transient response. If filter bandwidth is reduced, the response time increases. . However, reducing the bandwidth of the filter also reduces the capture range of the pll [4]. The filter serves one more important purpose. The charge on the filter capacitor gives a short time 'memory' to the pll. Thus, even if the signal becomes less than the noise for a few cycles, the dc voltage will continue to shift the frequency of the vco till it picks up the signal again [3]. This produces a high noise immunity and locking stability.

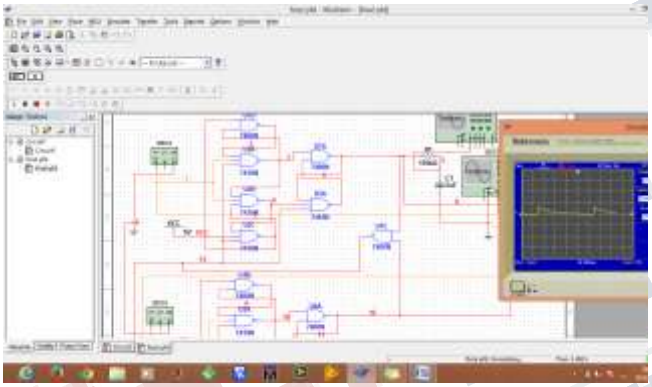

Fig 3: simulated result of the lpf C.**voltage controlled oscillator vco is commonly used in converting low frequency signals int**o an audio frequency range. A voltage-controlled oscillator is an electronic oscillator whose oscillation frequency is controlled by a voltage input. The input voltage determines the instantaneous oscillation frequency [1]. In this, we use a ring oscillator to make the oscillations. A ring oscillator consists of a number of delay stages, and the output of the last stage fed back to the input of the first stage [6]. **The vco oscillation frequency is determined b**y the resistor value, that is, the oscillation frequency decreases as the resistor value increases, and it will increases as the resistor value decreases. Here the lock frequency **range is from 250 khz to 1mhz at 5v** operation.

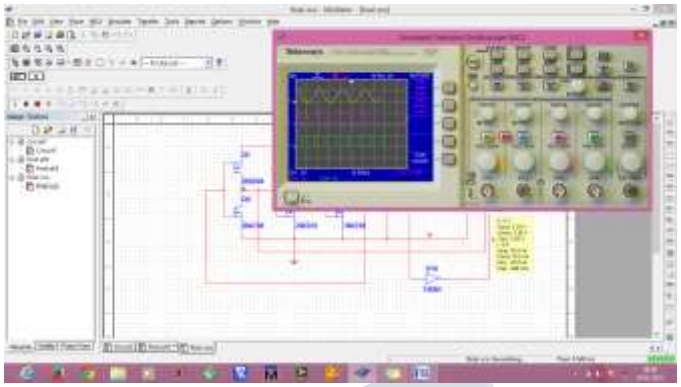

Fig 4: simulated result of vco

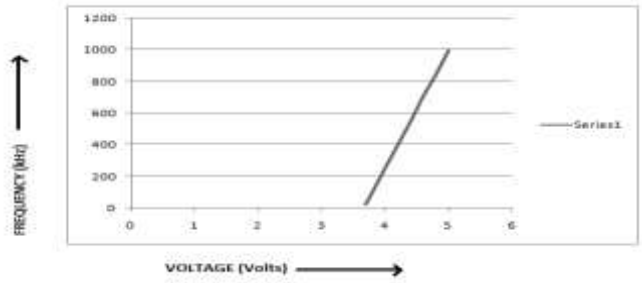

Fig 5: graphical representation of vcoG

G. Divide by n counter

we design the vco in such a way, the output of the vco is 'n' times the reference frequency. So the output o the vco is passed through a divide by 'n' counter and feedback to the input. Here the d flip-flop's qbar is connected to the d input. It will work as a t flip-flop with input connected to logic '1'.the frequency of oscillation is divided down to the feedback clock by the divider [3]. The phase is locked when the feedback clock has a constant phase error and the same frequency as the reference clock [2]. Because the feedback clock is a divided version of the oscillator's clock frequency, the frequency of oscillation is n times the reference clock.

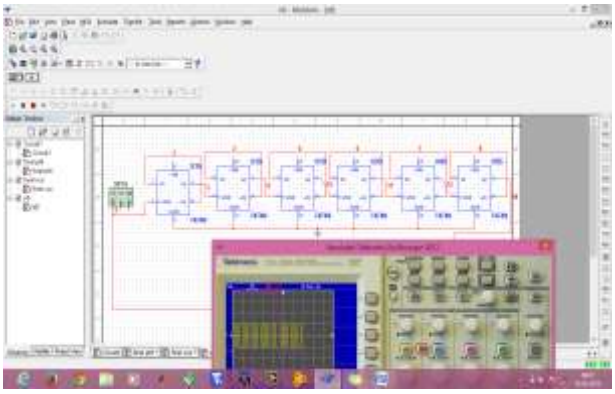

Fig 5: simulated result of divide by n counter

IV.CONCLUSION

the objective of the proposed work was to develop a phase locked loop as a frequency synthesizer. The schematic of all the four blocks are drawn and simulations of individual stages are verified. A new high speed low glitch cmos pfd is proposed. In order to achieve the stability in the loop filter, a resistor is added in series with the loop filter capacitor. Ring oscillator is selected as the voltage controlled oscillator in the design of pll. A divide by 64 counters is used for the synchronization with the input frequency. Power dissipation is reduced to 7.3w.

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