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Comparison Of Modelling Results On $Si_{0.74}ge_{0.26}$ And Ge Using High–K Dielectrics

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***Abstract:*— This work focusses on the use of Silicon Germanium ($Si_{0.74}Ge_{0.26}$) alloy and Germanium (Ge) as substrate materials for the simulation of MOS devices having a high–K material. HfO_2 was used as the dielectric material and Al as a metal gate. Two MOS devices on $Si_{0.74}Ge_{0.26}$ and Ge substrates have been simulated and their capacitance-voltage analysis has been done at different frequencies and compared. A comparative analysis of electrical characteristics of n-type MOSFETs made from $Si_{0.74}Ge_{0.26}$ and Ge substrate have been done in which channel length was varied to see the short-channel effects.**

***Index Terms* – dielectric; EOT; high–K; MOSFET; $Si_{1-x}Ge_x$**

I. INTRODUCTION

Germanium has lower bandgap and higher mobility of electrons, approximately twice as compared to silicon, but it is silicon which is being used because of its abundant presence. The issue of mobility could be resolved if some concentration of germanium is added in the silicon. This gives us the silicon-germanium ($Si_{1-x}Ge_x$) alloy. The higher mobility of carriers in $Si_{1-x}Ge_x$ led to the increase in drain current [1]. However, when its oxidation is done the oxide obtained has poor dielectric properties because of the formation of interfacial layers having Ge content [2]. This Germanium content layer mainly comprises of Germanium Oxide (GeO_x), which is an unstable material and often decomposes. This causes point defects at the surface, which becomes recombination – generation centers because Ge has small energy bandgap [3]. This led to the use of high-K dielectric materials as the gate oxide. These high–K dielectric materials offer very less Effective Oxide Thickness (EOT) [4]. It has been observed that the use of high–K dielectrics results in less gate leakage current and more on-state drain current [5]. Use of high–K dielectric materials like hafnium aluminate ($HfAlO_x$) [6], zirconium dioxide (ZrO_2), titanium oxide (TiO_2) [7], lanthanum lutetium oxide ($LaLuO_3$) [8] and hafnium silicate ($HfSi_xO_y$) [9] were reported earlier. HfO_2 has been used as the gate dielectric material for the formation of p-type Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) [10].

In this work, MOS and MOSFET structures on $Si_{1-x}Ge_x$ and Ge substrates were simulated using HfO_2 as the gate dielectric material. The simulations show the comparative study of device performance made on $Si_{1-x}Ge_x$ and Ge substrates. C-V characteristics of MOS structures at various frequencies were simulated and compared. I-V characteristics of MOSFET structures on $Si_{1-x}Ge_x$ and Ge substrates were simulated and compared by varying the channel length in order to see the short-channel effects. Here the composition of silicon and germanium in $Si_{1-x}Ge_x$ were taken as $Si_{0.74}Ge_{0.26}$.

II. MODELLING DETAILS

The device modelling was done on Synopsys Sentaurus Structure Editor. Four structures were modelled. First, two MOS capacitors were modelled which were based on p-type $Si_{0.74}Ge_{0.26}$ and Ge substrates. After that two MOSFETs were modelled by again using p-type $Si_{0.74}Ge_{0.26}$ and Ge substrates. Both the substrates had doping concentration of 10^{17} atoms/cm3 of boron (B). The modelled MOS structures along with their dimensions and materials are shown in figure 1(a) and 1(b).

In the case of MOSFET the gate metal used was of Al and the gate dielectric used was of HfO_2. The doping concentration of source and drain region was 10^{19} atoms/cm3 of arsenic (As). The modelled structures of MOSFET along with their dimensions and materials used are shown in figure 2.

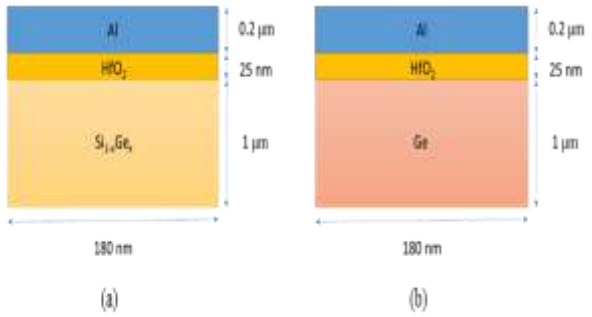

Figure 1: MOS Capacitor on (a)$Si_{1-x}Ge_x$ substrate, (b) Ge substrate.

In the figures 2(a) and 2(b), L is the channel length and L_S is the substrate length. These two lengths have been varied for different simulations.

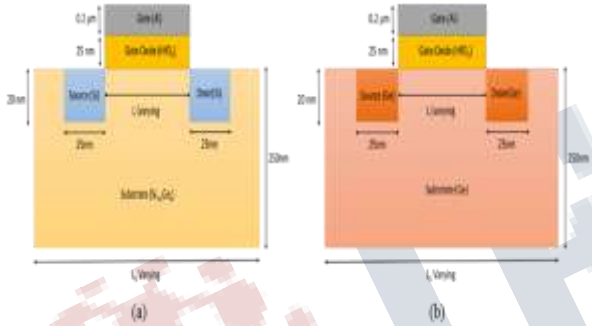

Figure 2: MOSFET on (a) $Si_{1-x}Ge_x$ substrate, (b) Ge substrate

III. RESULTS

The above mentioned structures were simulated on Synopsys Sentaurus Device.

I. Comparison of MOS Capacitors

The MOS capacitors shown in figure 1 were simulated after applying the voltage at the gate terminal and grounding the substrate terminal. The capacitance versus gate voltage curves were obtained for both the structures. The gate voltage was swept from -2 V to +2 V. The simulations for the C-V characteristics were done at various frequencies. The C-V characteristic curves at various frequencies for both the MOS capacitors are shown in figure 3

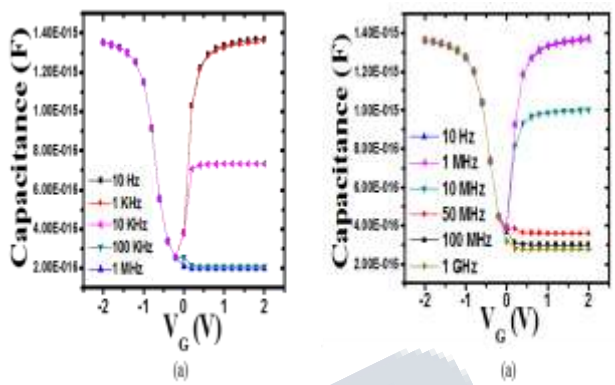

Figure 3: C-V Characteristics of MOS capacitor on (a) $Si_{1-x}Ge_x$, (b) Ge

Figure 3(a) shows the C-V characteristics of a MOS capacitor on $Si_{1-x}Ge_x$ substrate. When the gate voltage was swept from -2 V to +2 V at lower frequencies, the value of capacitance is same in the accumulation and the inversion regions. This occurs because at lower frequencies, the charges get sufficient time to follow the gate voltage. In the depletion region, the value of capacitance decreases due to the depletion capacitance. This does not happen when the simulation is done at higher frequencies. The charges could not follow the gate voltage and the value of capacitance remains at the value where there is maximum depletion width [11]. Figure 3(b) shows the C-V characteristics of a MOS capacitor on Ge substrate. This also shows the similar nature as shown by the MOS capacitor on $Si_{1-x}Ge_x$. The only difference is that the MOS capacitor on Ge substrate shows lower value of capacitance in the inversion region at very frequencies in the range of gigahertz. The reason behind this is the higher mobility of charge carriers in the Ge substrate [12], which gives sufficient time to charge carriers to follow the gate voltage even at frequencies in the range of megahertz. Figure 4 shows the comparison of change in capacitance with respect to the change in gate voltage, from 0 V to 2 V of the MOS capacitors made on Ge and $Si_{1-x}Ge_x$ substrates at high frequencies. This figure clearly shows that in the inversion region the value of capacitance for Ge MOS capacitor is more than from the $Si_{1-x}Ge_x$ MOS capacitors. This is because the value of capacitance for a material is directly proportional to its dielectric constant and the dielectric constant of Ge is higher i.e. 16 than that of $Si_{1-x}Ge_x$ which is 12.87 (11.7 + 4.5x, where x is 0.26) [13].

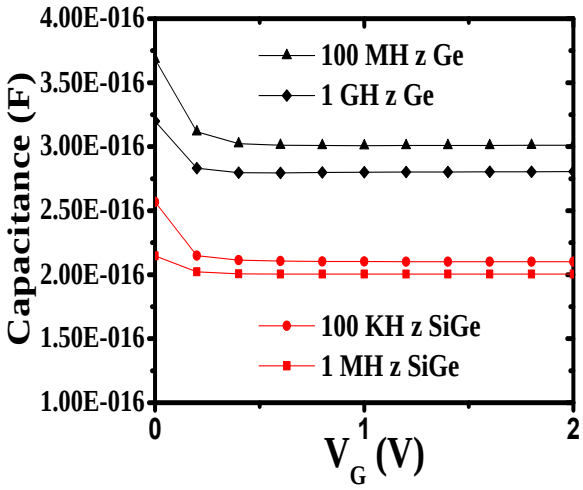

Figure 4. Comparison of C-V Characteristics of MOS capacitors at high frequencies in the voltage range of 0 to 2 V

II. *Output Characteristics of MOSFET*

The output characteristics of the structures shown in figure 2 were simulated. The simulations were done at various channel lengths. The channel length was varied from 180 nm to 28 nm. The voltage at the gate terminal has been kept equal to +2 V. The comparative curve of output characteristics of both the structures at various channel lengths is shown in figure 5.

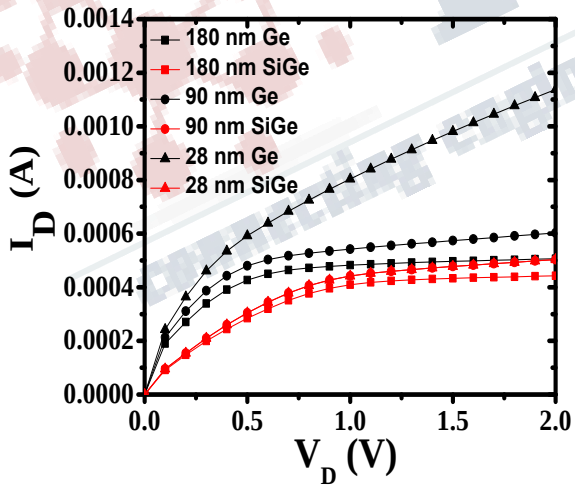

Figure 5: Output Characteristics of MOSFETs at V_G = 2 V for various channel lengths

From figure 5, it could be inferred that the value of drain current is more for the MOSFETs made on Ge substrate than on $Si_{1-x}Ge_x$ substrate. This is due to the higher electron mobility in Ge substrate than in $Si_{1-x}Ge_x$ substrate [12]. For both the structures, the value of drain current increases as the channel length was reduced. This could be understood from the equation given below:

$$I_D = \frac{\bar{\mu}_n Z C_i}{L}[(V_G - V_T)V_D - \frac{1}{2}V^2{}_D].....[1]$$

As the channel length is decreased, the value in the denominator becomes less which results in the increase of drain current.

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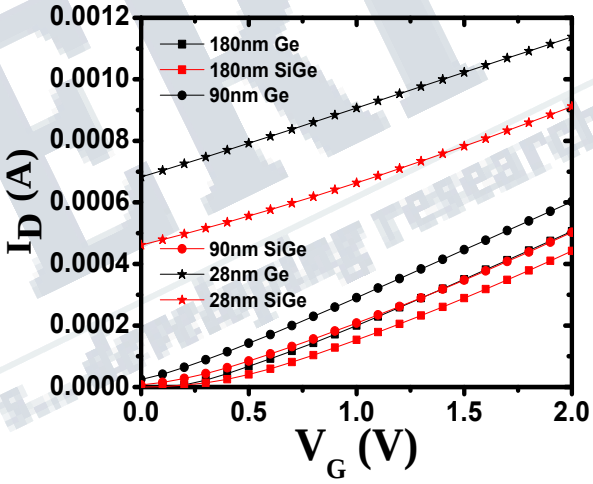

Figure 6. Transfer Characteristics of n-type MOSFETs at V_D = 2 V for various channel lengths

In figure 6, similar things could be observed. The values of drain current are more in the case of MOSFETs made from Ge in comparison to those made on $Si_{1-x}Ge_x$. This is again due to the larger electron mobility in Ge than $Si_{1-x}Ge_x$ [12]. When the channel has been decreased, similar sort of increase in drain current is observed, which could be understood from equation.

III. *Subthreshold Slope*

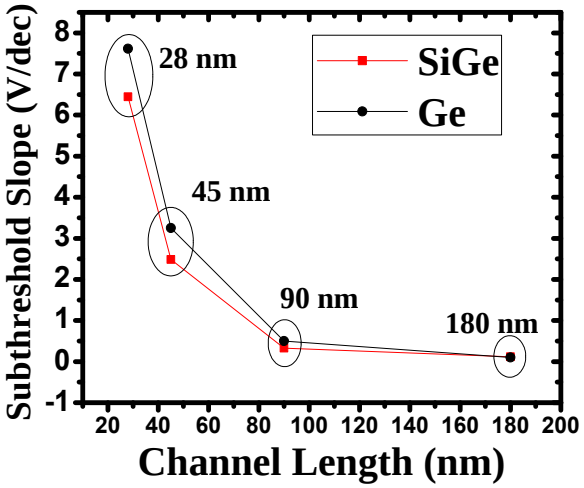

Figure 7: Subthreshold Slope at various channel lengths

The subthreshold slope of MOSFET structures shown in figure 2 were extracted from their $I_D - V_G$ characteristic curves. The results were obtained at various channel lengths and shown in figure 7.

The sub-threshold slope of a MOSFET is given by the equation:

$$S = \frac{dV_G}{d(\log I_D)} \quad \text{.....[2]}$$

At every channel length, the value of subthreshold slope for Ge is more. This is because the change in drain current with respect to the gate voltage is more in case of MOSFETs made on $Si_{1-x}Ge_x$ substrate than in case of MOSFETs made on Ge substrate (from figure 6). From figure 6, it could also be observed that change drain current for 90 nm channel length MOSFETs is more than from 28 nm channel length MOSFETs. Thus, lesser subthreshold slope (using equation (ii)). The same could be explained for 180 nm channel length MOSFETs. The small value of subthreshold slope indicates that the device act as excellent switch [16]. The values of 180 nm and 90 nm channel length MOSFETs are almost equal, in case of both the materials. So, these could act as excellent switch.

IV. CONCLUSION

The comparative study of devices made on Ge and $Si_{1-x}Ge_x$ substrate, with the use of high–K dielectric material, HfO_2 were compared. It could be concluded that devices made on Ge substrates could work at higher frequencies and could be used in various communication applications. The MOSFETs made on both $Si_{1-x}Ge_x$ and Ge substrates, having a channel length of 90 nm could act as excellent switches.

REFRENCES

[1] S. Mallik, C. Mahata, M.K. Hota, C.K. Sarkar, C.K. Maiti "Si1-xGex metal-oxide-semiconductor capacitor with $HfTaO_x$ gate dielectrics" in "Thin Solid Films" vol. 520 pp. 101-105.

[2] R Mahapatra, G S Kar, C B Samantaray, A Dhar,D Bhattacharya and S K Ray "ZrO_2 as a high-k dielectric for strained SiGe MOS devices" in "indian academy of sciences",vol. 25, No. 6, November 2002, pp. 455-457.

[3] Jongwoo Oh "Ge metal oxide semiconductor field effect transistor with optimized Si cap and $HfSiO_2$ high-k metal gate stacks" in "Current Applied Physics" vol 14 2014, pp S69-S73.

[4] S.Pal, S.K. Ray, B.R. Chakaraborty, S.K. Lahiri, D.N. Bose,"Gd_2O_3, $Ga_2O_3(Gd_2O_3)$, Y_2O_3, and Ga_2O_3, and Ga_2O_3, as high-k dielectrics on SiGe: A comparative study" in "Journal of applied physics" vol. 90, No. 8, 15 oct 2001.

[5] R.A. MinamisW, M. Schmidt, E. DurgunOzben, J.M.J. Lopes, J.M. Hartmann, K.K. Burdelle, J. Schubert, Q.T. Zhao, D.Buca, S.mantl "High mobility strained $Si_{0.5}Ge_{0.5}$/SSOI short channel field effect transistors with TiN/$GdScO_3$ gate stack" in "Microelectronic engineering" vol. 88 2011 pp. 2955-2958.

[6] S. Mallik, C. Mahata, M.K. Hota, G.K. Dalapati, D.Z. Chi, C.K. Sarkar, C.K. Maiti "$HfAlO_x$ High-k gate dielectric on SiGe: interfacial reaction, energy-band alignment, and charge trapping properties" in "Microelectronics Engineering" vol. 87 2010 pp. 2234-2240.

[7] M K Bera, C Mahata, C K Maiti "Ultrathin High-k Gate dielectric Films on strained-Si/SiGeHetrolayers" in "IETE journal of research" vol 53, No. 3, May-June 2007, pp 237-251.

[8] W.Yu, B. Zhang, Q.T. Zhao, J.M. Hartmann, D. Buca, A. Nichau, R. Luptak, J.M. Lopes, S. Lenk, M. Luysberg, K.K. Bourdelle, X. Wang, S. Mantl "High mobility compressive strained $Si_{0.5}Ge_{0.5}$ quantum well p-MOSFETs with higher-k/metal-gate" in "solid-state electronics" vol. 62 2011 pp. 185-188.

[9] S.Addepalli, P. Sivasubramani, M.J. Kim, B.E. Gnade, R.M. Wallace "The Electrical properties and stability of the hafnium Silicate/ $Si_{0.8}Ge_{0.2}$(100) interface" in "Journals of Electronic materials" vol. 33, No. 9, 2004.

[10] Olivier Weber, Jean-Francois Damlencourt, Francois Andrieu, Frederique Ducroque, Thomas Ernst, Jean-Michel Hartmann, Anne-Marie Papon, Oliver Renault, Bernard Guillaumot, Simon Deleonibus "Fabrication and mobility characterstics of SiGe surface channel pMOSFETs with a HfO_2/TiN gate stack" in "IEEE transactions on electron devices" vol. 53, No. 3, March 2006, pp.449-456.

[11] T. Kundu, R. Garg, N.A. Chowdhury, D. Misra "Electrical techniques for the characterization of dielectric films" in "The electrochemical society interface" Fall 2005.

[12] Chung-Hao Fu, Kuei-Shu Chang-Liao, Wei-Hao Tseng, Chun-Chang Lu, Tien-Ko Wang, Wen-Fa Tsai, Yu-Chen Li, Chi-Fong Ai "Improved electrical characteristics and reliability of Ge MOSFET device with nitride high-k gate dielectric by plasma immersion ion implantation" in "microelectronics engineering" vol 88 2011 pp. 1560-1563.

[13] Schaffler F., in Properties of Advanced SemiconductorMaterialsGaN, AlN, InN, BN, SiC, SiGe . Eds. Levinshtein M.E., Rumyantsev S.L., Shur M.S., John Wiley & Sons, Inc., New York, 2001, 149-188.

[14] Ben G. Streetman, Sanjay Kumar Banerjee, "Solid state electronic device," eq. 6-49, pp. 295.

[15] Ben G. Streetman, Sanjay Kumar Banerjee, "Solid state electronic device," eq. 6-66 pp. 311.

[16] Ben G. Streetman, Sanjay Kumar Banerjee, "Solid State Electronic Device," sec. 6.5.7, pp. 311.