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Improved Double Tail Dynamic Comparator

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***Abstract*- Comparator is one of the basic building blocks of analog to digital converter. The need for ultra-low-power, area efficient and high speed analog-to-digital converters is pushing toward the use of dynamic regenerative comparators to improve speed and efficiency of power. In this paper, an analysis on the delay of convectional dynamic single Tail comparator, Double Tail Comparator and double tail comparator for low power will be presented. The sub threshold leakage of transistors has usually been very small in the off state, as gate voltage is below threshold. But as voltages have been scaled down with transistor size, sub threshold leakage has become a considerable factor. Hence, to reduce the sub threshold leakage a new CMOS dynamic comparator using conventional CMOS inverter and switches method is proposed. The circuit has a dual input single output differential amplifier which is suitable for high speed analog to digital converters with improved speed and low power dissipation. The simulation results confirm the analysis and show that in the proposed dual tail dynamic comparator both power consumption and delay time are significantly reduced even in small supply voltage.. The simulation results will be shown in Mentor Graphics.**

I. INTRODUCTION

The clocked regenerative comparators are mostly used in High speed ADCs. Clocked comparators can make fast decisions as they have strong positive feedback in the regenerative latch. There are many analyses such as noise, offset; random decision errors and kick back noise are present. Here, a delay analysis is presented. The delay of different clocked comparators such as conventional dynamic single tail comparator, double tail comparator and double tail comparator for low power is analyzed practically. For each modification in the circuit the delay and power will be reduced. The comparator design is slightly modified in order to reduce the leakage power which further reduces the total power and delay of the circuit.

II. CLOCKED REGENERATIVE COMPARATOR

Clocked regenerative comparator have found wide application in many high-speed ADCs since they can make fast decision due to the strong positive feedback in the regenerative latch recently, many comprehensive analysis have been presented , which investigate the performance of the comparators from different aspects .such as noise, offset and noise.

- Conventional Dynamic single-tail comparator
- Conventional Dynamic double-tail comparator
- Dynamic double –tail comparator with low power

A. Conventional Dynamic single-tail comparator

Conventional dynamic comparator is widely used in A/D converters. The comparator has high input impedance, rail-to-rail output swing, and has no static power consumption. It has two phases

- Reset phase
- Comparison phase

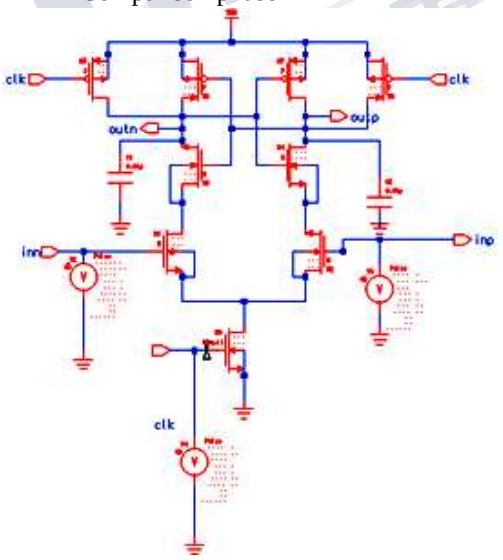

Fig 1 : Schematic diagram of the conventional Single-tail dynamic comparator

The operation of the conventional dynamic comparator is explained below. During the reset phase , when CLK=0 and Mtail is off , the reset transistor M5 and M8 pull both the output nodes Outn and Outp to VDD to define a start condition and to have a valid logical level during the reset. In the comparison phase, when CLK = VDD, transistors M5, M8 are off and Mtail is on. Output

nodes (Outp, Outn) which had been pre-charged to VDD, start to discharge at different discharging rates depending on the input voltages (VINP,VINN).Assuming the case where VINP > VINN, the output node Outp discharges faster than Outn, hence with Outp (discharged by transistor M2 drain current), falling down to VDD–|Vthp| before Outn (discharged by transistor M1 drain current), the corresponding PMOS transistor (M6) will turn on to initiate the latch regeneration caused by back-to-back inverters (M3-M6 and M4-M7). Thus, the output node Outn pulls to VDD and Outp discharges to ground. If the input voltage VINP is less than VINN, the circuit works vice versa.

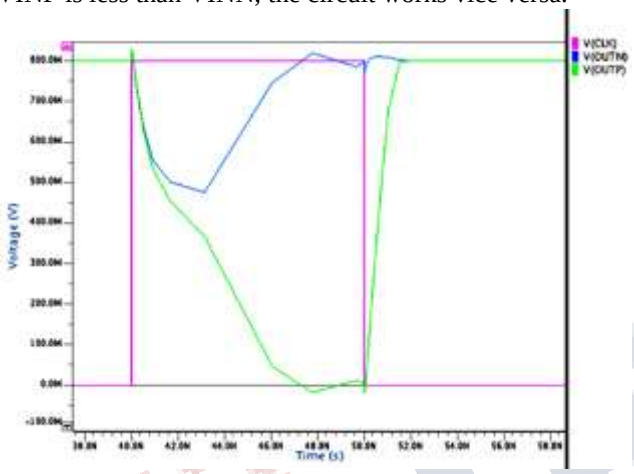

Fig 2: Transient simulation of conventional dynamic single double-tail comparator

The total delay of this comparator derived as

$$t_{delay} = t_0 + t_{latch} = 2\frac{C\,L|Vthp\,|}{I\,tail} + \frac{C\,L}{gm,eff}\,ln\left(\frac{VDD}{4|Vthp\,|\Delta vin}\sqrt{\frac{I\,tail}{\beta\,1,2}}\right)$$

Simulation results specify that the effect of reducing the Vcm along with the increase of *t*0 and reduction of *t*latch finally leads to an increase in the total delay of the comparator. This circuit structure has the advantages of high input impedance, rail-to-rail output swing, no static power consumption, and good robustness against noise and mismatch. Here, parasitic capacitances of input transistors do not directly affect the output nodes' switching speed. Hence, to minimize the offset, it is possible to design large input transistors. On the other hand, there is a disadvantage with this topology i.e., due to several stacked transistors, a sufficiently high supply voltage is needed to obtain a proper delay time. The delay time of the circuit becomes large due to lower trans conductance of the latch. Another main drawback of this structure is that there is only one current path. Through the tail transistor for both the differential amplifier and the latch there is only one current path. One should prefer a small current path for the differential amplifier to keep the differential pair in weak inversion and to obtain a long integration interval. A large current path is required for the fast regeneration in the latch.

B.Conventional Double-Tail Comparator:

This structure has less stacking and therefore can operate at lower supply voltages compared to the conventional dynamic comparator. The double tail enables both a large current in the latching stage and wider Mtail2, for fast latching independent of the input common-mode voltage (Vcm), and a small current in the input stage (small Mtail1), for low offset. It has two phases

- Reset phases
- Decision–making phases

During the reset phase (CLK = 0, Mtail1 and Mtail2 are off), transistors M3,M4 pre-charge the nodes fn and fp to VDD, which in turn make MR1 and MR2 to discharge the output nodes Outn and Outp to the ground. During decision-making phase (CLK=VDD, Mtail1 and Mtail2 turn on), the transistors M3,M4 turn off and the voltages at nodes fn, fp start to drop with the rate defined by IMtail1/Cfn(p) and an input-dependent differential voltage ΔVfn(p) will also build up. The intermediate stage formed by the transistors MR1 and MR2 passes ΔVfn(p) to the cross coupled inverters and provides a good shielding between to input and output to get a reduced value of kickback noise.

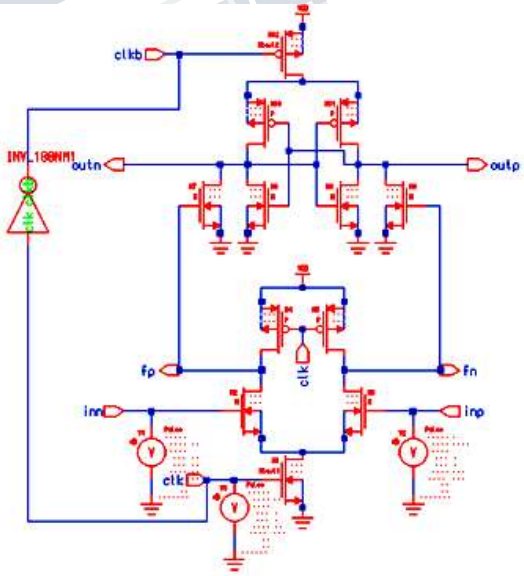

Fig 3: Schematic diagram of convectional double–tail comparator

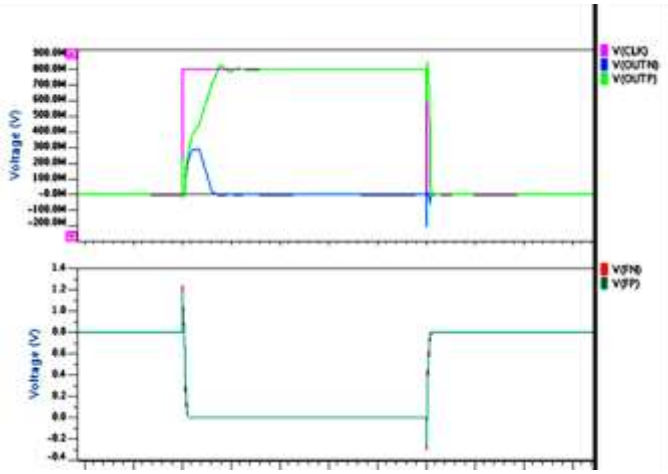

Fig 4: Transient simulation of convectional dynamic double-tail comparator

The total delay of this comparator derived as

$$t_{delay} = t_0 + t_{latch}$$

$$= 2\frac{C\,LoutVThn}{I\,tail2} + \frac{C\,Lout}{gm,eff}\,.\,ln\left(\frac{VDD/2}{\Delta vo}\right)$$

$$= 2\frac{C\,LoutVThn}{I\,tail2}\frac{C\,Lout}{gm,eff}\,.$$

$$ln\left(\frac{VDD.I\,tail^{\,2}\,C\,L,fn(p)\,.}{8V^{\,2}Thn.C\,Lout\;\;gmR1,2\;gm\;1,2\;\;\Delta vin}\right)$$

From the equations derived for the delay of the double-tail dynamic comparator, some important notes can be concluded.

The latch initial differential output voltage (ΔV0) and consequently the latch delay will be affected by the voltage difference at the first stage outputs (ΔVfn/fp) at time t0. Therefore, increasing it would profoundly reduce the delay of the comparator.

In this comparator, both intermediate stage transistors will be cut-off finally, (since fn and fp nodes both discharge to the ground), hence they do not play any role in improving the effective trans conductance of the latch. On the other hand, during reset phase, the nodes fn and fp have to be charged from ground to VDD, which means power consumption.

C.Double-Tail Dynamic Comparator With Reduced Low Power:

The structure of this comparator is to increase ΔVfn/fp in order to increase the latch regeneration speed. For this purpose, Mc1and Mc2 are the two control transistors that have been added to the first stage in parallel to M3/M4 transistors but in a cross-coupled manner

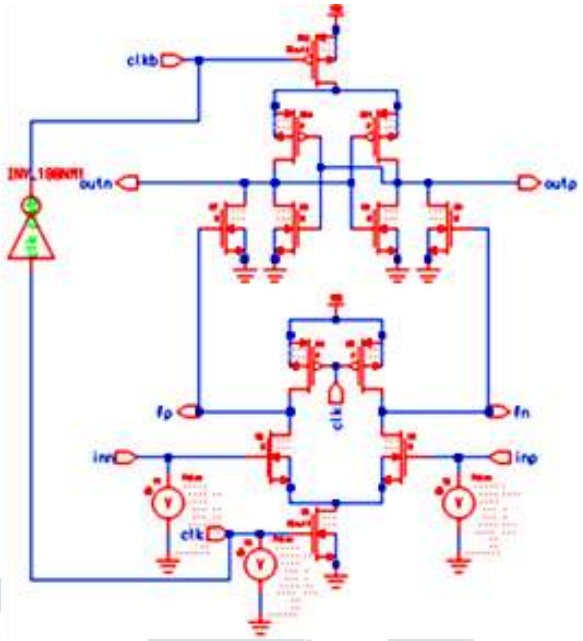

Fig 5: Schematic diagram of proposed double-tail comparator

It has 2 type of phases

- Reset
- Decision–making phase

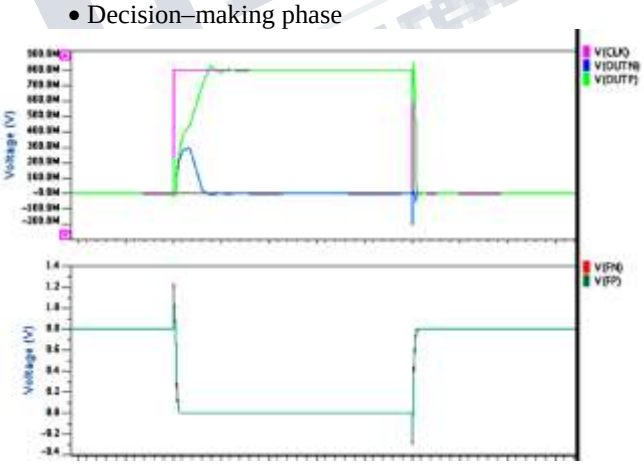

Fig. 6: Transient simulation of convectional dynamic double-tail comparator with low power

During reset phase (CLK = 0, Mtail1 and Mtail2 are off, avoiding static power), M15 and M14 pulls both fn and fp nodes to VDD, hence transistor M6 and M12 are cut off. Intermediate stage transistors, M8 and M10, reset both latch outputs to ground. During decision-making phase (CLK = VDD, Mtail1, and Mtail2 are on), transistors M15 and M14 turn off. Furthermore, at the beginning of this phase, the control transistors are still off (since fn and fp are about VDD). Thus, fn and fp start to drop with different rates according to the input voltages.

The total delay of this comparator derived as:

$$t_{delay} = t_0 + t_{latch}$$

$$= 2\frac{C\ LoutV\ \mathrm{Thn}}{I\ tail\ 2} + \frac{C\ Lout}{gm\ ,eff + gmr\ 1{,}2}.\ ln\left(\frac{VDD/2}{\Delta vo}\right)$$

$$= 2\frac{C\ LoutV\ \mathrm{Thn}}{I\ tail\ 2}\frac{C\ Lout}{gm\ ,eff + gmR\ 1{,}2}$$

$$.\ln\ \frac{\frac{VDD}{2}}{4V\mathrm{thn}\,|V\mathrm{thp}|\ \frac{gmR\ 1{,}2}{I\ tail\ 2}\ \frac{\Delta vin\ gmR\ 1{,}2}{I\ tail\ 1}\ \exp\frac{(Gm\ ,eff\ 1.to\ )}{C\ L,fn(p)}}$$

By comparing the expressions derived for the delay of the three mentioned structures, we can say that this comparator takes advantage of an inner positive feedback in double-tail operation and it also strengthens the whole latch regeneration. This speed improvement can be observed more in lower supply voltages. Because for larger values of VTh/VDD, the trans conductance of the transistors decreases, then the existence of an inner positive feedback in the architecture of the first stage will lead to the improved performance of the comparator circuit.

III. IMPROVED DOUBLE TAIL DYNAMIC COMPARATOR FOR LOW POWER APPLICATIONS

A. Sub-Threshold Conduction

As technology scales down, the size of transistors has been shrinking. The number of transistors on chip has thus increased to improve the performance of circuits. In order to maintain the characteristics of an MOS device, the supply voltage, being one of the critical parameters, has also been reduced accordingly. Therefore the threshold voltage is also scaled down at the same rate as the supply voltage in order to maintain the transistor switching speed. As a result, leakage currents increase drastically with each technology generation. As the leakage current increases faster, it will become more and more proportional to the total power dissipation.

$$PLEAK = ILEAK*VDD$$

To reduce total leakage in Nano scale circuits, some new techniques have to be developed to reduce the sub threshold leakage especially for chips that are used in portable systems which are power constrained. The leakage current consists of reverse bias diode currents and Sub-threshold current. The reverse bias current is due to the stored charge between the drain and bulk of active transistors while the Sub-threshold current is due to the carrier diffusion between the source and drain of the off transistors. Hence, in this paper conventional CMOS inverter based approach is used to reduce the Sub-threshold leakage power.

B. Design and Operation

The amplifier circuit is modified according to the inverter logic. The inverter logic which reduces the leakage. Here, two inverters are used. The inputs are applied to two inverters and the outputs are connected to a active load. The circuit will be used in our double tail comparator structure. The differential amplifier will be modified with this inverter logic. The output will be applied to the latch for regeneration.

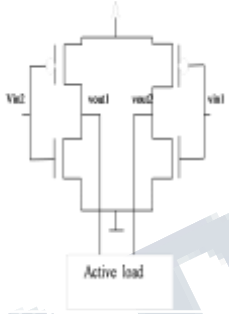

Fig. 7: Inverter Based Amplifier Design

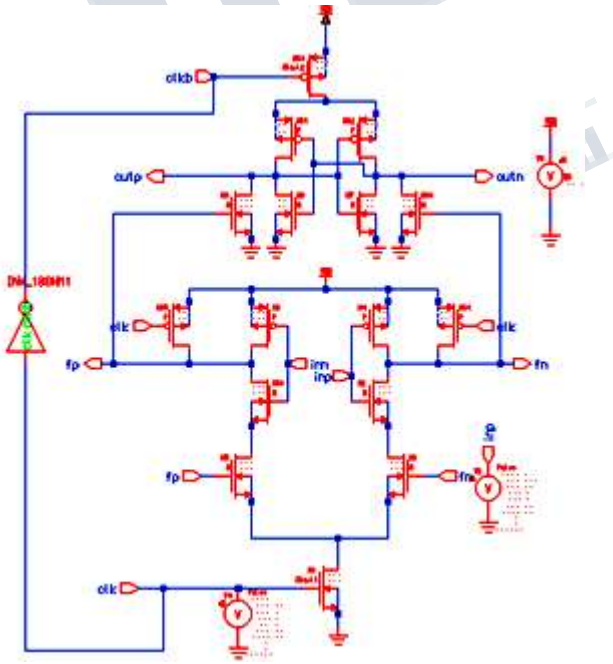

Fig .8: Schematic of Improved double-tail comparator with reduced leakage power and voltage

It has two phases:

- Reset
- Decision–making

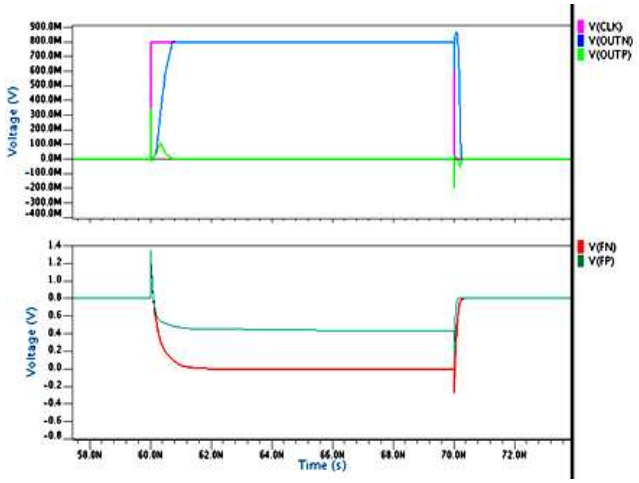

Fig .9: Transient simulation of conventional dynamic double-tail comparator with reduced leakage power and switches

During reset phase when CLK=0, M_{tail1} and M_{tail2} are off and M15 and M14 are on so that the two transistors M8 and M10 will be on and pulls the two output nodes outp and outn to ground. During decision making phase, when CLK=V_{DD}, the two tail transistors M_{tail1} and M_{tail2} are on and M14 and M15 are off which turns the two transistors M8 and M10 off. Consider the case where INN>INP, then the transistors M_2 will turn on faster so the output of that inverter falls down which turns the intermediate transistor M10 off. Hence, out1 pulls up to V_{DD}. When outp goes to V_{DD}, the transistor M11 will be off which remains outn at ground. By using this approaches the Sub-threshold leakage and hence the total power will be reduced. The simulation results prove the reduction on. Here in the differential amplifier inverters are used which are series transistors. Hence, the trans conductance of the total circuit increases which reduces the total delay of the circuit. Hence, by using this CMOS inverter approach the total power and delay can be reduced. The simulation results show the reduction in both power and delay.

IV. RESULTS AND CONCLUSION

Table .1: Comparison of different comparator structures

	Convectional dynamic comparator	Double tail dynamic comparator	Double-tail dynamic comparator with low power	Improved Double tail dynamic Comparator
Technology CMOS	180nm	180nm	180nm	180nm
Supply voltages	0.8v	0.8v	0.8v	0.8v
Delay	1.6192ns	993.20ps	90.000ps	58.935ps
Peak transient noise voltage	20.782	6.997	5.3705	1.2264
Power dissipation	12.90pW	9.6661pW	9.629pW	9.6017pW

Table. 2: Delay Vs Supply voltage for different i/p voltage differences

Delay vs. supply voltage		i/p voltage difference (ΔVin)		
	Supply Voltage	***5mv***	***50mv***	***200mv***
Double-tail dynamic comparator with low power	***0.7v***	849.82ps	159.2ps	140.2ps
	1v	233.10ps	125.8ps	119.58ps
	1.2v	159.21ps	95.35ps	83.933ps
Improved Double-tail comparator	***0.7v***	144.81ps	68.881ps	67.881ps
	1v	114.95ps	112.3ps	65.551ps
	1.2v	113.73ps	91.220ps	81.36ps

Table. 3: Delay Vs i/p voltage differences for different supply voltages

Delay vs. Δ Vin		i/p voltage difference (ΔVin)		
	Vcm	***0.001***	***0.015***	***0.03***
Double-tail dynamic comparator with low power	***0.6v***	254.3ps	147.33ps	147.33ps
	0.8v	103.01ps	102.3ps	94.28ps
	1v	103.00ps	94.28ps	46.488ps
Improved Double-tail comparator	***0.6v***	132.65ps	98.87ps	98.87ps
	0.8v	103.00ps	51.95ps	50.951ps
	1v	102.00ps	46.488ps	46.488ps

The delay of clocked comparators was analyzed and equations were derived. Dynamic latched comparator was designed that works with high speed and low power when compared to previous comparators. The simulation results showed that the proposed circuit can operate at higher speed with low power dissipation. Compared to the conventional structure, the proposed method occupies less chip area. A CMOS inverter based amplifier design with switches was implemented to reduce the sub threshold leakage. The simulation results confirmed the analysis and showed that in the proposed dual tail dynamic comparator both power consumption and delay time are significantly reduced even in small supply voltage. The Power and delay of each circuit were measured and compared. Now we can

conclude that the proposed comparator is delay efficient and power efficient.

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