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Programmable Hybrid Embedded Controller Architecture using Clock Gating Technique

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Abstract: **Power consumption has become a major concern for modern microprocessor designs; it affects the battery life in the mobile segment, and limits the chip frequency in desktops and servers. Minimizing power consumption is a primary consideration in hardware design of portable devices where high performance and functionality is required with limited battery power. With the scaling of technology and the need for high performance and more functionality, power dissipation becomes a major bottleneck for microprocessor systems design. Clock power can be significant in high performance systems. To reduce the wastage of clock power, a gating circuit is implemented to stop the clock where clock is not used by the blocks.Dynamic power can contribute up to 50 % of the total power dissipation. The main goal of this work is to implement a prototype programmable Hybrid Embedded Controller Architecture targeted on to the FPGA chip and analyze the power consumption of the registers and memory etc. The whole design is captured using VHDL make use of Xilinx tool.**

***Index Terms*—Microprocessor, Power consumption, Dynamic Power, VHDL, Clock Sig*nal**

I. INTRODUCTION

Excessive power dissipation in integrated circuits not only discourages their use in a portable environment, but also causes overheating, which degrades performance and reduces chip life time. In particular, modern devices have reached such a high level of complexity that an entire system can now be implemented on a single chip. Unfortunately, this has come at the cost of an extremely high power demand, which often dictates a strict limit to chip frequency. Recently growing demand for low-power portable devices and computing systems has created a need to limit the power consumption in many chip designs. Today, a large fraction of the overall power dissipation on a chip is due to clocks and data path. Power consumption is one of the important factors in the design of integrated circuits especially in CPU designs.

Clock gating is one of the techniques of dynamic power management to reduce the dynamic power consumption. Naturally in a processing unit clock runs continuously to all the blocks though there is no necessity of clock to all the blocks at the same time. By running the clock to the blocks where clock is unnecessary, clock power is wasted. To reduce the wastage of clock power, a gating circuit is implemented to stop the clock where clock is not used by the blocks. This is the main principle of the clock gating circuit.

II. LOW POWER METHODOLOGIES AND CLOCK GATING TECHNIQUES

Low power has emerged as a principle theme today. The need for low power has caused a major paradigm shift in which power dissipation is as important as performance and area. From the environmental point of view, the smaller the power dissipation of electronic systems, the lower the heat pumped into rooms; the lower the electricity consumed and less impact on the global environment. The motivation for reducing power consumption differs from application to application; for example, in the class of micro-powered battery operated portable applications, such as cellular phones and PDAs etc. The goal is to keep the battery life and weight reasonable and the packaging cost low. For high performance portable computers such as laptop and network computers, the goal is to reduce the power dissipation of the electronics portion of the system. Finally high performance, non-battery operated systems, such as work stations, set-top computers, and communication systems, the overall goal of power minimization is to reduce system cost (cooling, packaging, and energy) and ensure long term circuit reliability.

III. PROGRAMMABLE HYBRID EMBEDDED CONTROLLER (HEC) CORE ARCHITECTURE

Power has become a primary consideration in hardware design, and is critical in computer systems especially for portable devices with high performance and more functionality. Clock gating is the technique used for reducing processor's power. In this work clock gating technique is applied to optimize the power of fully programmable Hybrid Embedded Controller (HEC) employing RISC architecture. The CPU designed supports i) smart instruction set, ii) I/O port, UART and 7 segment driver, and iii) RISC as well as controller concepts.

A novel design of control unit is proposed and implemented to generate various clock gating signals along with control signals to perform required operations and to shut off the clock to the unused/unwanted components for

that particular instruction. When unused/inactive units are shut off, automatically charge/discharge capacitance of the units are reduced in turn reducing the dynamic power. The whole design is concentrated on how to reduce the dynamic power without compromising the performance and speed. The instruction set is designed in such a way that, user can develops the application program in simple manner. It has smart instruction set, these instructions do not cause any functional limitation, but enables an effective way of power saving through generation of gated clock signals. The whole design is captured using VHDL and Verizon and is implemented on FPGA chip using Xilinx.

IV. ARCHITECTURAL OVERVIEW

Figure 1 shows main modules of the programmable hybrid embedded controller (HEC).

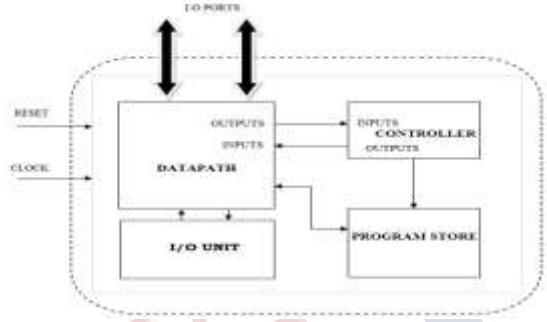

Fig: 1 Main modules of HEC core

The main modules of HEC are data path unit, control unit and program store. Program store is used to store the programs/instructions. Data path unit handles the data processing operations and provides data flow between the various sub modules of this unit. This data path is sufficient to execute most instructions, so it will be used to introduce the overall HEC core architecture. The controller module is connected via a number of inputs and outputs to the data path module. State of the art controller module is developed and implemented to control the overall operations of HEC. Data path unit also interfaces with external peripheral devices/ external world, the program store on-chip, enables the HEC core to execute at the internal clock speed of CPU.

The design description can be divided into two main blocks i) the controller ii) data path. The controller and data path communicate through two types of signals a) control signals are outputs of the controller and inputs of the data path b) conditional signals are outputs of the data path and inputs of the controller.

Data path is both logical and physical structure, which consists of two types of sources i) combinational elements such as adders, comparators etc. ii) active modules, which consists of multiplexors, tri-state buffers, modified latches and new registers driven by control signals. Registers and latches are enabled by control signals; hence they can be seen as stable holding active elements. To begin with CPU uses Harvard memory architecture, in which program and data are accessed from separate memories using separate buses, this improves bandwidth over traditional Princeton memory.architecture, where data and program may be fetched from the same memory using the same bus. Instruction words are 16 bits wide making it possible to have all single word instructions. A 16-bit wide program memory access bus fetches a 16-bit instruction in a single cycle. The CPU directly addresses its register files or data memory. All special function registers (including the program counter) are mapped in the memory. The designed PEC CPU has a smart instruction set that makes it possible to carry out any operation or any register using single addressing mode. This nature makes programming with the CPU simple but efficient. PEC core contains various modules; controller, ALU, register file, program memory, data memory, external I/O interface, UART, BCD to 7 segment driver, clock generator. The Controller module generates the control signals as well as clock gating signals to the various modules of CPU to perform the desired operation and shut off the clocks to the unused modules. ALU module contains 16-bit ALU and working register (Z). The ALU is general arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file. In two operand instructions, typically one operand is the working register (Z register called output register), the other operand is a file register or an immediate constant. In single operand instruction, the operand is the either the working register or a file register. Register file is a set of registers that are modeled as 16-bit words, used to store intermediate values during instruction processing. The program memory (ROM) is 4K×16 bit word length and is used to store the instructions. The data memory (RAM) 256×16 is used to store the temporary data during execution of instructions. Port 0 and Port 1 are two ports which are configured as output and input ports respectively. A display driver for BCD to 7 segment display is designed to drive the 7-segment display unit. Universal Asynchronous

Receiver and Transmitter (UART) is modeled to receive / transmit the data serially to/from the serial I/O devices. Serial I/O line is compatible with TTL logic levels. The PEC is initiated by the reset signal whenever reset signal asserts high, the controller generate appropriate signals to load the PC address of the ROM. The external interrupt mechanism activates on any hardware interrupt or reset signal arriving at the controller when it is in idle mode.

Modules of PEC core: The PEC core architecture is divided into five main modules, viz; i) control unit/controller, ii)

data path unit, iii) Memory unit, iv) I/O unit, and v) other units. Control unit decodes the instruction input and generates the control signals, clock gating signals to the active modules. Data path unit handles the data transfer and performing ALU operations by executing the instructions. Memory unit handles the both data and program instructions individually. I/O unit handles the input and output operations with the external devices. The other units like clock generator and clock management system manage the clocks as per the requirement of the PEC core CPU.

***Controller Architecture*:** The controller module (figure 6.15) is connected via a number of inputs and outputs to the data path module. The controller is responsible for decoding the current instruction in the instruction register (IR). The control signals of the data path are generated to route the data correctly from source to the destination according to the instruction. For different instructions, the controller generates different set of control signals to perform the operations of the data path unit. These signals also controls on chip peripherals (ports, UART, BCD to 7 segment). Figure 6.15 shows the inputs and outputs of the controller module. The controllers produce the control signals for the micro operations. The micro operations are the operations that are executed by the subunits of the PEC in one machine cycle. The control unit provides all of control signals to regulate the data traffic and necessary signals to perform the desired functions. The control unit architecture contain a state machine that causes all appropriate signal values to update, based on current state and input signals and produce a next state for state machine. Simply saying, state machine that asserts a predefined number of signals for various instructions. The control unit performs two processes. The first is a combinational process (not clocked) that examines the current state and all inputs and produces output control signals and next state output. The second is the sequential process (having a clock) that is used to store the current state and copy of the next state to the current state. If the reset signal is high the sequential process set the current state value to reset1, the first state of the reset sequence. The controller generate appropriate clock gating signals to implement clock gating mechanism at various levels of embedded controller to reduce the power consumption of the chip.

V. RESULTS AND DISCUSSIONS

An important aspect in the design of PEC core architecture is to generate the clock signals and distributing the clock signal to all the units of PEC core. Buffered clock tree is considered, to drive the internal buses, input and output of each subunit. By isolating each unit from the other, desired signal levels are obtained. The whole design is captured in HDL and simulated, synthesized using Xilinx tool. The dynamic power was measured using Xpower power analysis tool and the design was successfully tested with and without clock gating technique. The results of whole design are divided into parts as i) clock gating circuit ii) latches iii) clock error detecting circuit iv) data path and control unit v) ALU and vi) HEC core.

Control Unit : Control unit is the heart of HEC core which will take instruction code as input and decoded by this unit and generates various control signals to select or activate the components for the particular instruction processing. These signals control on-chip RAM, ROM, register bank, serial I/O port, parallel I/O port, BCD to 7 segment display drivers and latches. These signals are classified as i) address signals (for on chip peripherals) ii) control signals (read/write) iii) select signals (activate the components) iv) clock gating signals (to generate gated clocks signals for the active components). Control unit is successfully implemented and all above signals are generated based on the type of instruction executed.

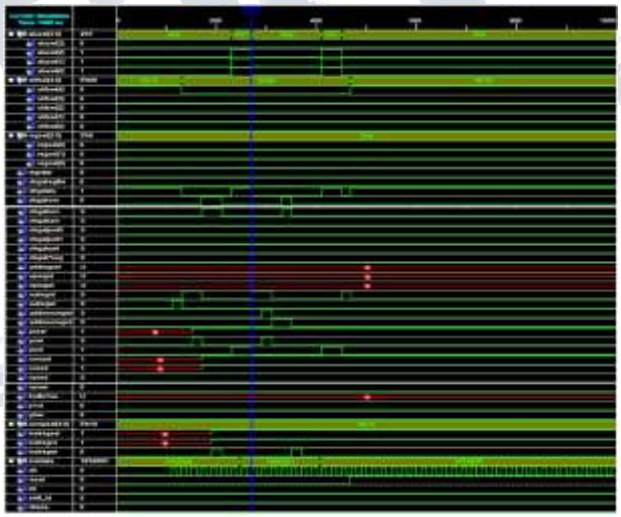

Fig: 2 Simulation results of PEC core control unit during execution of ADD instruction.

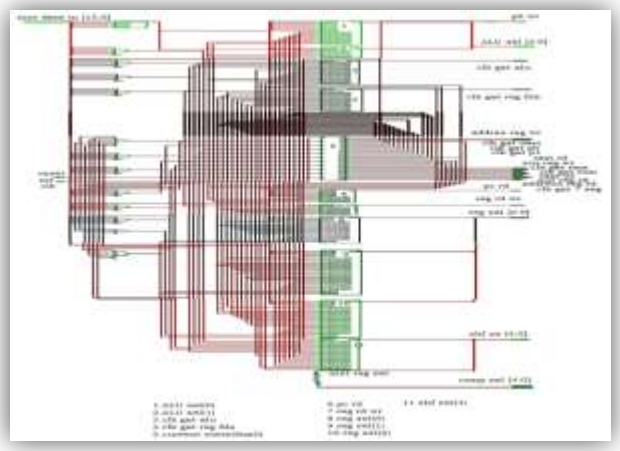

Fig: 3 RTL schematic of a novel control unit of PEC core architecture

Registers **:** During PEC core implementation, various registers are new register, out-register, modified out register, register file used to store the data temporarily during execution of the program or provides the data to the data path unit to perform ALU operations. Figure 4 & 5 shows the RTL schematic of new register and modified out-register respectively.

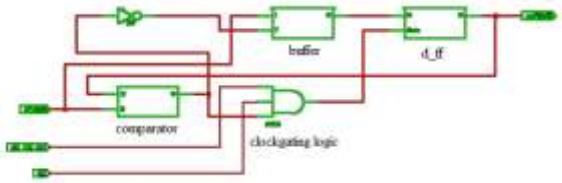

Fig: 4 RTL schematic of new register

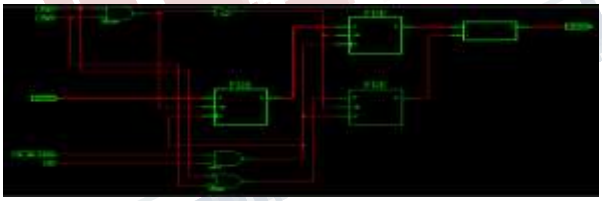

Fig: 5 RTL schematic of modified 16-bit out_register

Power consumption of new register and conventional register are shown in figure 6. When using new register instead of conventional register in the architecture of HEC core, the power analysis shows that new register saves the power. Power saving can be 10.38% operated at 1GHz.

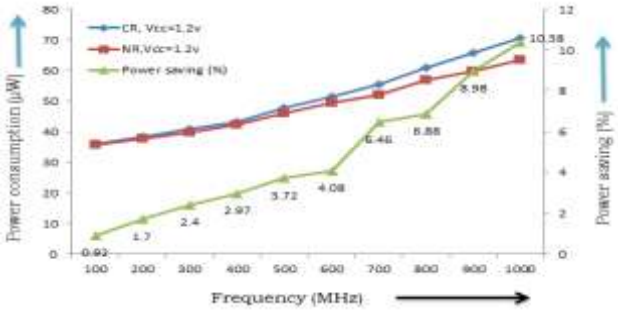

Fig: 6 Power consumption of conventional and new registers

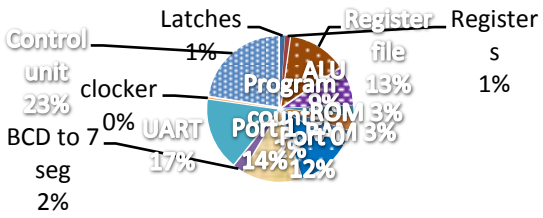

Fig: 7 Power wheel for sub modules of HEC core with clock gating

Implemented HEC core using i) conventional driving elements ii) modified driving elements and employed clock gating technique. In both the cases power consumption and delay reduced.

VI.CONCLUSIONS

The designed CPU, embedded controller called as soft processor is built using FPGA's general purpose logic. PEC core offers many exceptional advantages compared to typical hard processors or controllers: It has complete flexibility to select any combination of peripherals based on the application, with user defined/designed peripherals being easily attached, Improves system's interface capabilities, the multiple components can be replaced with a single FPGA, design time and cost also less, An FPGA PEC core has the ability to make tradeoffs between hardware and software to maximize efficiency and performance.

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