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Implementation and Analysis of Sign Extension and Baugh WOOLEY Multiplier in Ant Architecture

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***Abstract:*--Multiplier is the most crucial part in any digital signal processing (DSP) system applications. Designing a reliable multiplier in the deep submicron era is a challenging task. Deep sub micron technology needs low power, high signal to noise ratio, reliability and etc. There exists always a trade of between low power and reliability. The approach in this paper is to compromise both the reliability and low power in designing a multiplier. This paper deals with, implementation of reliable low power multiplier for signed bits and performance analysis of sign extension and Baugh wooley multipliers in ANT (Algorithmic Noise Tolerant) architecture with fixed width RPR block.**

Keywords:—ANT architecture, Sign Extension Multiplier, Baugh Wooley multiplier.

I. INTRODUCTION

Now a day's low power circuits are developing very rapidly. These low power circuits are using in many applications such as digital signal processing systems and etc. Hence digital signal processing systems also need to achieve low power consumption. The vital part in DSP system is multiplier. By improving the qualities of this multiplier will improve the quality of DSP system. In order to design low power digital signal processing systems design low power multipliers required to design. To achieve this low power present techniques are clock gating, voltage over scaling, multi threshold and etc[1]. In these techniques voltage over scaling is aggressive technique to reduce the power consumption [2]. In CMOS the dynamic power is directly proportional to the square of the supply voltage[3]. By reducing the supply voltage the power consumption of the circuit will be reduced.

$$P_D = V_{DD}^2 .C. F \quad ... (1.1)$$

In voltage over scaling (VOS) the supply voltage is reduced beyond the critical voltage without scarifying the throughput to achieve low power consumption. In VOS critical path delay of the system becomes greater than the sampling period of the system. Due to this some input dependent soft errors will occur. This causes severe degradations in signal to noise ratio. To minimise these soft errors, ANT (algorithmic noise tolerant) architecture was implemented in this paper.

Fixed width RPR block was used in ANT architecture and unsigned Baugh wooley multiplier was designed [4]. In this paper signed Baugh wooley multiplier and sign extension multiplier was implemented for 12x12 bits and the performance was analysed.

II. ANT ARCHITECTURE

In ANT architecture there will be two blocks. One is main DSP block and other is EC (error correction) block. The error correction block was composed of other blocks such as RPR (reduced precision replica redundancy) block, comparator and multiplexer. The RPR block is same as the main block but with reduced precision. There will be two ways to implement this RPR block. One is full width and other is fixed width multiplier. In this paper fixed width multiplier was implemented. Fixed width multiplier means cutting of n-bit LSB bits of final output. Due to this round off error will occur. To minimise this round off error compensation circuit will be implemented. There are mainly two types in designing the compensation circuits. One is by using constant correction value and other is by using variable correction value. Even though compensation circuit by using variable correction value has more area and power consumption it was used in this paper due to it's high efficiency.

The main block and the RPR block have same input. The output of the main block is $Y_a[n]$ and the output of RPR block is $Y_r[n]$. These two are compared with comparator to reduce the errors. If the comparator value is

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greater than the threshold value then RPR block's output is the final output else main block's output is the final value. Selection of the final output will be carried by a 2x1 multiplexer. Comparator value is greater than the threshold value means error was presented in the main block's output.

$$Y[n] = \begin{cases} Y_a[n], & \text{if } |Y_a[n] - Y_r[n]| \le Th \\ Y_r[n], & \text{if } |Y_a[n] - Y_r[n]| > Th \end{cases} \quad \text{... (2.1)}$$

'Th' is calculated as

$$Th = \max_{\forall inputs} |Y_a[n] - Y_r[n]| \quad \text{... (2.2)}$$

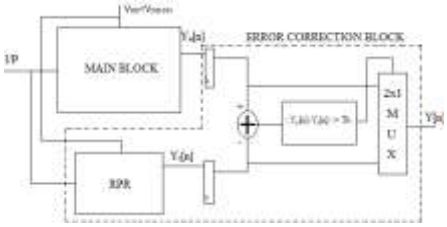

Figure 2.1: ANT architecture

2.1 Main Block

The main block was implemented with two techniques in this paper. They are sign extension multiplier and baugh wooley multiplier. Sign extension multiplier was considered as the conventional method to multiply two sign bits. Baugh wooley was the advanced technique compared to sign extension. To multiply two sign bits in sign extension method there are three important steps to consider. First one is extend the sign bit in each and every row upto $2n^{th}$ position(here n is the number of bits). Second one is invert all the bits in the last row of partial product. Third one is add logic 1 to the LSB of the last row.

To multiply two sign bits by using baugh wooley multiplier there will be three main steps to consider. First one is complement the MSB partial product in every row ecxept the final one. Second one is complement all the partial products except MSB in the final row and add the logic one at n^{th} position in the first row. Finally invert the MSB of final product result. The below 4x4 multiplication table shows the sign extension method of multiplication. This can be extended to 12x12 .

A3 A2 A1 A0

B3 B2 B1 B0

A3B0 A3B0 A3B0 A3B0 A3B0 A2B0 A1B0 A0B0

A3B1 A3B1 A3B1 A3B1 A2B1 A1B1 A0B1

A3B2 A3B2 A3B2 A2B2 A1B2 A0B2

$\overline{A3B3}$ $\overline{A3B3}$ $\overline{A2B3}$ $\overline{A1B3}$ $\overline{A0B3}$

1

P7 P6 P5 P4 P3 P2 P1 P0

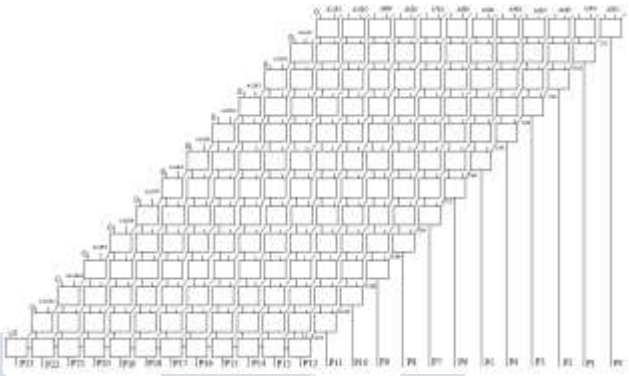

Figure 2.2: 12x12 Baugh Wooley multiplier

2.2 RPR Block

RPR block is the most important in entire ANT architecture. It has to be designed with low precision operands and fixed width hence n-bit left most bits in the final output are truncated. Due to the truncation of the n-bit left most bits round of error will be occured. To minimise this round of error variable correction value method is used in this paper. Binary code ia a weighted code hence each bit in binary has a particular weight. MSB has the highest weight and LSB has lowest weight. The weight will be reduced from MSB to LSB. So, in the truncated n-bit LSB, $(n-1)^{th}$ bit weight will be more. In variable correction value method, the $(n-1)^{th}$ bit column is directly injected into the n^{th} bit column hence maximum error will be reduced. If the value of the $(n-1)^{th}$ bit was logic 0 and the $(n-2)^{th}$ bit value is logic 1 then the round of error will be not reduced. To further reduce the error one logic was implemented to know the values of $(n-1)^{th}$ bit and $(n-2)^{th}$ bit. If the value of the $(n-1)^{th}$ bit was logic 0 and the $(n-2)^{th}$ bit value is logic 1 then logic 1 will be added to the n^{th} bit column. By implementing this logic maximum error due to round off will be eliminated. The $(n-1)^{th}$ bit column is called ICV (Input Correction Vector) and $(n-2)^{th}$ bit column is called MICV (Minor Input Correction Vector) as shown in figure.

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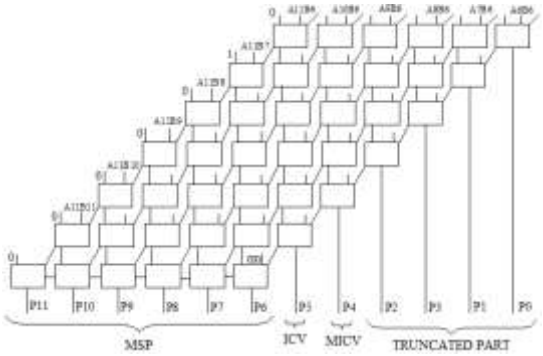

Figure 2.3: Fixed width RPR with error compensation

The input correction vectors are A11B6, A10B7, A9B8, A8B9, A7B10 and A6B11. The minor input correction vectors are A10B6, A9B7, A8B8, A7B9 and A6B10. To find the value of cm (shown in above figure) firstly apply all the input correction vectors to NOR gate and then apply the all minor input correction vectors to OR gate. Then apply these two gates output to AND gate. To generate the value of cm apply the AND gate output and A6B11 combinely to OR gate.

III. RESULTS

Waveforms of both the Sign extension multiplier and Baugh wooley multiplier in the ANT architecture are presented here. The synthesis reports for both the implementations are shown in tables through 3.1 through 3.3.forall the three performance metrics viz., power,area and delay. These synthesis reports are generated with the help of synopsis 'design complier' tool and 'saed90nm' library files.The performance analysis of Sign extension multiplier and Baugh wooley multiplier in the ANT architecture are shown in the graphs through figure 3.3 through figure 3.6

Table3. 1: Area report

Parameter	Sign Extension	Baugh wooley
Combinational area(nm)	12871.98	8576.40
BUF/INV area(nm)	222.10	222.71
Net interconnect area(nm)	647.93	380.48
Total cell area(nm)	12871.98	8576.40
Total area(nm)	13519.92	8956.89

Table 3.2: Power report

Parameter	Sign Extension	Baugh Wooley
Cell internal power(mW)	1.094	0.801
Net switching power(μW)	251.97	195.24
Total dynamic power(mW)	1.34	0.996
Cell leakage power(μW)	45.26	29.89
Total power(mW)	1.39	1.02

Table 3.3: Comparision of power area and timing

Parameter	Sign Extension	Baugh Wooley
Timing(ns)	292.83	153.70
Power(mW)	1.39	1.02
Area(nm)	13519.92	8956.89

The below shown waveforms are generated using synopsis 'verilog compiler and simulator' tool.

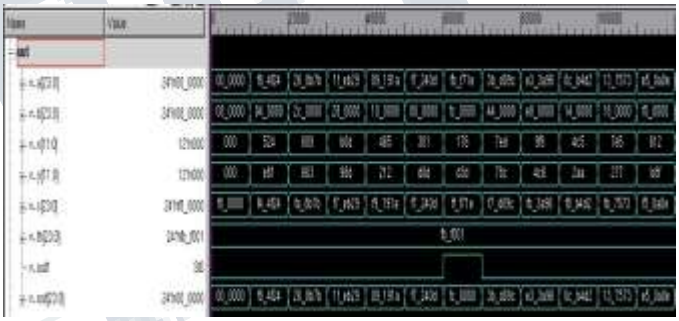

Figure 3.1: output waveforms for Baugh wooley 12x12 multiplier in ANT architecture

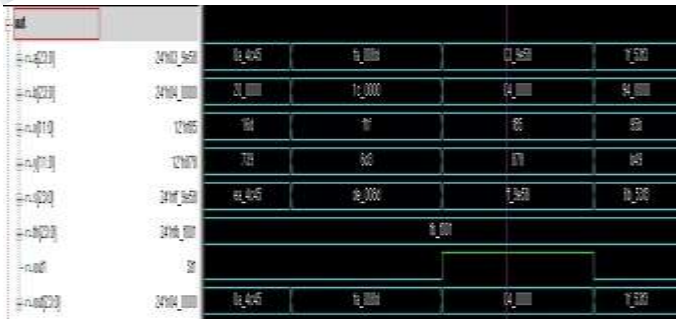

Figure 3.2: output waveforms for Sign extension 12x12 multiplier in ANT architecture.

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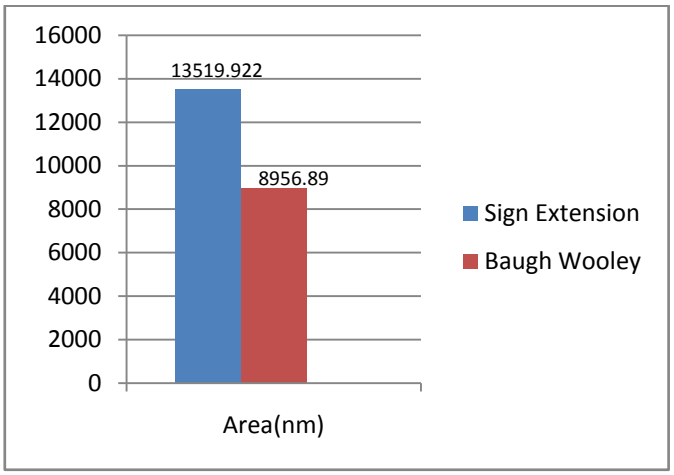

Figure 3.3: Bar chart analysis to compare area of both the Sign extension and Baugh wooley methods.

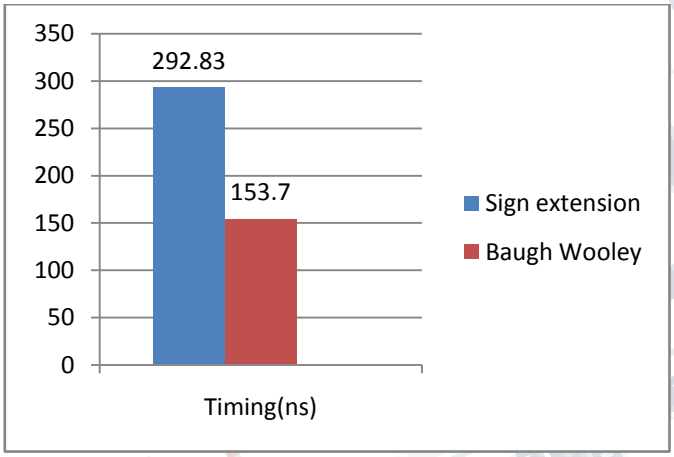

Figure 3.4: Bar chart analysis to compare timing of both the Sign extension and Baugh wooley methods.

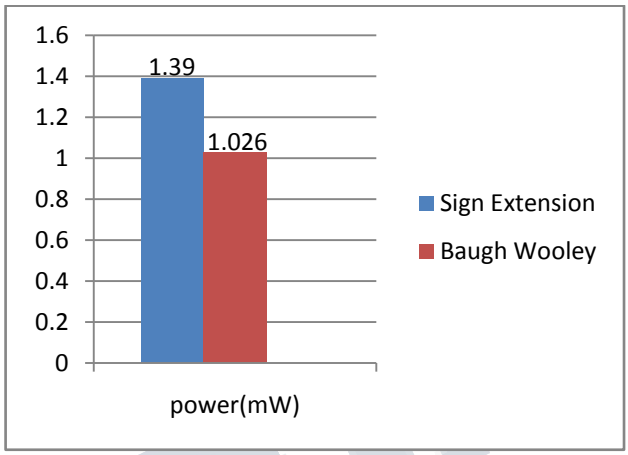

Figure 3.5: Bar chart analysis to compare power of both the Sign extension and Baugh wooley methods.

IV. CONCLUSION

The signed Baugh wooley multiplier and sign extension multiplier was implemented for 12x12 bits.From the results it is concluded that the performance of Baugh wooley 12x12 multiplier is better when compared to thesign extension multiplier in all the three aspects viz., power, area and delay.The results shows that,Baugh wooley multiplier consumes 26.1% less power, 33.7% less area and it reduces the delay by 47.5%when compared to thesign extension multiplier.

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