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# Low Power and High performance JK Flip - Flop using 45 nm Technology

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***Abstract:*** **-- In current scenario, VLSI circuit's greatest challenges is to reduce the power dissipation and surface area so that longer life and high performance achieved to greater extent. The key parameter is threshold voltage to reduce the leakage power. In our proposal, we design low power and high performance JK flip-flop. JK flip-flop is designed with the help of D flip-flop and with some logic gates. The proposed work is mainly of double gate MOSFET (DG MOSFET) concept and transistor stacking method is used to reduce power dissipation and delay. This circuit is examined some parameter like power dissipation, delay and power delay product (PDP).Some Simulation like Tanner EDA tool and a 45 nm technology shows that the proposed JK flip-flop has lower power dissipation and small delay comparable to those of published an explicit-pulsed double-edge triggered JK flip-flop (EP-DET-JKFF). In this circuit we observe the power dissipation decreases 21.87%. An improvement of 46.24% in PDP in JK flip-flop as compared to explicit-pulsed double edge triggered JK flip-flop.**

***Index Terms*:—JK Flip flop, MOSFET, Edge triggered Flip flop Transistor Stacking.**

## I. INTRODUCTION

In the world of technology, electronics begin to consume more and more power. So power dissipation problem becomes complicated for both the industry and academic field. The devices like palmtop, cellular and mobile phones have been increased due to designing of low power VLSI circuit. Scaling of the device is needed to increase the density of the chip. There are a number of problems like leakage current, short channel effects (SCE's) and drain induced barrier lowering (DIBL) effect which lags the performance of the circuit. So there is a need of improved device structure having higher performance in nanometer range of operation. Due to increasing trend of various leakage current power consumption in Nano-scaled device is outreach the startling state.

Along with dynamic power, leakage power has turned out to be a major contributor to the overall power dissipation in VLSI circuits. Leakage power of a CMOS transistor depends on gate length and oxide layer thickness. Double gate MOSFET has such potential because of its scalability in Nano circuit. Double gate MOSFET finds the huge application in ultra-low power design. It consists of drain, source and two gates. Electrical coupling is used to couple two gates (front and back) in double gate devices. The conducting channel in double gate MOSFET is surrounded by gate electrode on either side. This assures that no part of channel is far away from a gate electrode.

Double-gate devices with isolated gates (independent gates) are being developed. This independent gate option will provide the low power and mixed signal applications for the circuit designer. Such developments at the device level provide opportunities for new ways of circuit design for low power and high performance. ITRS (International Technology Roadmap for Semiconductor) reports also show the inexorable admittance of double-gate MOSFET.

## II. TRANSISTOR STACKING

The natural stacking of MOSFET helps in reducing the leakage current in CMOS circuit. The leakage through two series OFF transistor is much lower than that of single transistor because of stack effect. An effective way to reduce leakage power in active mode is stacking of transistor. When more than one transistor is in series in a CMOS circuit, the leakage current has strong dependence on the number of turned off transistor, this is known as stack effect. Leakage current decreases with an increasing number of OFF transistors in stack technique as shown in Fig1.1.

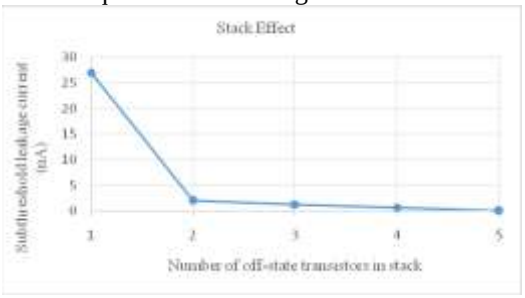

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***Fig.1 Stacking Effect***

This paper is organized into five sections. Section 1 give the general information for low power designing, introduce DG-MOSFET device and transistor stacking. Section 2 illustrates the existing single gate based an explicit-pulsed double-edge triggered JK flip-flop. In section 3, JK flip-flop using DG-MOSFET and transistor stacking method has been proposed. Simulation, results and comparison are given in Section 4 and finally Section 5 concludes the paper.

## III. DESIGN OF EXPLICIT-PULSED DOUBLE-EDGE TRIGGERED JK FLIP-FLOP

The JK flip-flops can be constructed with D flip-flops and some logic gate circuits. Fig.2 illustrates a general method for transferring D flip-flops into JK flip-flops.Fig.3 shows the schematic of an explicit-pulsed double-edge pulse-triggered JK flip-flop. When the clock pulse is 1 and q = 0, J = 1, and K = 0, transistor NMOS_1, NMOS_2 and NMOS_5 are ON and the transistor NMOS_3 and NMOS_4 are OFF then node X is pull-down to zero through NMOS_1, NMOS_2 and NMOS_5 results in PMOS_2 is ON. The final output q is pull-up to one. When clock pulse is one and q = 1, J = 0 and k = 1, transistor NMOS_3, NMOS_4 and NMOS_5 are ON and the transistor NMOS_1 and NMOS_2 are OFF.

The node X will remain in previous state and final output q is pull-down to zero. When clock pulse = 1, J = 0, and K = 0, transistor NMOS_1, NMOS_3 and PMOS_1 is OFF. The discharge path of node X is disconnected, results in PMOS_2 is OFF, due to this pull-up and pull-down path of final output q is disconnected and final output q remains in previous state. When clock pulse = 1, J = 1 and K = 1 and previous output q = 0, the transistor NMOS_1, NMOS_2 and NMOS_5 are ON and transistor N4 is OFF.

The node X is pull-down to zero through NMOS_1, NMOS_2 and NMOS_5 are ON results in PMOS_2 is ON and the final output q is pull-up to one. When clock pulse is zero, the transistor PMOS_1 is ON and NMOS_5 is OFF. The node X is pull-up to one results in PMOS_2 is OFF. The final output q and q bar remains in previous state. The above analysis describes the function of pulsed JK flip-flop.

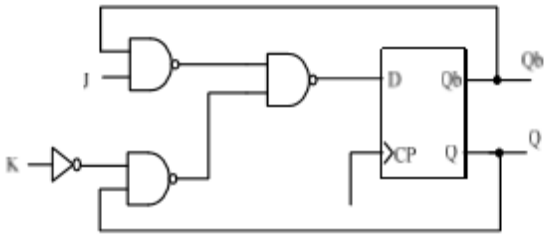


***Fig.2 Schematic of JK flip-flops based on D flip-flops***

Earlier work has been done at 0.18 technology in which the power dissipation and delay was more. To overcome these limitations the proposed work has been done at 0.045 technologies and it has been analyzed that power dissipation and delay reduced by 21.87 % and 31.18 % respectively.

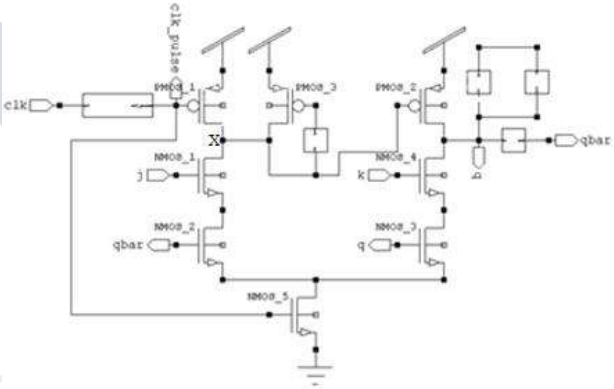


***Fig.3 Schematic of an explicit-pulsed Double-edge pulse-triggered JK flip-flop***

## IV. JK FLIP-FLOP CIRCUIT USING DOUBLE GATE MOSFET

The proposed design for JK flip-flop is given in Fig.4. The circuit comprises of D flip-flop and some logic gates (NAND and NOT gate).The NAND and NOT gate is designed using double gate MOSFET. The JK flip-flop circuit using double gate MOSFET is shown in Fig.4. The double gate MOSFET may be constructed by connecting two single gate MOSFET transistors in parallel in such a way that their source and drain are connected together. The two gates in DG-MOSFETs lead to increased current driving capability of transistor. The DG-MOSFET structure provides electrostatic coupling for conduction channel and two gates allows

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additional gate length scaling by factor of 2 as compare to the single gate MOSFET.

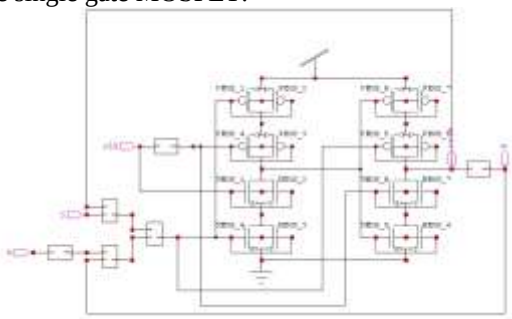

*Fig.4 Schematic of proposed JK flip-flop*

## V. SIMULATION AND RESULTS HELPFUL HINTS

The simulations of proposed circuit have been done at 0.045µm technology using level-54. The output waveforms of proposed circuit have been shown in Fig.5.The simulation results were obtained from tanner EDA tool using typical models of a 0.045µm CMOS technology at room temperature with VDD =1.1Volt and clock frequency of 50MHz.

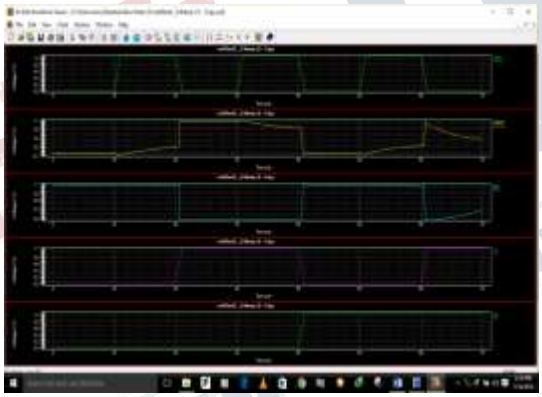

*Fig.5 Simulation output waveform of proposed JK flip-flop*

Table 1 shows the comparison on the basis of power dissipation, delays and transistor count of an explicit-pulsed double edge triggered JK flip-flop (EP-DET-JKFF) and proposed JK flip-flop at 0.045. The power dissipation metric for flip-flops is average power dissipation. As shown in Table 1, proposed JK flip-flop exhibits an improvement of 46.24% in PDP as compared to explicit-pulsed double edge triggered JK flip-flop. The proposed design has 26 transistor counts while explicit-pulsed double edge triggered JK flip-flop has 31 transistor counts with pulse generator included. The proposed design shows 21.87% power saving as compared to previous design.

***Table 1 Comparison between EP-DET-JKFF and proposed JK flip-flop***

| | Average power dissipation (µw) | Transistor count | Delay (ns) | PDP (fJ) |
|---|---|---|---|---|
| JKFF | 7.441 | 31 | 28.54 | 212.366 |
| Proposed JKFF | 5.813 | 26 | 19.64 | 144.167 |

## VI. CONCLUSION

An explicit-pulsed double edge triggered JK flip-flop and JK flip-flop using double gate MOSFET (DGMOSFET) circuit has analyzed for various parameters. T-Spice simulation results shows that the power dissipation and delay of JK flip-flop using double gate MOSFET as compared to an explicit-pulsed double edge triggered JK flip-flop is reduced. Simulation result shows 21.87% power saving in proposed design. Proposed JK flip-flop exhibits an improvement of 46.24% in PDP as compared to explicit-pulsed double edge triggered JK flip-flop. In future, newly emerging leakage power reduction techniques at block level and gate level abstractions are expected to give more power savings than the existing circuit level technique.

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