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Design and Development of Bi-Phase Coded RF Signal Generator for Atmospheric Radars

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***Abstract:* -- The aim of the present work is to design and develop an RF Exciter in the VHF band frequency. The exciter provides pulse modulated Bi-phase coded RF signal at 53 MHz frequency. And it generates highly coherent Receiver local oscillator signal, as well as required auxiliary clock signal for synchronizing operations of all the sub-systems of the radar. The spectral performance of the 53MHz RF signal is achieved via use of quartz crystals in the Master Oscillator, and a variety of recently developed circuit technologies and frequency synthesis techniques.**

***Index Terms*: - OCXO, PLO, Bi-Phase Coder, Amplifier, T/R Switch**

I. INTRODUCTION

The global atmosphere, by virtue of its composition, controls the temperature and provides a shielding effect from harmful radiations, thus making life, exist on earth. Atmosphere affects the life on earth through various meteorological phenomena such as winds, precipitation and storms. Radars are used to find out all these changes in the atmosphere, and to predict the behavior of the it through modeling.

Radar is an electromagnetic system for the detection and location of objects. It operates by transmitting a particular type of RF signal, a Bi-phase coded pulse-modulated sine wave for example, into a specific volume of space to detect for targets. If the transmitted electromagnetic wave encounters sudden change in conductivity **σ**, permittivity **ϵ** or permeability **μ** in the medium, a part of the electromagnetic energy gets absorbed and is re-radiated. This sudden change in the electrical property of the medium constitutes the target. The re-radiated signal on being received back at receiver gives information about the location of the target. The location of the target includes range, angle and velocity. The range is the distance of the target from radar station, the angle could be azimuth or elevation angle for static targets, and velocity for moving targets. If relative motion exists between target and radar, the shift in the carrier frequency of the reflected wave is a measure of target's relative radial velocity and may be used to distinguish moving targets from stationary objects.

The Indian MST Radar (Mesosphere – Stratosphere –Troposphere Radar) - at National Atmospheric Research Laboratory, (Gadanki 13.47 N, 79.18 E) - is a high power VHF phased array radar operating at 53MHz in coherent backscatter mode with peak power aperture product of $3x10^{10}$ Wm^2.The MST radar is a pulsed Doppler radar to support the atmospheric research in the MST regions. In order to study the atmospheric parameters like temperature, humidity, wind speed and direction etc., precisely, the radar needs a signal generator with very low phase noise and with very high short term and long term stabilities. The exciter generates pulse modulated Bi-phase coded RF signal for operation of the radar at 53MHz frequency.

II. DESCRIPTION OF THE SYSTEM

The functional block diagram of the signal generator unit is shown in the fig-1. It comprises of oven controlled crystal oscillator (OCXO) , SPDT switch, Wilkinson Power Divider, Phase Locked Oscillator, Pulse modulator, Bi-phase coder, Band Pass Filter, Amplifier , and T/R Switch.

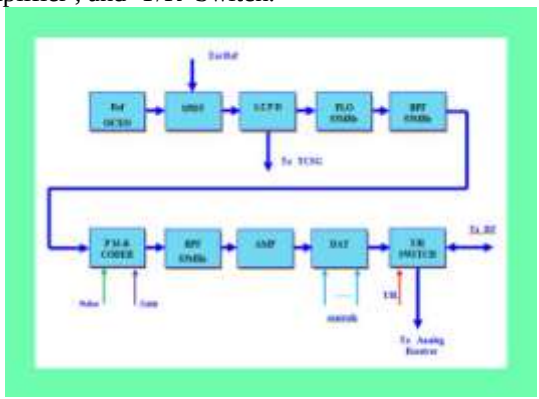

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Fig:1 Functional block diagram of the Signal Generator

Oven Controlled Crystal Oscillator

The reference **OCXO** master oscillator generates the 10 MHz sinusoidal signal with very low phase noise, that is about -145 dBc/Hz. This signal is used as the reference clock for phase synchronization of all the sub-systems of the radar, like TCSG (Timing and Control Signal Generator). It provides very high short term and long term frequency stability. The oscillator output signal parameters were measured in a spectrum analyzer and practically observed that the peak power level is about 5 dBm, and the second harmonic level is about -39.8 dBc as shown in the fig-2.

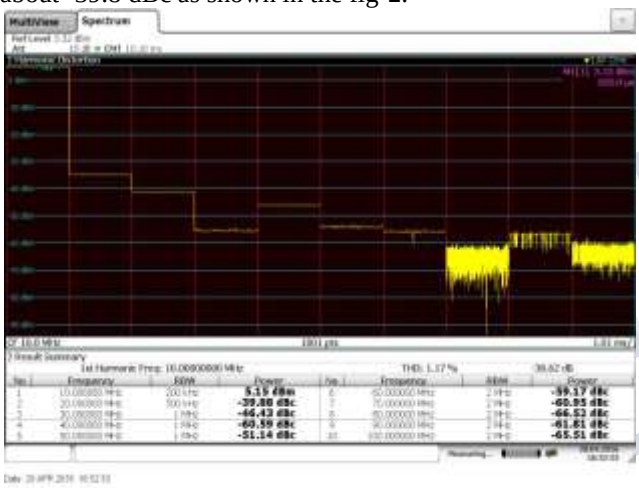

Fig:2 Peak power and harmonic levels of the oscillator

Leeson's equation is an empirical expression to measure phase noise, that describes an oscillator's phase noise spectrum. Leeson's expression[1] for single-sideband (SSB) phase noise in dBc/Hz is

$$L(f_m) = 10\log\left[\frac{1}{2}\left(\left(\frac{f_0}{2Q_l f_m}\right)^2 + 1\right)\left(\frac{f_c}{f_m} + 1\right)\left(\frac{FkT}{P_s}\right)\right]$$

Where f_0 is the output frequency, Q_l is the loaded Q, f_m is the offset from the output frequency (Hz), f_c is the $1/f$ corner frequency, F is the noise factor of the amplifier, k is Boltzmann's constant, in Joules/Kevin , T is absolute temperature in Kelvins, and P_s is the output power.

The measured phase noise of the oscillator in the spectrum analyzer is about -145 dBc/Hz at 10 KHz offset frequency. The screenshot of the same is shown in the fig-3.

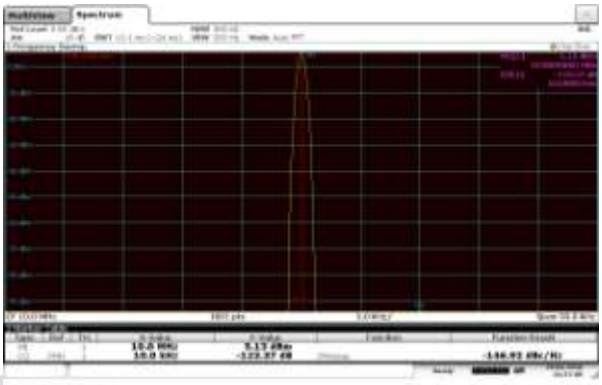

Fig:3 Phase noise of the oscillator

SPDT switch

A **Single Pole Double Throw switch** was used **to** synchronize to the radar exciter to the external clock reference signal. This external reference clock signal state in the SPDT would be used, to inject the simulated pulsed RF signals in the transmit path, for calibration of the radar, and to conduct some kind of special experiments like Spaced Antenna mode. The **HMC349AMS8G** component was used to implement SPDT switch. The switching speed of the component is 60 n sec, and it has a 0.8 dB insertion loss. It provides a great isolation that is about 70 dB between the two states (ON/OFF). A TTL control signal is required to alter the state of the switch.

Wilkinson's Power Divider

The 10 MHz signal being generated by the OCXO was divided into two equal power levels by developing a Wilkinson's Power Divider. It consists of two quarter wave (**λ/4**) transmission lines which were designed with lumped elements. The signal emerging at 'port 2' of the power divider was used as input reference signal for 53 MHz synthesizer, and the signal coming out at 'port 3' was used as clock for the Timing and Control Signal Generator. An ideal 1:2 Wilkinson power divider yields **$S_{21} = S_{31} = -3$ dB**. But practically it has 0.5 dB insertion loss, hence the total signal power level at each port is about -3.5 dB. The simulated and measured return loss is about -27dB at each port that is,

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(S_{11}) = (S_{22}) = S_{33}) = 27 dB at 10 MHz frequency.

The distribution loss at each port of 1:N Wilkinson power divider can be calculated as

$10 \log_{10} (1/N)$

Where 'N' is the number of ports required to split/combine the signal

The implementation of the Wilkinson power divider was done with lumped elements L and C, and their values are calculated by using the below formulae. The same calculated values were used in the ADS simulation as shown in fig-4a & 4b.

$$L = \frac{\sqrt{2}\ Zo}{2\pi f} = 1.6\ uH \quad \text{and}$$

$$C = \frac{1}{2\pi f\ \sqrt{2}\ Zo} = 159\ pF$$

where Z_0 in the above equations

$$= Z\frac{\lambda}{4} = \sqrt{Zin\ .\ ZL} = \sqrt{50\ .\ 100} = 70.71\ \Omega$$

The practically measure isolation between the port 2 and port 3 is about 29dB

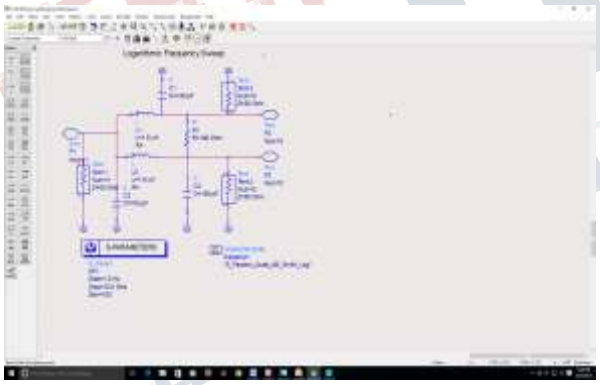

Fig: 4a Wilkinson power divider circuit diagram

Fig: 4b ADS simulation results of Wilkinson power divider

Phase Locked Oscillator

The basic block diagram of the phase locked loop is connected as shown in the fig-5. The reference signal and the signal from the voltage controlled oscillator are connected into the phase detector. The output from the phase detector is passed through the loop filter and then applied to the voltage controlled oscillator.

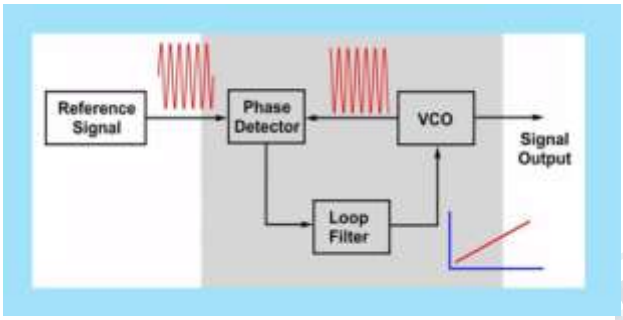

Fig: 5 Basic block diagram of PLL

The Voltage Controlled Oscillator, VCO, within the PLL produces a signal which enters the phase detector. Here the phase of the signals from the VCO and the incoming reference signal are compared and a resulting difference or error voltage is produced. This corresponds to the phase difference between the two signals. The functional block diagram of the PLL is shown in the fig-6.

The error signal from the phase detector passes through a low pass filter which governs many of the properties of the loop and removes any high frequency elements on the signal. Once through the filter the error signal is applied to the

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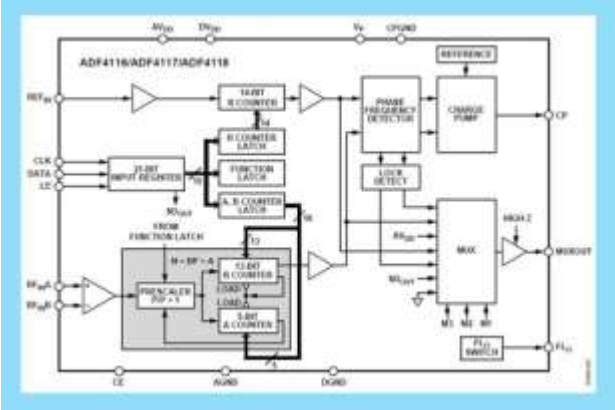

Fig: 6 Functional block diagram of PLL

Control terminal of the VCO as its tuning voltage. The sense of any change in this voltage is such that it tries to reduce the phase difference and hence the frequency between the two signals. Initially the loop will be out of lock, and the error voltage will pull the frequency of the VCO towards that of the reference, until it cannot reduce the error any further and the loop is locked. When the phase locked loop, is in lock a steady state error voltage is produced. By using an amplifier between the phase detector and the VCO, the actual error between the signals can be reduced to very small levels. However some voltage must always be present at the control terminal of the VCO as this is what puts onto the correct frequency. The fact that a steady error voltage is present means that the phase difference between the reference signal and the VCO is not changing. As the phase between these two signals is not changing means that the two signals are on exactly the same frequency.

During the practical implementation of the Phase Locked Oscillator, the 10 MHz signal emerging at 'port 2' of the power divider is connected as the input reference signal for the PLO. Then the PLO generates the required 53 MHz RF signal which has the same phase as compared to the reference signal. The 53 MHz RF signal is then amplified with GALI- 6 amplifier, and then it is being divided into two equal power levels by using Wilkinson power divider. During the process of frequency synthesis, some unwanted frequency components were produced. Hence in order to select the required 53 MHz frequency component, a Band Pass Filter is used. The 53 MHz RF signal, at 'port -2' of the power divider is connected to the pulse modulator, and the signal at 'port-3' would be used as the Local oscillator signal for the Receiver. The PLO was practically implemented with **ADF4118** frequency synthesizer component, and it is shown in the fig-7

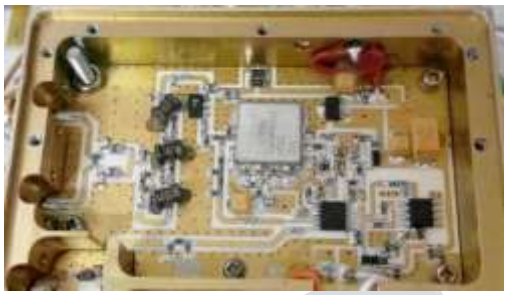

Fig:7 Phase Locked Oscillator

Pulse Modulator

The Pulse Modulator implementation was done by using an RF switch. For getting pulse modulation, the 53 MHz continuous RF signal is passed through an RF switch and making it 'ON' for the required time period and 'OFF' for the rest of the time. This was build up with **HMC349AMS8G** component to give better ON/OFF ratio of the pulse modulated RF signal. The ON/OFF ratio can be calculated by using the below formula for the 50 Ω system.

$$P_{dBm} = 10 \log_{10} (V^2 / 400)$$

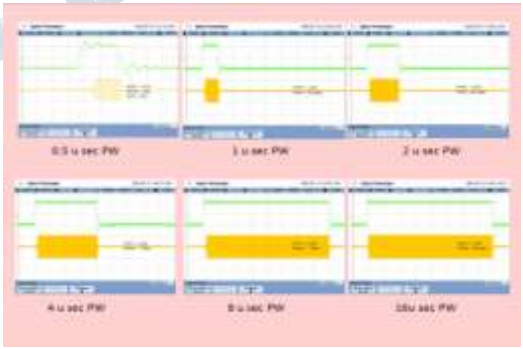

Fig 8 : Pulse modulator output for different pulse widths

The measured rise and fall times of the modulator is about 100 n sec, and this has been measured for different pulse widths i.e., from 0.5 u sec to 64 u sec as shown in the fig-8.

Bi-Phase Coder

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Bi-phase coder plays an important role in the exciter. It's main function is to alter the phase of the RF signal. This phase change is done by multiplying the pulse modulated RF signal with the code pulse. In this process of multiplication, the phase of the RF signal 'will not be changed (0°)' when the code pulse transition takes place from logic zero level to logic 1 level .Whereas, the phase of the RF signal 'will be changed (180°)' when the code pulse transition takes place from 'logic 1' level to 'logic zero' level.

In order to develop this circuit, a phase shifter is designed for 53 MHz RF signal, and an SPDT switch (ADG 936) was chosen, as it contains two independently selectable SPDT's. Both CMOS and LVTTL control inputs are compatible to select/deselect the switch. Phase shifter implementation was done with π-type, low pass filter to generate 90º phase shift at 53MHz, and two such π-sections are cascaded to get a total of 180° phase shift. The lumped elements L and C calculations for the phase shifter design were done by using the below formulae.

$$L = Z_0 \frac{\sin \emptyset}{2\pi f} = 150.3 \text{ nH}$$

$$C = \frac{1-\cos \emptyset}{2\pi f \ Z0 \ \sin \emptyset} = 60 \text{ pF}$$

ADS simulations were done with the same L and C calculations for the design of the phase shifter, before going to implement the hardware. During the simulation, it is observed that the insertion loss is about -4 dB as shown in the below fig-9a & 9b.

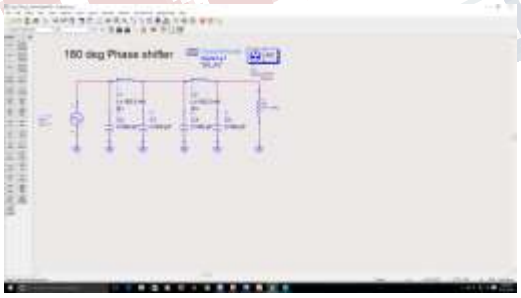

Fig:9a circuit diagram of 180^0 phase shifter

Fig:9a ADS simulation results of 180^0 phase shifter

The hardware implementation of the Bi-phase coder is shown in the fig-10. The output of the Pulse modulator, i.e., 53 MHz pulsed RF signal is given as the input to the coder, then the coder provides the Bi-phase coded RF pulse, which is the required signal for the operation the Radar.

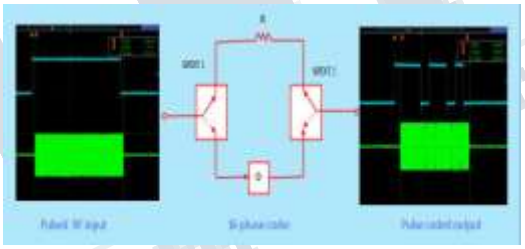

Fig:10 Hardware

Amplifier

In order to raise the signal strength to the required power level, a linear amplifier is used, which is implemented with GALI 74+ component. The noise figure of this amplifier is 2.7 dB. The circuit diagram of the amplifier is shown in the Fig-11. Its linear response characteristics measurements are tabulated as shown in the table-1.

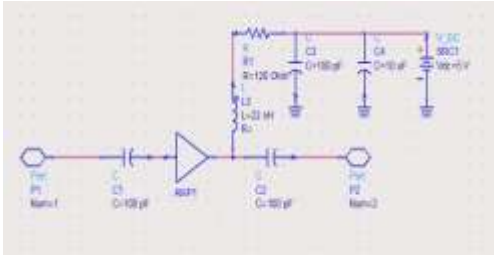

Fig:11 Amplifier circuit diagram

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Table: 1 Linear characteristics of the amplifier

SL NO	Input power level in dBm	Output power level in dBm
1	-110	-83.5
2	-100	-73.5
3	-90	-64.1
4	-80	-54.4
5	-70	-44.4
6	-60	-34.5
7	-50	-24.5
8	-40	-14.5
9	-30	-4.49
10	-25	+0.51
11	-22	+3.5
12	-21	+4.5
13	-20	+5.5
14	-19	+6.5
15	-18	+7.5
16	-17	+8.5
17	-16	+9.5
18	-15	+10.5
19	-14	+11.36
20	-13	+12.29
21	-12	+13.18
22	-11	+13.9
23	-10	+14.89
24	-9	+15.88
25	-8	+16.5
26	-7	+16.89
27	-6	+17.3
28	-5	+17.79
29	-4	+18.0
30	-3	+18.3
31	-2	+18.4
32	-1	+18.5
33	0	+18.58

Phase Shifter

A 5-bit digital attenuator was used to control the output power level of the amplifier, and it was implemented with HMC539LP3 component. This component provides a total of 7.75 dB attenuation. The various attenuation ranges can be selected are 0.25, 0.5, 1, 2, and 4 dB. In order to apply attenuation in the RF path, it is required to select that particular pin on the component with the help of TTL control signals. The pin diagram and the circuit diagram of the attenuator is shown in the fig-12.

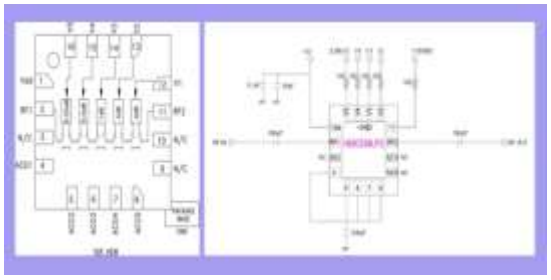

Fig: 12 5-bit Digital Attenuator

Band Pass Filter

A **band-pass filter** is a device that passes frequencies within a certain range and rejects (attenuates) frequencies outside that range. An ideal band pass filter would have a completely flat pass band with no gain/attenuation, and would completely attenuate all frequencies outside the pass band. In practice, no band pass filter is ideal. The filter does not attenuate all frequencies outside the desired frequency range completely The bandwidth of the filter is simply the difference between the upper and lower cut-off frequencies. A band-pass filter can be characterized by its Quality factor. The Q-factor is the inverse of the fractional bandwidth. A high-Q filter will have a narrow pass band and a low-Q filter will have a wide pass band.

The practical implementation of this Bessel type BPF was developed at 53MHz center frequency with the band width of 15MHz . It consists of parallel resonant L-C circuits coupled via series capacitors. This type of filter is very practical since all inductors are of same value. It has the insertion loss about -4dB, and the return loss is -33dB. BPF circuit simulations were done in the ADS. The circuit diagram and it's response are shown in the fig-13a & 13b respectively.

Fig: 13a BPF circuit diagram

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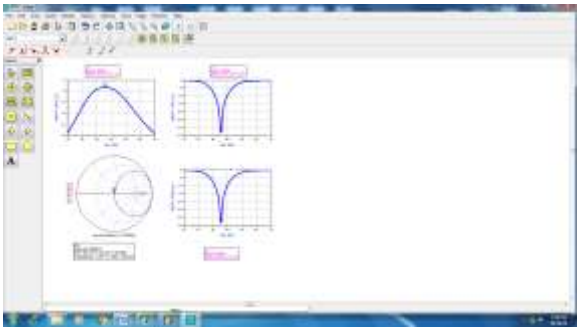

Fig: 13b ADS simulation results of BPF circuit

T/R switch

Transmit/Receive switch in the exciter is an SPDT switch, which was essentially used to isolate the transmitter and receiver, in order to avoid any small leakage entering into receive path. During the transmit period, the switch would be in ON state. In this period the output of the exciter would be connected to the input of the transmitter, while during the OFF state, the switch would be connected to the receiver. The default position of the switch is connected to receiver. The implementation of the switch was done with HMC349AMS8G, which has more isolation, that is about 70 dB. The block diagram of the switch is shown in the fig-14

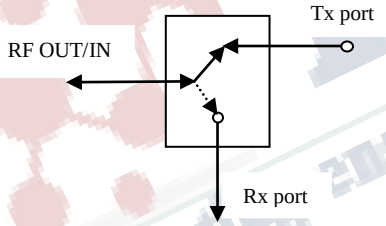

Fig:14 Block diagram of the T/R switch

RESULTS

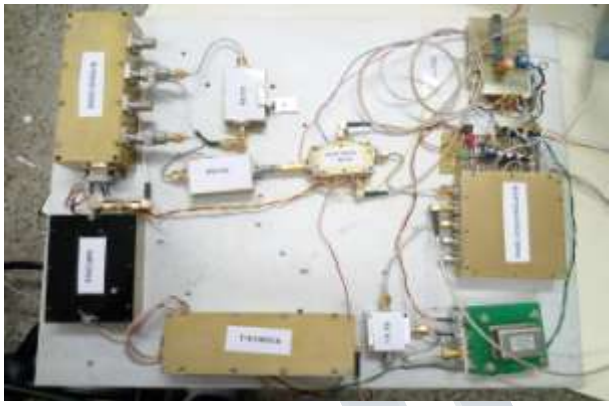

Fig: 15 Complete Signal Generator unit

Fig:16 Test set up

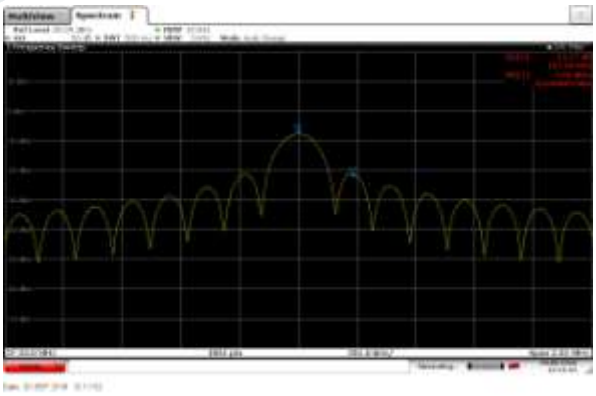

Fig:17 Power spectrum output for 8 u sec pulse width

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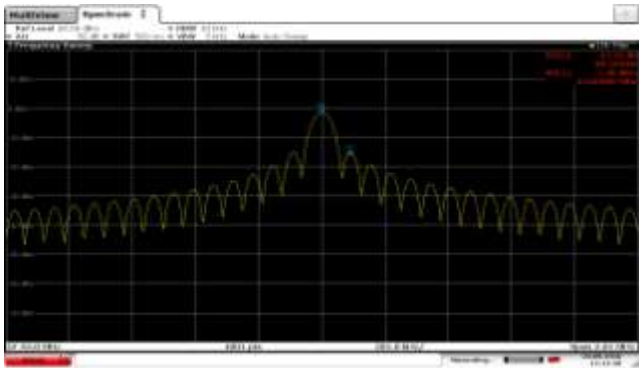

Fig:18 Power spectrum output for 16 u sec pulse width

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