ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
Vol 3, Issue 12, December 2016

Proposed FAM Unit with S-MB Techniques and Kogge Stone Adder using VHDL

[1]Dhumal Ashwini Kashinath , [2] Asst. Prof. Shirgan Siddharudha Shivputra
[1] [2] Department of Electronics and Telecommunication
[1][2] N. B. Navale Sinhgad College of Engineering, Kegaon,Solapur,India

***Abstract:*--This paper represent the high efficient design of Add-Multiply operator. The DSP applications requires the more number of add and multiplier operator .In this paper only concentration on how to reduce the Add-Multiply operator and increase the speed of the process .In the recent paper ,first addition of the two number and after convert into its Modified Booth (MB)form. It required more gates then performance decreases. But in this paper we take direct two number and given to the efficient recoding technique it generate MB form .The Booth algorithm required the adder but adder have number of types. If we use the Kogge stone adder bits size increase then the performance of adder also increase means whole system performance increase. Then compare the proposed system with existing system ,we get less gates and less combinational delays of the proposed system .**

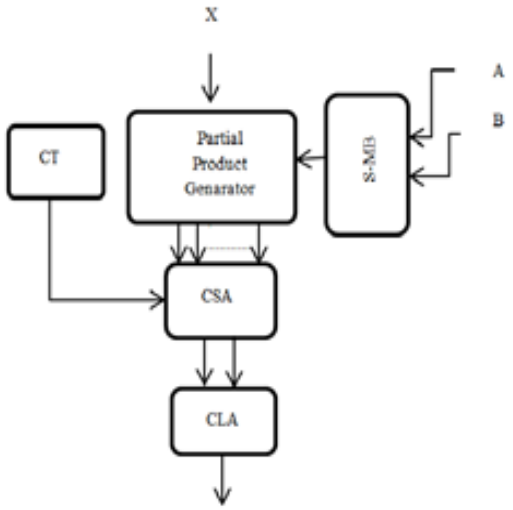
***Index Terms:*— Fused Add-Multiply Operator, Modified Booth Algorithm, S-MB Recoding Techniques, Kogge Stone Adder.**

I. INTRODUCTION

The basic building block in Digital Signal Processor (DSP) is multiplier. Multiplication is important arithmetic operation having huge application in DSP. Multipliers have large area, long latency and consume considerable power. Therefore, low-power and reduction of delay in the multiplier design has been an important part in VLSI system design. The research of this work is that optimization of FAM unit using the Kogge stone adder which produces more efficient solutions than existing techniques. The primary objective is power reduction with small area and delay overhead .By using new algorithms, different recoding techniques and Kogge stone adder it is even possible to achieve both power reduction and area/delay reduction, which is the strength of the optimization. For these requirements of smaller area occupation, less power consumption and faster operation, modified booth algorithm is practically used. For partial product generation, we propose a new modified Booth encoding (MBE) scheme to improve the performance of traditional MBE scheme.. This encoding algorithm also requires redundant partial product generation so called sign-extension. In this multiplication algorithm ,the operation is decomposed in a partial product summation .Each partial product represents a multiple of the multiplicand to be added to the final result. In the recent techniques , at the output the Carry-save adder (CSA) and Carry look-ahead, adder(CLA) is used so the gates has been increased but we use in this paper Kogge stone adder which reduces number of gates and delays. To optimize the design of fused add-multiply operators the direct recoding of the sum of two numbers in its Modified Booth (MB) form are applied. The direct recoding of the sum of two numbers in its MB form and Kogge stone adder gives an efficient implementation of the fused Add Multiply operator[1] [2]. In the Fig.1(a) shows the conventional method ,which provides direct recoding of the sum to its MB representation but it has correction term(CT), CSA and CLA adder which increases area and we get the output after long time so it has critical delay. In Fig. 1(b) shows the proposed system in which only one adder kogge stone adder used at final which reduces number of gates so the area and the hardware complexity will be decreased. In the conventional design of the AM operator (Fig.1(a)) uses first A and B inputs to an adder and then input X and the sum Y=A+B are given to the multiplier which gives Z . The drawback of the conventional design of AM unit which uses adders CLA and CSA which increases delay .To overcome this problem we optimize AM units with fusion of MB encoding unit and Kogge stone adder . In the optimized design of the AM operator(Fig.1(b)) , by direct recoding of the sum Y=A+B to its MB representation. The fused Add- Multiply (FAM) component contains only one adder at the end ,we know there is parallel adder. The result, we get significant areas are saved and the critical path delay of the recoding process is reduced. FAM Design is a new technique for direct recoding of two numbers in the MB representation of their sum.

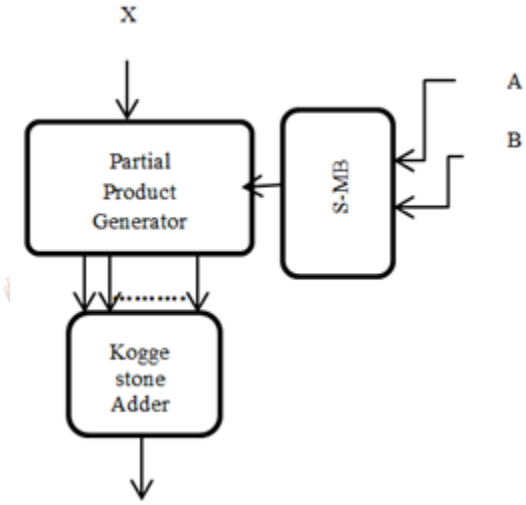
ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
Vol 3, Issue 12, December 2016



Z=X.Y=X(A+B)

Fig.1.(a) Conventional design of AM Operator.



Z=X.Y=X(A+B)

Fig.1. (b) Proposed FAM design using Kogge stone Adder.

FAM design with sum-modified booth (S-MB) recoding technique reduces the number of partial products and increasing speed of calculation. The FAM technique which decreases the critical path delay and reduces area and power consumption. The proposed S-MB algorithm is structured, simple and can be easily modified in order to be applied either in signed (in 2's complement representation) or unsigned numbers, which comprise of odd or even number of bits .In this paper, we present new technique for direct recoding of two numbers in the MB representation of their sum .In the unsigned or signed numbers ,there are six techniques in both which are implemented with separate design.

II.MODIFID BOOTH ALGORITHM USING RADIX 4

Modified Booth algorithm was implemented by the O.L.Macsorley in 1961. We know the Modified Booth with Radix-4 is used for fast multiplication process and to generate the partial products for implementation of the large parallel multipliers ,which done the parallel encoding scheme. The main advantages of Modified Booth Algorithm with Radix-4 is reduces by half the number of partial product than the original Booth Algorithm with Radix-2 . Recoding the multiplier in higher radix is a powerful way to speed up standard Booth Multiplication algorithm. .In each cycle a greater number of bits can be eliminated , so the total number of cycles required to obtain product get reduced [3] [4.]

III. SUM TO MODIFIED RECODING

In this design, the three new schemes of the S-MB recoding techniques are used for both the signed or unsigned numbers which consist of odd or even number of bits .So, we use the conventional and signed HA's and FA's for this recoding schemes. In S-MB recoding ,we recode the sum of two successive bits of inputs A(a2j,a2+1) with two successive bits of the input B (b2j,b2j+1) into one MB digit yjMB.So, we require three bits for forming MB digit. For all these schemes we use inputs A and B in 2's complement form and they consist of 2k bits for even case and 2k+1 bit for odd case .

Table I . Modified Encoding Table

Binary Numbers				MB Encoding			Input
y_{2j-1}	y_{2j}	y_{2j-1}	y_j^{MB}	$Sign(S_j)$	One_j	Two_j	Carry
0	0	0	0	0	0	0	0
0	0	1	+1	0	1	0	0
0	1	0	+1	0	1	0	0
0	1	1	+2	0	0	1	0
1	0	0	-2	1	0	1	1
1	0	1	-1	1	1	0	1
1	1	0	-1	1	1	0	1
1	1	1	0	1	0	0	0

The MSB of these bit is weighted by negatively and the two bits of LSB is positively weighted .These pairs of former bit convert in MB form we want signed-bit arithmetic. Hence we implement the bit-level signed Half Adders and Full Adders for their input and output will be signed. These

ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
Vol 3, Issue 12, December 2016

S-MB Recoding techniques are implemented by using the Radix-4 .

Defining Sum-to-Modified Recoding technique (S-MB):

1)S-MB 1 Recoding Scheme : This is the first scheme of the recoding which is called S –MB 1 and it is used for both the even and odd bit of the input numbers. The sum of the input A and B given by the following equation:

$$Y=A+B=y_k.2^{2k}+\sum^{k-}1v_{j-o}\,y_j^{MB}.2^{2j} \quad (1)$$

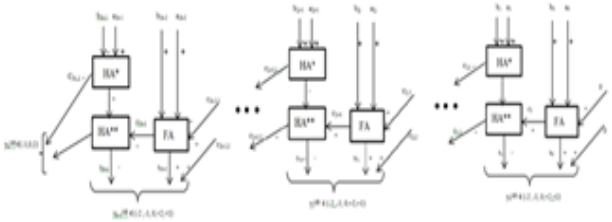
In the Fig.2 shows the conventional FA has inputs a2j , b2j and b2j-1 which produces carry c2j+1=(a2j ^ b2j) v (b2j-1 ^(a2j v b2j)) and sum s2j= a2j xor b2j xor b2j-1.S2j+1 is bit which is extracted from jth recoding cell and if we want to be negatively signed ,then we use FA* with inputs a2j+1,b2j+1(-) and c2j+1 which produces the carry c2j+1 and the sum s2j+1(-):

$$c_{2j+2} = (a_{2j+1}\wedge b_{2j+1}) \vee (c_{2j+1} \wedge (a_{2j+1} \vee b_{2j+1}))$$
$$S_{2j+1}=a_{2j+1} \text{ xor } b_{2j} \text{ xor } c_{2j+1}. \quad (2)$$

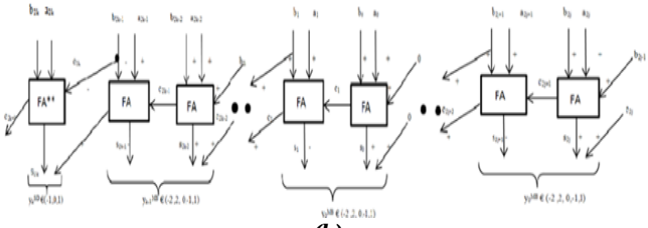
In S-MB 1 recoding scheme ,the most significant digit (MSD) can be formed by two cases -(1) both inputs A and B are even number of bits. (2) both inputs A and B are odd number of bits. In the first case the MSD is signed digit and it is given by following equation :

$$y_k^{SD}, \text{ even} = -a_{2k-1} + c_{2k}. \quad (3)$$

And in second case ,the MSD is a MB digit which is depend on c2k+1,s2k, and c2k.Then the carry c2k+1(-) and the sum s2k are produced by the FA** which has the input a2k(-),b2k(-) and b2k-1.



(a)



(b)

Fig.2.S-MB 1 Recoding Scheme: a) even b) odd number of bits.

2) S-MB 2 Recoding Scheme : The second technique is S-MB 2 which is also used for both even and odd number of inputs .In this we consider the initial value $c_{0,1-0}$ and $c_{0,2-0}$.We know in the S-MB 1 scheme the conventional FA is used to produce the carry c_{2j+1} and sum s_{2j} .Similarly used in S-MB 2 which has inputs of FA are a_{2j},b_{2j} and c_{2j}.And in fig shows there is above conventional HA produces output carry c_{2j+1} and it is part of (j-1) recoding cell and has inputs a_{2j-1},b_{2j-1} .The HA* produces output which is sum s_{2j+1}.The HA* is used to produce negatively signed sum s_{2j+1} and output is given by following Boolean equation:

$$c_{2j+2,2}= c_{2j+1} \vee (a_{2j+1} \text{ xor } b_{2j+1})$$
$$s_{2j+1}=a_{2j+1} \text{ xor } b_{2j+1} \text{ xor } c_{2j+1} \quad (4)$$

In case of the inputs A and B are even, the bits a_{2n-1} and $b_{2n1}$are negatively weighted and MSD is signed digit

$$y_k^{SD},\text{even}= -c_{2k,1}+c_{2k,2}. \quad (5)$$

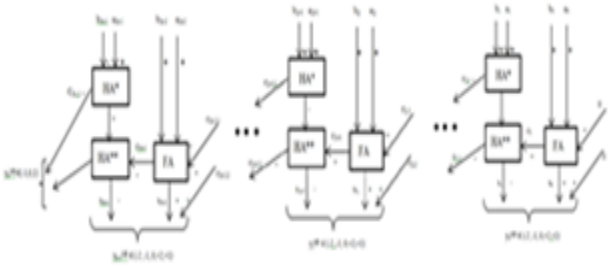
In case of the inputs A and B are odd ,the MSD is MB digit and it is depend on $c_{2k+1,}s_{2k}$ and $c_{2k,2}$.

3) S-MB 3 Recoding Scheme : The third method of recoding is S-MB 3 it is also used for both the odd and even number of bits. Let consider $c_{0,1}=0$ and $c_{0,2}=0$.Again in this we use conventional FA to produce the carry c_{2j+1} and sum s_{2j}. The HA* is produces output carry $c_{2j,1}$ and the HA** produces negatively signed bit s_{2j+1} which shown in the Fig.4

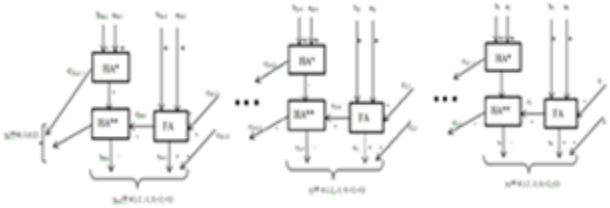
$$c_{2j+2,2} = c_{2j+1} \wedge (a_{2j+1} \text{ xor } b_{2j+1})$$
$$s_{2j+1}= a_{2j+1} \text{ xor } b_{2j+1} \text{ xor } c_{2j+1}. \quad (6)$$

ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
Vol 3, Issue 12, December 2016



(a)



(b)

Fig.3. S-MB 2 Recoding Scheme : a) even b) odd number of bits

IV .Kogge Stone Adder

Kogge stone adder is the parallel prefix adder which is the form of carry look ahead (CLA) structure .Fig.5 shows the 8-bit kogge stone adder. We know parallel prefix adders are done arithmetic operation faster than other adders and more flexible. In the industries mostly the parallel prefix adder because of their high performance arithmetic circuits [7]. The kogge stone required time to generate the carry signals is o(log n).The main focus on the design of the kogge stone adder is because of its less logic gates and critical delay.The kogge stone adder consist of three steps these are:

1.Pre-processing step: At each pair of input A and B the signal are propagated and generate the signal which is given by following equation.

Pi= Ai xor Bi (7)

Gi= Ai and Bi (8)

2. Carry –Generation Network step: In this step the carries are generated from each bit and computed in parallel fashion. After the carry computation in parallel they segmented into small pieces. It is used for propagate the carry and generate the intermediate signals which are given by the following equation:

CPi,j= Pi:k+1 and Pk:j (9)

CGi:j= Gi:k+1 or (Pi:k+1 and Gk:j) (10)

3.Post Processing step: This final step is common to all the adder which done the summation of the input bits. The following equation is given by :

Ci-1= (Pi and Cin) or Gi (11)

Si = Pi xor Ci (12)

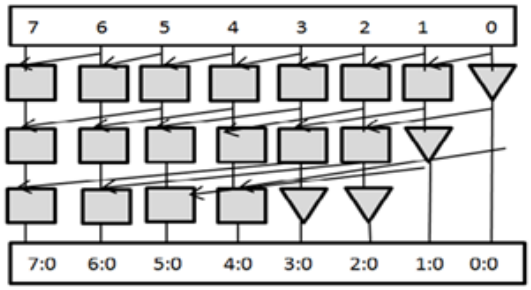
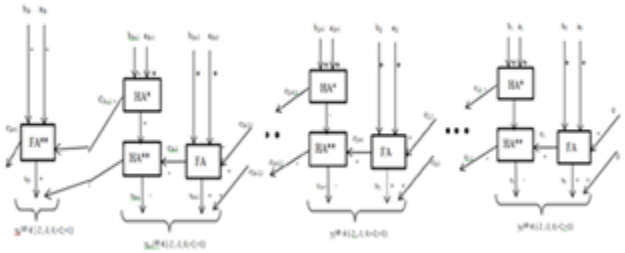
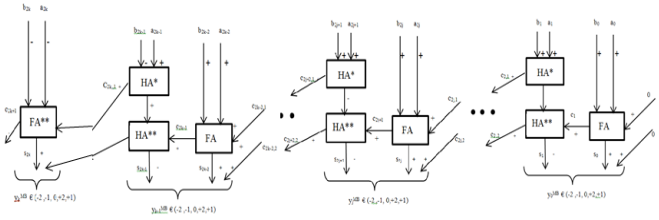


Fig.5.8-Bit Kogge Stone Adder



(a)



(b)

Fig.4.S-MB 3 Recoding Scheme : a)even b) odd number of bits

Table.II.Comparison Of Proposed Sm-B Techniques

Logic Utilization	SMB-1	SMB-2	SMB-3
No .of Slices	89	106	106
No. of Slices Flip Flops	46	45	44
No. of 4 Input LUTs	169	203	205
No .of bounded IOB	11	11	11
Delay	5.271ns	5.558ns	5.558ns

ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
Vol 3, Issue 12, December 2016

V. EXPERIMENTAL WORK

Sum to modified recoding techniques which are based on FAM design , these are implemented by using the Xilinx ISE design suit and the output waveform

VI. CONCLUSION

In this work, we focus on optimizing the design of the Fused-Add Multiply (FAM) operator. In this structure the S-MB1 ,S-MB2 and S-MB3 recoding schemes are the most efficient ones (regarding their overall performance which includes critical delay, area complexity and power dissipation). Fused Add-Multiply Operator is implemented by using different full adders and half adders whose output values has been given according to the signed and unsigned bit stream of the input numbers depending on the Modified Booth encoded table and the techniques has been designed for the odd and even bit- width of the input numbers. And at last the Kogge stone adder will be added so it requires less gates ,so the circuit complexity as well as area will be decreased. As compare to previous multiplier, the present multiplier has more advantages like requirement of less gates, low power, high speed, high performance. If this multiplier is used in any processor, it increases the performance of processor.

REFERENCES

[1]Kostas Tsoumanis, Sotiris Xydis, Constantinos Efstathiou, Nikos Moschopoulos, and Kiamal Pekmestzi,"An Optimized Modified Booth Recoder for Efficient Design of Add-Multiply Operator." IEEE Trans. ,VOL.61,NO.4,APRIL 2014.

[2]W.-C.Yeh,"Arithmetic Module Design and its Application to FFT,"Ph.D.dissertation,Dept.Electron Eng.,National Chiao-Tung University,Chiao-Tung,2001.

[3]R.Zimmermann and D.Q.Tran,"Optimized Synthesis of sum-of-products," in Proc .Asilomar Conf.Signals,Syst.Comput,PacificGrove,Washington,DC,2003,pp.867-872.

[4]Y.-H. Seo and D.-W. Kim, "A new VLSI architecture of parallel multiplier–accumulator based on Radix-2 modified Booth algorithm,"IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 18, no. 2, pp.201–208, Feb. 2010.

[5] O. L. Macsorley, "High-speed arithmetic in binary computers," Proc.IRE, vol. 49, no. 1, pp. 67–91, Jan. 1961.

[6] B. Parhami, Computer Arithmetic: Algorithms and Hardware Designs. Oxford: Oxford Univ. Press, 2000.

[7] V. Krishna Kumari, Y.Sri Chakrapani, Dr.M.Kamaraju Design and Charact erization of Koggestone, Sparse Koggestone, Spanning tree and Brentk ung Adders International Journal of Scientific & Engineering Research, Volume 4, Issue 10, October 2013 , 1502.