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Design And Development Of ARINC 717 Protocol

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Abstract- **ARINC has provided leadership in developing specifications and standards for avionics equipment, and one of the standard protocol used for communication bus is ARINC 717. This communication occurs between Digital flight data acquisition unit (DFDAU) and Digital flight data recorder (DFDR). The basic unit of information defined by the ARINC 717 protocol is a 12-bit word. The Programmable bit rates of ARINC 717 are 384, 768, 1536, 3072, 6144, 12288, 24576, 49152 and 98304 bits/sec (32, 64, 128, 256, 512, 1024, 2048, 4096 and 8192 words/sec). The data is serially transmitted in ARINC 717. The top level architecture of the ARINC 717 protocol has 4 modules ARINC 717 transmitter, ARINC 717 receiver, Transmit and Receive 32*12-bit FIFO to store and fetch the data, and ARINC 717 clock generation.**

In this proposed work a Hardware Descriptive Language (HDL) based design and development of the ARINC 717 protocol for standard data bus communication. The input data is taken from Digital flight data acquisition unit. This continuous data stream is stored in a 32*12-bit FIFO. The encoder module at ARINC 717 transmitter converts a continuous data stream into a 12 bit encoded Harvard Bi-Phase (HBP) format which are then encoded to form ARINC 717 frames. This encoded data is decoded using both Harvard bi-phase and bi-polar return to zero at the receiver. The decoded data is stored in the Receive FIFO. Then the continuous stream of output data is taken for recording in Digital flight data recorder. The design and development is done using Xilinx software.

Keywords— **ARINC 717, BPRZ decoding, DFDAU, DFDR, FIFO, HBP encoding, , VHDL**

I. INTRODUCTION

Aeronautical Radio, Incorporated (ARINC) is a major company that develops and operates systems and services to ensure the efficiency, operation, and performance of the aviation and travel industries. It was organized in 1929 by four major airlines to provide a single licensee and initiator of radio communications outside the government. Only airlines and aviation-related companies can be shareholders, although all airlines and aircraft can use ARINC's services. It is now a $280 million company with headquarters in Annapolis, Maryland and over 50 operating locations worldwide. ARINC has provided leadership in developing specifications and standards for avionics equipment and these specifications are used to define physical packaging and mounting of avionics equipment, data communications standards and High level computer languages.

A. ARINC STANDARD SERIES

ARINC has many number of series like 400, 500, 600, 700 and each series has its own advantages and used for different avionics equipment's. For example ARINC 400 Series describes guidelines for installation, wiring, data buses, and databases. ARINC 500 Series describes older analog avionics equipment used on early jet aircraft such as the Boeing 727, Douglas DC-9, DC-10 , Boeing 737 and 747 , and Airbus A300. ARINC 600 Series are reference standards for avionics equipment specified by the ARINC 700 Series ARINC 600 is the predominant avionics packaging standard introducing the avionics Modular Concept Unit (MCU). ARINC 700 Series describes the form, fit, and function of avionics equipment installed predominately on transport category aircraft.

B. ARINC 717

The ARINC 717 specification defines the communication protocol used by the Digital Flight Data Acquisition Unit (DFDAU) and the Digital Flight Data Recorder (DFDR). The DFDAU accumulates data from the aircraft systems and converts digital and analog aircraft inputs into a standard ARINC 717 data stream that is compatible with all ARINC 717 flight data recorders then transmits it to the DFDR on a Harvard bi-phase ARINC 717 data bus. A similar bipolar ARINC 717 data bus can connect to a Quick Access Recorder (QAR) as shown in figure 1.

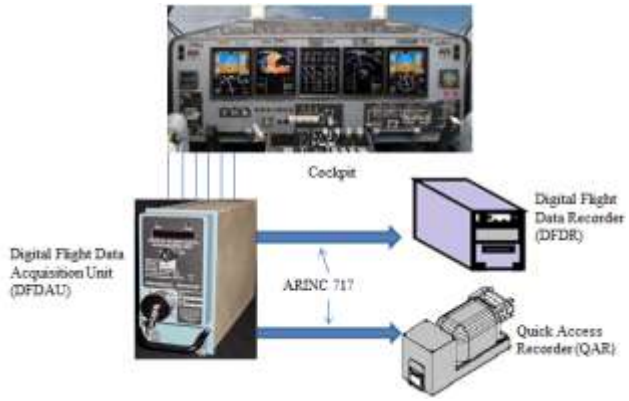

Figure 1: Flight data management system[2]

Here, the DFDAU assumes the position of the computer and the transmission point, as the different data are collected, combined, and transformed into the format of the ARINC 717 protocol on these system components. This data bundle then reaches the DFDR only.

C. FEATURES OF ARINC 717

- It defines standard data communication between DFDAU and DFDR.
- It is dual mode transmission.
- It has independent bi-phase and bipolar receive channels.
- It is capable of transmitting at the rates of 32, 64, 128, 256, 512, 1024, 2048, 4096 and 8192 words per second.
- It uses Harvard bi-phase encoding and both Harvard bi-phase and bipolar decoding methods.
- The data is more secured for the better performance.

D. ARINC 717 FRAME FORMAT

The basic unit of information defined by the ARINC 717 protocol is a 12-bit word. There are two types of words: synchronization words and data words as shown in figure 2.

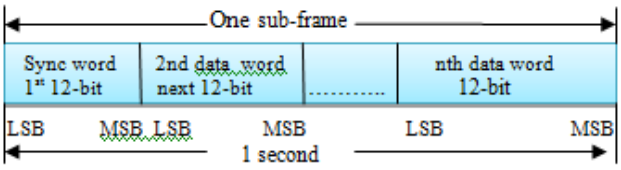

Figure 2: one sub-frame

The first 12- bit word of a sub-frame that appears on the ARINC 717 bus is the synchronization (sync) code with the least significant bit (LSB) first. This is immediately followed by up to 63(basic rate) 12-bit data words, all within1 second from the start of the synchronization code for 64 words per second. There are four sub-frame and is transmitted every second. The length of a sub-frame is determined by the transmission speed of the bus. Although the ARINC 717 specifies bus speeds of 64 to 8192 words per second. Four sub-frames are grouped together into a single frame. Since a sub-frame is transmitted every second, a frame is transmitted every four seconds as shown in figure 3.

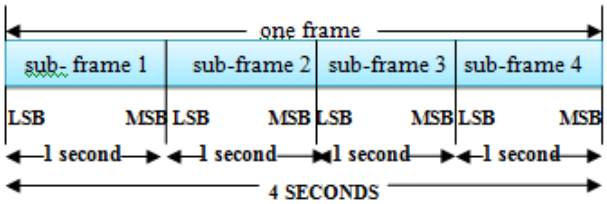

FIGURE 3: ONE FRAME

ARINC 717 messages consist of 12-bit words sent in a 4 seconds frame divided into four 1 second sub-frames. Each sub-frame consists of 64 (basic rate), 128, 256, 512, 1024, 2048, 4096 or 8192 12 bit words, depending on the data rate of the target system.

II. OPERATIONS OF ARINC 717

A. FIRST PHASE OF ARINC 717

In this phase of the ARINC 717 the digital flight data acquisition unit receives information from the different components in the aircraft. The collected data includes information concerning the condition of the devices. This data can also provide information regarding the altitude, the current and average velocity and the position of the rudder. These data elements are recorded as so called parameters. Each individual fraction is verified via an 8-bit identifier and additionally, it also contains a payload between 18 bits and 19 bits.

The digital flight data acquisition unit buffers the data, thus converting them to frames and sub-frames. A recording of four seconds of the life of an aircraft is called a frame. The sub-frames then are the subdivisions of this frame. A frame has a total of four sub-frames, which are then assigned each second of the four seconds of recorded life time. As such, the sub-frame contains all of the collected data gathered by the DFDAU. In former times, when ARINC 717 was not yet on the market, aircraft mostly recorded only up to 64 parameters, but since the introduction of the digital flight recorders, the average is 128 parameters. In comparison, 256 parameters must always be recorded for an aircraft in the United States of America, and in the case of the Airbus A380, the largest commercial aircraft that produced in serial production, one recording is made up of 1024 parameters.

B. SECOND PHASE OF ARINC 717

This phase of the ARINC 717 - a set of parameters is only considered as having been transmitted completely when one frame, i.e. all four seconds of the recorded life

time of an aircraft has been transmitted. Afterwards this process can start again. As a rule a whole 25 hours of the life time of an aircraft are recorded and stored. Each individual parameter of the set to be transmitted holds 12 bits of stored payload. At this point of the ARINC 717 protocol, the bits which regulate identification and synchronization are no longer needed, as the sub-frames always have the same construction.

This makes it possible to determine an element just by its position in the frame, and the parameters can transmit data in their chronological order without interruptions and separations. However, not every parameter is actually needed in each transmission, so that the parameters considered as less important in the system are only used and transmitted in each second or fourth parameter. The sub-frames also always differ in their first parameter, which is used for the purpose of identification. The remaining parameters then can be installed according to a scheme defined by a specified pattern.

C. FINAL PHASE OF ARINC 717

The ARINC 717 encoder accesses data from a 32 word x 12 bit Transmit FIFO, encodes it into HBP data stream at the selected data rate, and converts the digital data stream to ARINC 717 bus compatible outputs. The input to the encoder is from the DFDAU, the data from this unit consists of a snapshot of the many avionics subsystems on the aircraft. The data is serially transmitted to the module. The encoder compares the data with 0's and 1's and encodes it in Harvard Bi-Phase format. The HBP bit encoding is as shown in the figure 4.

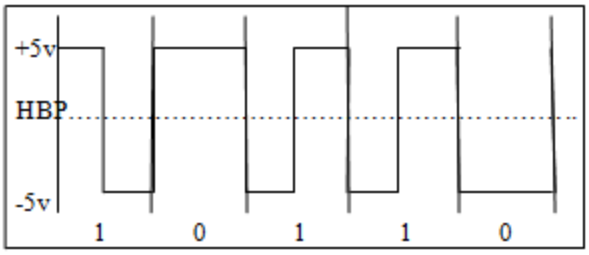

Figure 4: ARINC 717 Harvard bi-phase input format

Then the decoder recovers the clock and resynchronizes each valid one or zero to the transition bit period. The Harvard Bi-phase decoder confirms that sampler provided only a valid One or Zero, not both, then detects the presence or absence of an edge in the data bit period. The output of the decoder is a "1" if there was a transition, otherwise a "0".

III. TESTING METHODOLOGY OF ARINC 717

There are two types of testing the ARINC 717 protocol such as loop-back test and individual test.

A. LOOPBACK TEST

In loopback test the buffered input data is taken from DFDAU and the input data is stored in 32x12 transmit FIFO as 12-bit data.

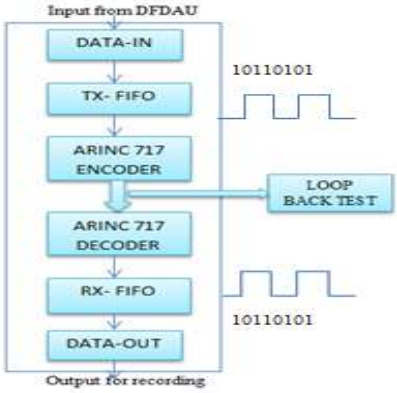

Figure 5: Block diagram of ARINC 717 with loop back test This 12-bit data is encoded in Harvard bi-phase format. The encoded data is transmitted by ARINC 717 encoder and transmit it to the receiver. The ARINC 717 decoder decodes the data and stores the data in 32X12 receive FIFO. The data from the receive FIFO is looped back to the interface between input data and transmit FIFO to check if the data received is same as transmitted data.

B. INDIVIDUAL TEST

In individual test each ARINC 717 transmitter and ARINC 717 receiver is tested separately. The buffered input data is taken from DFDAU and the input data is stored in 32x12 transmit FIFO as 12-bit data. This 12-bit data is encoded in Harvard bi-phase format and transmits it to the ARINC 717 line driver for transmitter test as show in figure 6.

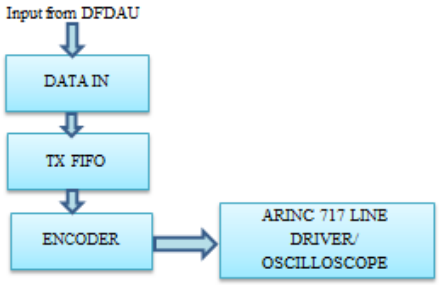

Figure 6: Block diagram of ARINC 717 Transmitter test

The ARINC 717 line receiver gives the data to the encoder as shown in figure 7. The ARINC 717 decoder decodes the data and stores the data in 32X12 receive FIFO. The data from the receive FIFO is output data taken for recording in DFDR.

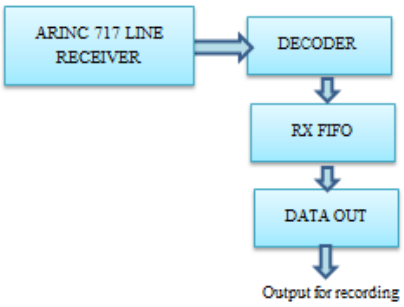

Figure 7: Block diagram of ARINC 717 Receiver test

IV. IMPLEMENTATION ARINC 717

A. Top level block diagram of ARINC 717

The top level block diagram of ARINC 717 is as shown in Figure 8. The ARINC test bench provides the input data to the ARINC 717 module. It acts as a microcontroller. The test bench inputs are the addresses and data. The ARINC clock generation takes the clock provided by the microcontroller (100/50 MHz in this case) and generates a ARINC 717 clock of ((32, 64, 128, 256, 512, 1024, 2048, 4096, 8192)*12-bit)HZ which is used by the transmitter and the receiver.

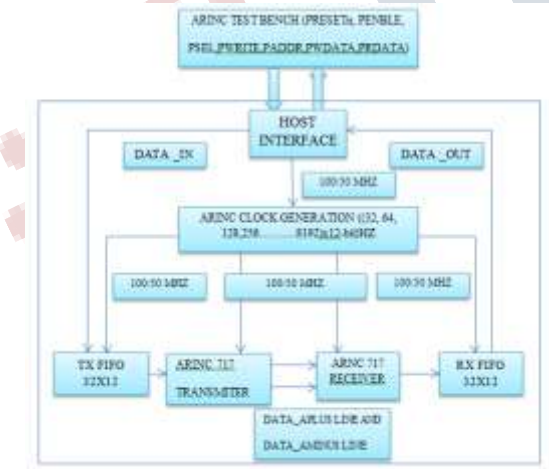

Figure 8: Top level block diagram of ARINC 717

The TX FIFO takes the input from the test bench and ARINC clock generation. The input from the test bench is buffered and stored in 32X12 FIFO as 12-bit data. This 12-bit data is taken and encoded into HBP format. The encoded data is transmitted by the ARINC 717 transmitter.
The ARINC 717 receiver decodes the data and stores the data in 32X12 FIFO. The data from the receiver FIFO is looped back to the host interface to check if the data is received correctly. Host interface interfaces the ARINC 717 module to the microcontroller.

B. Top level Finite State Machine for ARINC 717 IP core

The Finite State Machine for ARINC 717 is as shown in the Figure 9. There are five states: Reset state, idle state (s1), configuration state, transmit state, and receive state. The events for the FSM are reset, config, START_TX, STOP_TX, START_RX, STOP_TX.

The working of the FSM is as stated below:

When reset event occurs, reset state transitions to idle state or to reset state itself depending upon the event. If reset is 1, the state transitions to itself or if reset is 0, the state transitions to idle state. When config event is set to 1, the state transitions from idle state to configuration state. The transition from the configuration state to transmit state or receive state occurs depending on which of the event occurred. If START_TX event had occurred, the configuration state transitions to transmit state, else if START_RX had occurred, the transition will be to receive state. In transmit or receive state the config will be set to 0. During no transmission or reception of data the STOP_TX or STOP_RX event goes to 1 and the current state transitions to the idle state. The process repeats when the config event is set to 1.

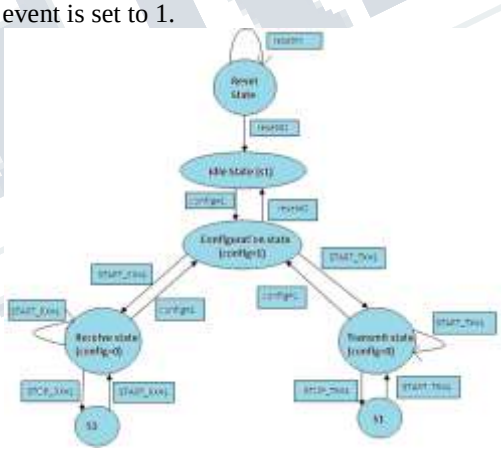

Figure 9: FSM for ARINC 717

V. SIMULATION RESULTS

Figure 10: Simulated output for the data given from the test bench to transmitter FIFO (waveform in red color)

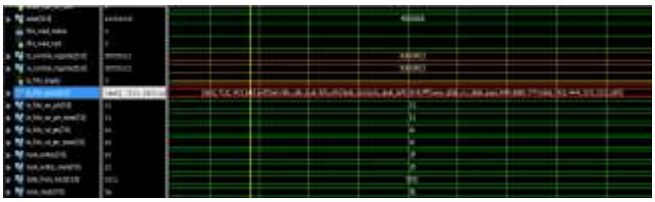

Figure 11: Simulated output for the data stored in Transmit FIFO (waveform in red color)

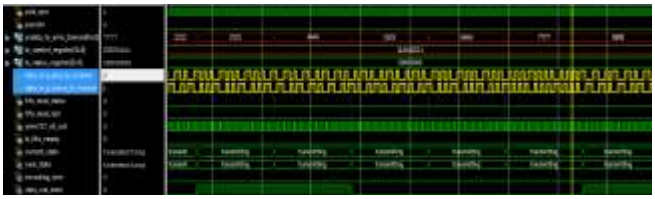

Figure 12: Simulated output for the data read out from the transmit FIFO (red color) and encoded output (yellow color)

Figure 13:Simulated output for encoded data sent to ARINC 717 receiver (yellow color) and decoded data (purple color)

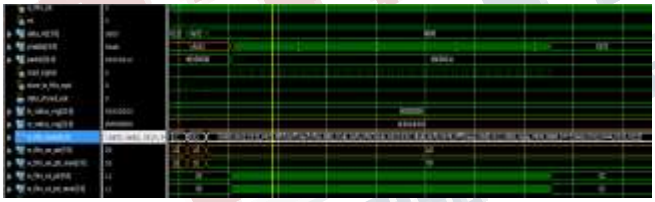

Figure 14: Simulated output for showing the data in the receive FIFO (white color)

Figure 15: Simulated output for decoded data sent from ARINC 717 receiver FIFO and read by ARINC 717 (blue color)

VI. CONCLUSION

The ARINC 717 protocol is a significant protocol which has been successfully implemented and simulated in VHSIC Hardware Description Language for different bit rates ranging from 32 words/sec to 8192 words/sec. HBP encoding method eliminates the need of extra bits for synchronization by self-clocking. This protocol is developed using Xilinx 14.2 version. This can be further implement on smart fusion evaluation kit.

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