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Radar Control Pulse Generation Using FPGA

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Abstract: **The current work is aimed to fabricate a pulse generator to meet the requirements of control and process signals to be applied on to several basic constituting functional units of a radar system. The functional units of Radar system includes Exciter, Receiver, Radar Controller, TCSG and Duplexer Antenna.The synchronized pulses generated are operate on functional units is accomplished by generating a reference pulse known as "Inter pulse period". The controlled pulses in the radar systems are categories as Exciter pulse, Transmit pulse, Gating pulse, Blanking pulse and are generated with respect to "Inter pulse period". All these functions of the different control signals generated for the functioning of radar is conveniently done by FPGA system using Spartan 6.Pulsed radar transmits high power, high-frequency pulses toward the target. Then it waits for the echo of the transmitted signal for some time before it transmits a new pulse and it can be used to measure target velocities. Target Range and bearings can be determined from the measured antenna position and time-of-arrival of the reflected signal.Pulse generator is the equipment that are used to generate pulses - normally rectangular pulses, these pulses can be used to generate pulses that can stimulate logic circuit.These different pulses can be generated by using FPGA, it can be programmed to the desired application or functionality requirements.**

***Keywords*: Inter pulse period, Echo Signal, TCSG, FPGA.**

I. INTRODUCTION

Acronym **RADAR** stands for **R**adio **D**etection and **R**anging. Radar is an electromagnetic system used to detect the objects which are not visible to normal eye sight. It can be used to detect aircrafts, ships, space vehicles etc... Such objects which are detected by Radar are called 'targets'. There are many types of radars based on their area application. It can be used in air force, weather forecasting, to measure speed and shape of the moving target etc.It is mainly used to detect the presence of any target in the range of Radar. A radar system includes a transmitter which emits a series of EM pulses. These pulses are radiated in a directional pattern using a suitable high-gain antenna. The radar then uses a receiver, usually connected to the same antenna, to detect any returned pulses being reflected from objects appearing in the antenna's field of view.

II. EXISTING SYSTEM

Complex electronics (CE) encompasses programmable and designable complex integrated circuits. Programmable logic devices can be programmed by the user and range from simple chips to complex devices capable of being programmed on-the-fly. In the term complex electronics, the complex adjective is used to distinguish between simple devices, such as off-the-shelf ICs and logic gates, and user-creatable devices. A good rule of thumb is, if you can program or design the internal logic of the device and it has more than a few gates and connections, it is probably complex. Some types of programmable devices are:

- Complex Programmable Logic Device (CPLD)
- Field Programmable Gate Arrays (FPGA)
- Application Specific Integrated Circuit (ASIC)
- System-on-chip (SoC)

A. Complex Programmable Logic Devices:

The building block of a CPLD is the macrocell,which contains logic implementing disjunctive normal form expressions and more specialized logic operations. A CPLD contains a set of simple Programmable Logic Device (PLD) blocks whose inputs and outputs are connected together by a global interconnection matrix. A CPLD has two levels ofprogrammability: each PLD block can be programmed, and then the interconnections between the PLDs can be programmed. A key feature of the CPLD architecture is the arrangement of logic cells on the periphery of a central shared routing resource. CPLDs use EEPROM, SRAM, or Flash memory to hold the interconnect information. The main distinction between FPGA and CPLD device architectures is that FPGAs are internally based on Look-up tables (LUTs) while CPLDs form the logic functions with sea-of-gates. The maindifference between a FPGA and a

CPLD is the different functional logic that is used in their design. In the CPLD, the functional logic is called PLD but the functional logic in FPGA is called complex logic block (CLB). The density and size of a CLB is much smaller compare to size and density of a PLD. But inside a FPGA, there is much more CLBs compared to the numbers of PLDs inside the CPLD. These CLBs are distributed across the entire chip and connected through the programmable interconnection.

III. PROPOSED SYSTEM

The proposedRadar system consists of Exciter, receiver,and the out-door TR modules. Exciter generates (i) the pulse-coded 53-MHz waveform, which will be fed to the out-door TR modules via the RF distribution/combining network, and (ii) the 10-MHz clock/reference signal, which will be given to the back-end receiver section and the direct digital receiver (DRx), and timing and control signal generator (TCSG) for their operation. Thereceived RF signal is suitably amplified and band limited in the back-end receiver unit and fed to the DRx for processing and display. TCSG generates the inter-pulseperiod (IPP) marker trigger pulse, which will be used as reference to generate different timing and control signals.

Timing signals are used to switch different RF switches in both transmit and receive paths where as the control signals are used to set the gain/attenuation, phase shift etc., in both transmit and receive paths. Master radar controller (RC) controls and monitors the functioning of all the radar subsystems.

The functional block diagram of Radar Control Pulse Generator is shown in fig 1. It mainly consisting of radar exciter, TCSG, radar controller, TX-RF distributor, T/R switches,
DRx etc.

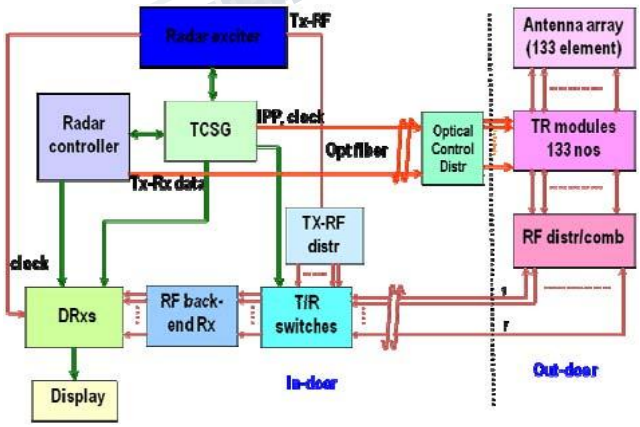

Fig1: Block diagram of Radar Control Pulse Generator

A. Radar Controller (RC):

The PC-based RC performs the following basic functions. (i) Facilitates the user to set the experimental parameters and beams through GUI, (ii) stores the calibration phase-error data, generates phase correction file, and generates the phase data required for each TR module for the beams selected, (iii) pre-loads the experimental parameters and phase data into the TCSG, Exciter, Receiver and TR modules through Ethernet switching network before starting the radar operation, and (iv) reads the status data from the TR modules during operation and displays the status data through the GUI, and (v)Sends the experimental parameters to Digital Receiver through Ethernet switch before starting the radar operation and communicates during the operation.

B. Timing and Control Signal Generator (TCSG):

TCSG works directly under the control of RC and interfaced through Ethernet. It receives the 10-MHz reference clock from the Exciter and generates the reference IPP marker when radar operation is started in the RC. It also generates the timing and control signals required for other subsystems such as Exciter, distribution network, TR modules, receive back-end, and DRx. All the timing pulses will be generated with reference to the IPP and the rising edge and width ofthese timing signals will be as specified in the experimental parameters in the RC GUI. i.e. Depending on the data received from the master radar controller, TSG card generates timing and control signals in synchronization with IPP trigger pulse received from radar controller. The phase shifter data corresponding to the beam direction are stored in the module and beam direction will be controlled from IPP to IPP. Data for phase shifter is provided by Radar controller.

The RF signal from the coupled port is brought to the optical transceiver unit via the SPDT switch. The SPDT SW is switched between the Tx and Rx mode. During the transmit mode, the output of the SPDT SW is converted into optical signal and sent to the instrumentation room through optical fiber cable for measuring the amplitude and phase. In the receive mode, the simulated RF pulse is injected into the TR module via the optical fiber, converted into RF pulse and fed to the forward coupled port through SPDT SW. this signal passes through the RX chain and sent back to the instrumentation room for measuring the amplitude and phase.

The pulse generation can be done by using radar exciter , radar controller and all other elements which are used in active array radar for radar applications and can be

done effectively by using this FPGA as a control pulse generator.

All these control pulses can be generated by FPGA utilized as a part of Xilinx Spartan6.

IV. SIMULATION RESULTS

The controlled pulses required for operation of basic functional units in a radar system with respect to a standard "Inter pulse period" is as follows:

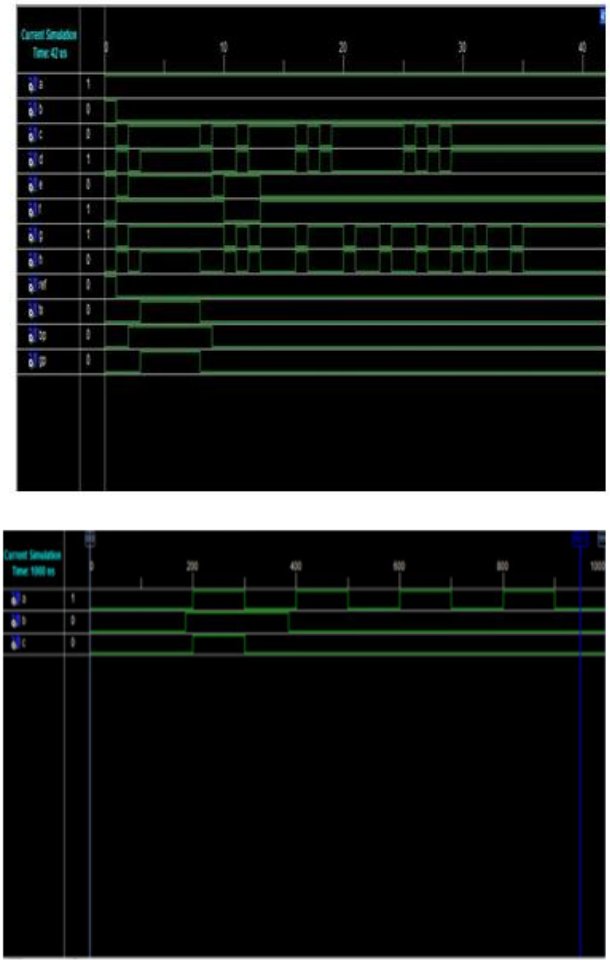

Fig2: Simulation results of Timing Control Pulse Generator.

All these control pulses required for the Radar system. Transmit pulses are generated with respect to this Inter pulse period.

In IPP the distance between one rising edge of clock to another clock pulse will be 1000us,and for TR switch the pulse will lower for 6us after it will rise up to 8us, and again it goes constant time period for 14us, like wise it will be repeat up to 1000us.For blanking pulse, the signal will be constant for 4us and the lagging edge of clock pulse will be started and it will rise after 10us change according to the IPP. Here three command switches are used for controlling of radar, those are nothing but A,B,C. the operation of switch A will be similar to the TR switch, switch B will be rise and constant for 14us and switch C will be constant for 1000us.Similarly all the pulses have different time periods and vary according to the IPP.

V. CONCLUSION

All the timing pulses are generated for effective functioning of Radar system with different time periods can be simulated and configured by XilinxSpartan6 on FPGA Board. Which presents flexible, easy and trustable methodology? The configured system can be programmed to act according to the target of the system.

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