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Design of 512-bit Wallace Tree Multiplier by Sklansky Adder

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Abstract- **Power consumption has become a crucial concern in today's VLSI system style. The growing marketplace for quickfloating purpose coprocessors, digital signal process chips, and graphics processor has created a requirement for topspeed and space economical multipliers. A Wallace tree multiplier factor may be a improved version tree based mostly multiplier factor design. It uses carry save addition rule to cut back the latency. This paper aims at extrareduction of latency and power consumption of the Wallace tree multiplier factor. The simulation has been meted outmistreatment the Xilinx ISE tool.**

***Keywords*: Adder, Black cell, Grey cell, Multiplier, sklansky adder, Wallace tree.**

I. INTRODUCTION

A multiplier factor is one in all the key hardware blocks in most digital and high performance systems like FIR filters, digital signal processors and microprocessors etc. With advances in technology, several researchers have tried and are attempting to style multipliers which provide either of the following- high speed, low power consumption, regularity of layout and thus less space or perhaps combination of them in multiplier factor. Therefore creating appropriate for varied high speed, low power and compact VLSI implementations.But space and speed area unit 2 conflicting constraints. Thus rising speed results perpetually in larger areas. Thus here we tend to attempt to verify the simplest trade off resolution among the each of them. Then we've got designed Wallace tree multiplier factor then followed by standard, planned Wallace multipliers and have compared the speed and Power consumption in each of them. Whereas scrutiny the adders we tend to acknowledged that Ripple Carry Adder had a smaller space whereas having lesser speed, in distinction to that sklansky Adders area unit high speed however posses a bigger space. When planning the adders we tend to turned to multipliers. At the start we tend to went for Parallel multiplier factor then Wallace Tree multiplier factor. Within the time unit we tend to learned that delay quantity was significantly reduced once sklansky adder were utilized in Wallace Tree applications.

II. WALLACE TREE MULTIPLIER

Wallace tree reduces the quantity of partial merchandise to be supplementary into a pair of final intermediate results. The Wallace tree essentially multiplies 2 unsigned integers,A Wallace tree is AN economical hardware implementation of a digital circuit that multiplies 2 integers, devised by AN Australian computer user Chris in 1964.

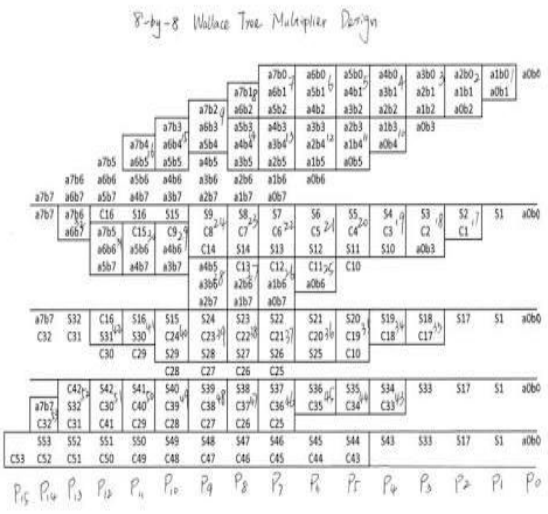


Fig 1: Design of Wallace tree multiplier

The Wallace tree multiplier has 3 steps:
A. Partial Product Generation

B. Partial Product Reduction
C. Partial Product Addition

A. PARTIAL PRODUCT GENERATION

Partial product generation is that the terribly 1st step in binary multiplier factor. These are the intermediate terms that are generated supported the worth of multiplier factor. If the multiplier factor bit is '0', then partial product row is additionally zero, and if it's '1', then the number is traced because it is. From the ordinal bit multiplication for adder, every partial product row is shifted one unit to the left as shown within the on top of mentioned example. In signed multiplication, the sign bit is additionally extended to the left. Partial product generators for a standard multiplier factor include a series of logic AND gates.

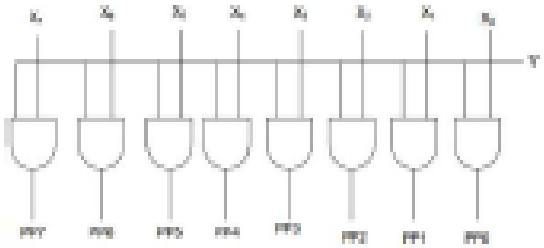


Fig 2: Partial Product Selection Logic

The main operation within the method of multiplication of 2 numbers is addition of the partial products. Therefore, the performance and speed of the multiplier factor depends on the performance of the adder that forms the core of the multiplier factor. To attain higher performance, the multiplier factor should be pipelined.

B. PARTIAL PRODUCT REDUCTION

The design analysis starts with the analysis of the elementary formula for multiplication by Wallace Tree multiplier factor. Figure 3.1 shows the formula for 8-bits x 8-bits multiplication performs by Wallace Tree multiplier factor. There square measure 5 stages to travel through, to finish the multiplication method. Every stage used 0.5 adders and full adders that square measure denoted by the red circle for the one bit 0.5 adder and also the blue circle for the 1-bit full adder. For this project, ripple-carry adder (RCA) is employed, to induce the ultimate product of the 2 operandsmultiplication. Secondly, the schematic of the standard 8-bits x 8-bits high speed Wallace Tree multiplier factor is style by pertaining to the formula.

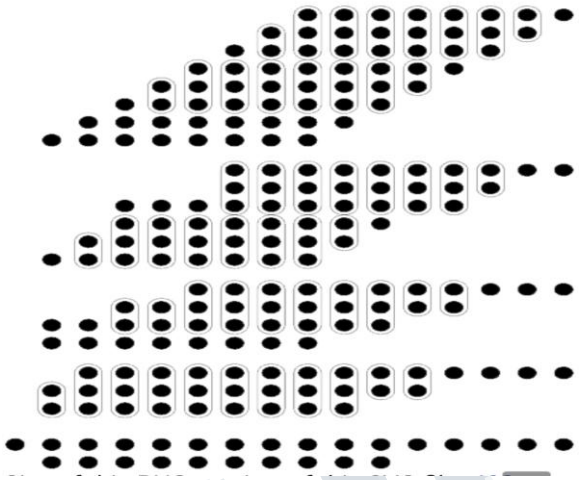


Fig 3: 8*8 Multiplication Partial ProductReduction.

Fig:3 shows the diagram for the standard high speed 8-bits x 8-bits Wallace Tree multiplier factor. Scale back the quantity of partial merchandise to 2 when the Verilog ASCII text file of the multiplier factor has been style, we have a tendency to should simulate and check its practicality. If it's functioning properly, we have a tendency to may proceed to consequent step, that is to see the utmost speed and time that the multiplier factor takes to finish one multiplication method.

III. PROPOSED WALLACE TREE MULTIPLIER

The projected design aims to scale back theoverall latency. This results in exaggerated speed and reduced power consumption. The look makes use ofcompressors in situ of full adders, and therefore thefinal carrypropagate stage is replaced by a Sklansky tree adder.Depicts the primary stage consist of a full adder. Within the second stage, 2 full adders aregrouped and enforced employing a 4:2mechanical device.Similarly, the third stage consists of 5:2 mechanical device,which may be a combination of three full adders so on. In thismanner, the individual full adder blocks within the original structure are classified and enforced victimization compressors.The quantity of interconnections is taken care of, since they play a significant role within the flow of carry from one stage to following within the tree.

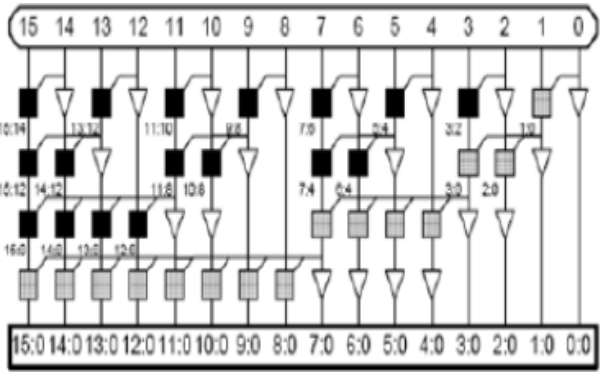


Fig 4(a): Schematic Wallace tree multiplier

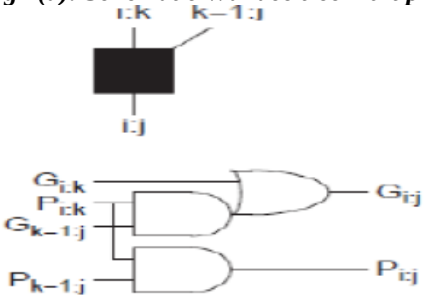


Fig 4(b): Black Cell

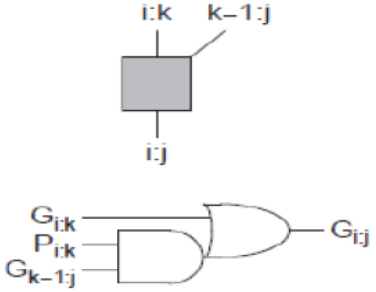
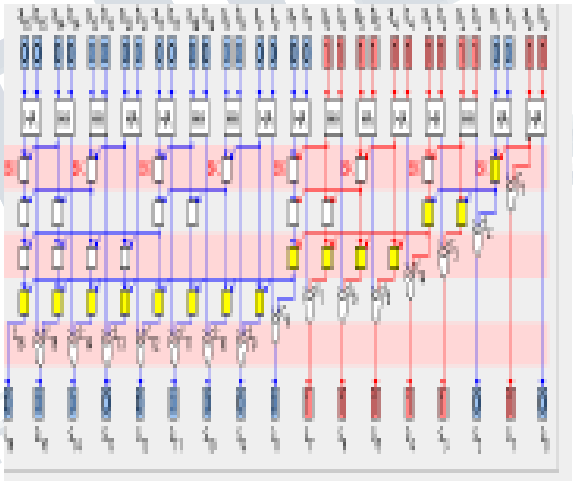


Fig 4(c): Grey Cell

The employment of the Sklansky adder within the structure any leads to a reduced latency of half dozen with a latency of one for the AND array. Hence, this structure brings down the general latency count to fifteen. Thus, a big latency reduction of forty four percentage 44% than the conventional counterpart is realized.

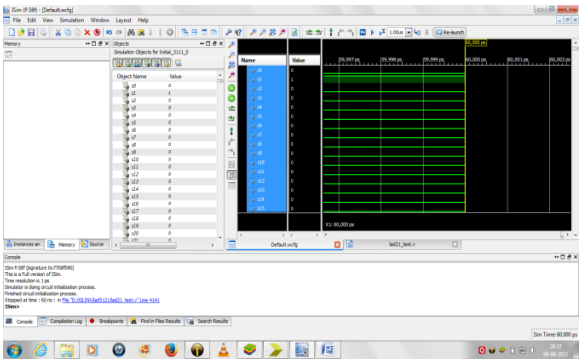
The Wallace tree primarily multiplies 2 unsigned integers. The projected Wallace tree multiplier design includes of Associate in Nursing AND array for computing the partial merchandise, Associate in Nursing adder for adding the partial merchandise thus obtained and a Sklansky adder in the final stage of addition. Compressor structures and therefore the last of addition is performed by a Sklansky adder. This number design includes of a partial product generation stage, partial product reduction stage and therefore the final addition stage. The latency within the wallace tree number may be reduced by decreasing the number of adders within the partial merchandise reduction stage.

The choose bits to the multiplexers are obtainable a lot of prior to the inputs so the crucial path delay is reduced. The varied adder structures in the conventional design are replaced by compressors. In high-speed styles, the Wallace tree construction methodology is typically want to add the partial products in an exceedingly tree-like fashion. So as to provide 2 rows of partial merchandise that may be added within the last stage. The Wallace tree is quick since the crucial path delay is proportional to the exponent of the quantity of bits within the number. There exist some of how to construct the Wallace Tree.



The distinguished methodology considers all the bits in every column at a time and compresses them into 2 bits (a total and a carry). The Wallace tree is made by considering all the bits in every fours row at a time and pressing them in Associate in Nursing acceptable manner. The speed, space and power consumption of the multipliers will be in direct proportion to the potency of the compressors. The projected designs are extremely economical in terms of little space and low power consumption.

IV. SIMULATION RESULTS



V. CONCLUSION:

In this paper, the implementation and analysis of a unique Wallace tree design is projected. The latency of existing Wallace tree multiplier factor that is found to be twenty seven has been reduced to fifteen.The comparison result additionally shows thatsignificant reduction of power is achieved. At associate degree operative frequency of fifty Mc at one.2V, the ability is found to be 153.47mW. it's a realization of eleven.6% of power reduction than the standard Wallace tree multiplier factor. At 1.14V,the power consumed is found to be 147.66mW, that could be a twelve.03% reduction of that obtained from the present design.

REFERENCES

[1] A. P. Chandrakasan and R. W. Brodersen, Low Power Digital CMOS Design. Norwell. MA:Kluwer.

[2] C. H. Chang, J. Gu, M. Zhang, "Ultra low-voltage low power CMOS 4-2 and 5-2 compressorsfor fast arithmetic circuits" IEEE Transactions on Circuits and Systems .

[3] H. Neil. Weste and Kamran Eshraghian, "Principles of CMOS VLSI design-A Systems Perspective," Pearson Edition Pvt Ltd. 3rd edition, 2005

[4] List I. Abdellatif, E. Mohamed, "Low-Power Digital VLSI Design, Circuits and Systems," Kluwer Academic Publishers, 1995.

[5] H. Neil. Weste and Kamran Eshraghian, "Principles of CMOS VLSIdesign-A Systems Perspective," Pearson Edition Pvt Ltd. 3rd edition, 2005.