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Modified Approximate DCT for Image Compression

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***Abstract*— DCT has a fundamental role in signal processing techniques and is a part of modern image and video compression standards. The major difficulties encountered in compressed DCT domain are computational complexity of image compression and decompression algorithms. Distributed algorithm is a fast algorithm that can perform these tasks directly in the transform domain. Low-complexity DCT approximations employs distributed algorithm and hence it is best preferred for image and video compression. Approximate DCT have some of the disadvantages likes having only adder circuits for operations, more number of gates during implementation and high delay. Modified approximate DCT is an approximate DCT which uses efficient binary adders. Advantages of efficient binary adders include reduction in number of gate counts and logic implementation which reduce clock cycles and power consumption. By using DCT coefficients, histogram based block optimization and arithmetic coding is designed for efficient image compression. This technique is designed within the MATLAB environment and routed to FPGA device.**

***Index Terms*— Approximate DCT, Block optimization, Distributed algorithm, Image compression.**

I. INTRODUCTION

Nowadays the demand of multimedia product grows increasingly fast, these leads to insufficient bandwidth of network and storage of memory device. For this reason data compression becomes more significant, i.e.; it reduces data redundancy and save more hardware space and transmission bandwidth. DCT has a significant role in image compression because it has some properties such as real, coefficients are uncorrelated, better energy compaction property. The major difficulties in compressed DCT domain are computational complexity of image compression and decompression algorithm, high data rate and increased hardware area. Fast algorithm is developed to perform these tasks with low-complexity. DCT approximations [8] for image and video processing that employs fast algorithm, which can reduce the computational demands of DCT leading to low-power, high-speed realizations while ensuring adequate numerical accuracy.

A transform approximation for speeding up the software compression of images, here only few DCT coefficients is actually encoded. Approximation is combining the requirements of high compression and low complexity. Multiplier-free approximate DCT transforms [3] offer superior compression performance at very low circuit complexity. The computational complexity of computing the DCT can be significantly reduced by fast algorithms even then floating-point operations are still required. Floating-point operations are expensive in terms of circuitry complexity and power consumption. One way of avoiding this issue is by means of approximate transforms. An approximate DCT [8] is a variety of DCT with the 8*8 matrix space and matrices that possess low computation cost. Here cost of transformation matrix is defined as number of arithmetic operations like additions or subtractions required for its computation.

Approximation DCTs uses addition and does not have multipliers or shifter, which uses efficient binary adders instead of normal adders. Using efficient binary adders have advantages like reduction in logic implementation and the numbers of gate counts are reduced. Reduction in logic implementation and the number of gate counts proportional to the clock cycles and power consumption.

II. LITERATURE REVIEW

Several compression techniques are developed nowadays for efficient storage of image and video. Comparison of different image compression formats [9] describes various compression formats and compares their difference. Comparison of DCT and DWT of image compression techniques [6] explain the difference between the DCT and DWT. DCT has some of the advantages like better energy compaction property, real and coefficients are really uncorrelated so it is a better solution for image compression. In [6] compare the performance of DWT and DCT and finally concluded DWT is more suitable for

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compression. Shape-adaptive image compression algorithm [9] is another method for image compression but it has some disadvantages like performance degradation, increase high-order transform coefficients. A DCT approximation for image compression [8] describe the approximate DCT, i.e.; approximate DCT is nothing but here only few DCT coefficients are actually encoded. In [8] have some disadvantages like have only adder circuits for operations, more number of gates, more Delay. 1D discrete cosine transform using distributed algorithm [7], DA-based DCT architectures are suitable for VLSI implementations, low hardware circuit cost. Modified Approximate DCT transforms with efficient binary adder [2] have advantage like reduction in number of gate counts and logic implementation. Numbers of gate counts are proportional to the clock cycles and power consumption.

III. PROPOSED SYSTEM

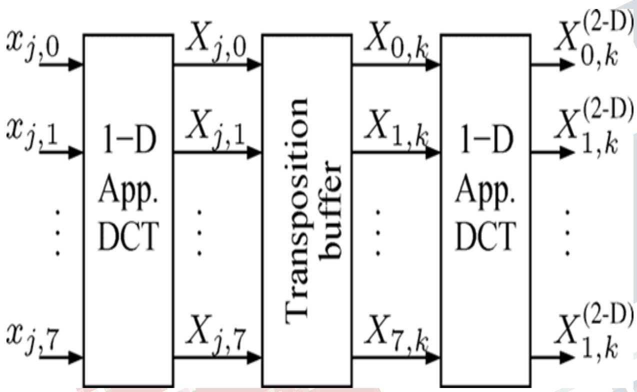

Fig. 1. Block diagram of 2D Approximate DCT

Modified approximate DCT is an approximate DCT which uses efficient binary adders instead of normal adders. Transform approximation speeds up the software compression of images and video. It is used to replace the regular DCT whenever only few DCT coefficients are actually encoded. The approximation is applicable to environments combining the requirements of high compression and low complexity. Superior compression performance at very low circuit complexity is the important feature of multiplier-free approximate DCT. Significant reductions in chip area and power consumption compared to conventional DCTs, because it consist additions and subtractions only. From Fig. 1, image Pixel values extracted as a text file is applied to the 1D DCT; it acts as a row-wise transformation while the second 1D DCT acts as a column-wise transformation. Between the DCT blocks, transposition buffer block is required. The transposition buffer is used to store the intermediate result. It ensures a data ordering method.

A. Computation of 2D –DCT

DCT equation consist of number of addition and multiplication operation it increases the complexity of implementation. In the case approximate DCT, for computing 2D DCT equation using distributed Algorithm (DA). For calculating DCT equations DA uses pre computed look-up tables and accumulators instead of multipliers. DA-based DCT architectures are suitable for VLSI implementations and low hardware circuit cost as well as low power consumption. For 2-D DCT computation of a 8x8 2-D data, first row-wise 8x1 1-D DCT is taken for all rows followed by column-wise 8x1 1-D DCT to all columns. Intermediate results of 1-D DCT are stored in transposition memory.

For a 2-D data X (p, q), 8x8 2-D DCT is given by,

$$F(a,b) = 2/8c(a)c(b)\Sigma_{p=0}^{7}\Sigma_{q=0}^{7}X(p,q)*cos(\frac{(2i+1)*a\Pi}{16}) *cos(\frac{(2j+1)*b\Pi}{16}) \quad (1)$$

$where \quad 0 \le a \le 7 and \quad 0 \le b \le 7 and \quad c(a), c(b) = 1\sqrt{2};$
$a, b = 0, c(a), c(b) = 1 otherwise.$

1-D DCT is given by,

$$F(a) = 1/2c(a)\Sigma_{i=0}^{7}X(p) * cos(\frac{(2i+1)*a\Pi}{16}) \quad (2)$$

1D DCT can be simplified as,

F(0)=[x(0)+x(1)+x(2)+x(3)+x(4)+x(5)+x(6)+x(7)]A (3)

F(1)=[x(0)-x(7)]C+[x(1)-x(6)]E+[x(2)-x(5)]F+[x(3) -x(4)]G (4)

F(2)=[x(0)-x(3)- x(4)+x(7)]B+[x(1)-x(2)-x(5)+ x(6)]D (5)

F(3)=[x(0)-x(7)]E-G[x(1)-x(6)]-C[x(2)-x(5)]-G[x(3) -x(4)] (6)

F(4)=[x(0)-x(1)-x(2)+x(3)+x(4)-x(5)-x(6)+x(7)]A (7)

F(5)=[x(0)-x(7)]F-C[x(1)-x(6]+[x(2)-x(5)]G+[x(3) -x(4)]E (8)

F(6)=[x(0)-x(3)-x(4)+x(7)]D+[x(1)-x(2)-x(5) +x(6)](-B) (9)

F(7)=[x(0)-x(7)]G-F[x(1)-x(6)]+[x(2)-x(5)]E -C[x(3)-x(4)] (10)

Where,
$A = 1/2\cos\pi/4$, $B = 1/2\cos\pi/8$, $C = 1/2\cos\pi/16$, $D = 1/2\cos3\pi/8$,
$E = 1/2\cos3\pi/16$, $F = 1/2\cos5\pi/16$, $G = 1/2\cos7\pi/16$.

Instead of computing F(0)to F(7) in parallel process, they can be computed in DA method.
Let us consider,

$$a1= x(0)+x(1)+x(2)+x(3)+x(4)+x(5)+x(6)+x(7) \quad (11)$$
$$a2=x(0)-x(1)-x(2)+x(3)+x(4)-x(5)-x(6)+x(7) \quad (12)$$
$$b1=x(0)-x(7) \quad (13)$$
$$b2=x(1)-x(6) \quad (14)$$
$$b3=x(2)-x(5) \quad (15)$$
$$b4=x(3)-x(4) \quad (16)$$
$$c1=x(0)-x(3)-x(4)+x(7) \quad (17)$$
$$c2=x(1)-x(2)-x(5)-x(6) \quad (18)$$

Substitute (11) to (18) in (3) to (10) respectively.

$$F(0) = a1A \quad (19)$$
$$F(1) = b1C + b2E + b3F + b4G \quad (20)$$
$$F(2) = c1B + c2D \quad (21)$$
$$F(3) = b1E - b2G - b3C - b4G \quad (22)$$
$$F(4) = a2A \quad (23)$$
$$F(5) = b1F - b2C + b3G + b4E \quad (24)$$
$$F(6) = c1D - c2B \quad (25)$$
$$F(7) = b1G - b2F + b3E - b4C \quad (26)$$

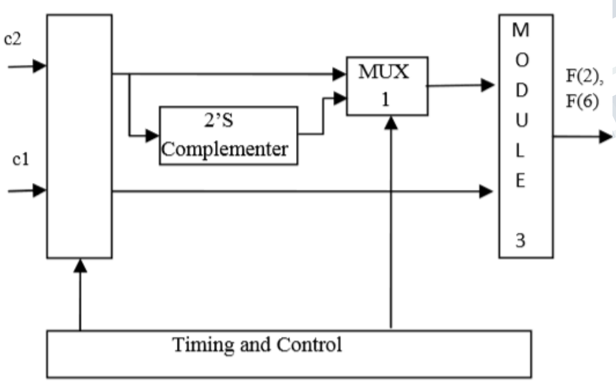

Fig. 2. Computation of F(0) and F(4)

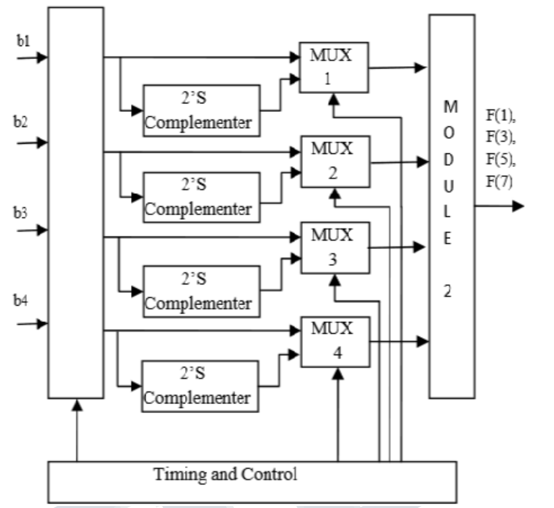

Fig. 3. Computation of F(1),F(3),F(5) and F(7)

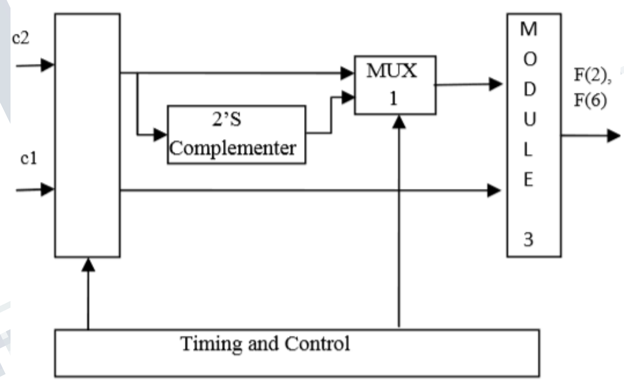

Fig. 4. Computation of F(2) and F(6)

VLSI architecture for computation of 8 point DCT is shown in Fig. 2, 3 and 4 respectively. For 8 coefficients computations three modules namely MODULE1, MODULE2 and MODULE3 is constructed. In MODULE1, (1/2)cos(π/4) is expressed in DA form with one input. According to the timing and Control signal, select either a1,a2. Remaining cosine terms are expressed in DA form with their inputs in MODULE2 and 3.

B. Transposition buffer

Two-dimensional transformation of the data is required for several compression standards. One dimensional transformation is performing at a time and the intermediate results stored in a transpose buffer. A transpose buffer may store 8x8 or smaller sized blocks of data. Smaller sized blocks can reconfigure to fit within the available space within the buffer. As a result lower bandwidth transport media to be utilized while conserving the bandwidth of higher bandwidth transport media.

Fig. 5. show the internal architecture of transposition buffer consists of registers, counters and MUXs. Existing structure consist of AND gate are eliminated in this modified structure, hence area is reduced. In the existing transposition buffer, the

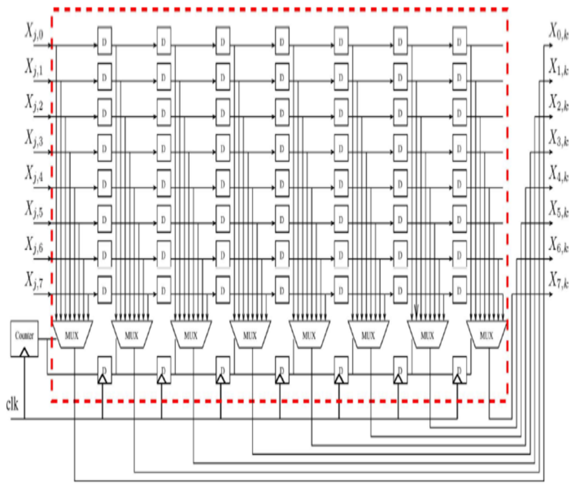

Fig. 5. Internal architecture of transposition buffer.

Enable signal is given manually hence the delay is high, here the counter is used to give the signal automatically hence delay is reduced. The counter used in the modified transform is an up counter used to load the values automatically without any delay. The counter is powered by a clock for every one tick of clock the registers values are shifted. The Multiplexers select the input lines according to select lines connected to counter.

C. Compression technique

An efficient algorithm based on histogram based block optimization and arithmetic coding is designed for image compression [5]. Fig. 6. Shows the block diagram of compression technique, here block preparation can be done by using DCT coefficient. In block preparation, first find the maximum and minimum pixel value from the DCT coefficients then compute the range(R)=max-min and set the block size(R*R). Then finds the histogram of the block and arithmetic coding is to be done, after that the compression image is obtained.

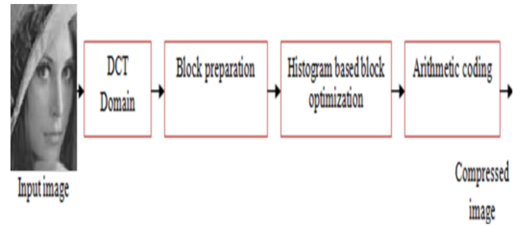

Fig. 6. Block diagram of compression technique.

IV. EXPERIMENTAL RESULT

To perform simulation of modified approximate DCT, first the Pixel values are extracted as text file using MATLAB function. After extraction the following steps are performed,

- Simulation of 1D DCT
- Simulation of transposition buffer
- Simulation of 2D DCT

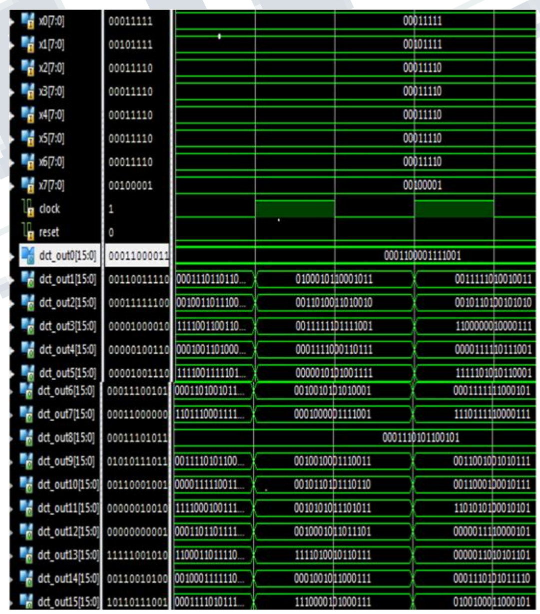

Fig. 7. Simulation result of Modified Approximate DCT

After performing the simulation of modified approximate DCT, the input image pixel values are converted into the frequency domain. By using DCT coefficients, histogram based block optimization and arithmetic coding is to be designed for efficient image compression. Simulation is done in Xilinx ISE Design suite 13.2.

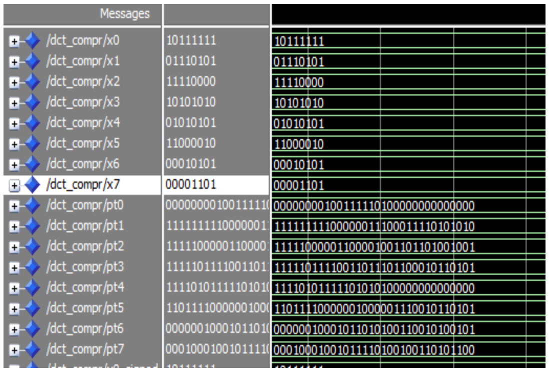

Fig. 8. Simulation result of DCT based image compression

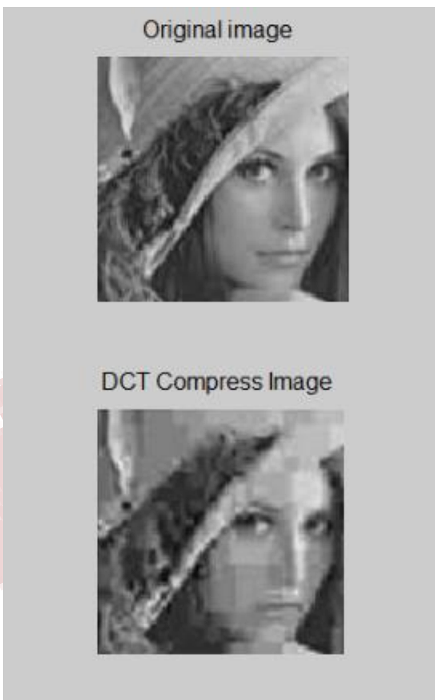

Fig. 3. MATLAB result of DCT based image compression

V. CONCLUSION

Images contain more number of pixel values and hence take up a larger bandwidth and longer time for uploading and downloading. Digital Image Compression helps in reducing the storage space required by an image file. DCT plays fundamental role in signal processing and is a part of modern image and video standards, such as JPEG, MPEG-1, MPEG-2, H.261, HEVC etc. But DCT has some limitations; it can be overcome by using transform approximation here only few DCT coefficients are actually encoded. Multiplier-free approximate DCT transforms reduces the complexity and it can be realized in digital VLSI hardware. The main advantages of modified approximate DCTs are reduction in chip area and power consumption. As an extension of this work, reconstruction of original image can be done using decoding algorithm.

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