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Hardware Simulation for Bio-Signal Acquisition System

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***Abstract*- Designing an amplifier board for Bio-signal amplification and filtering requires both software based simulation and hardware implementation of design and testing. There are many tools available today like LabView™, multisim™ etc for software simulation with available components. But hardware testing becomes difficult as the bio-signals are very low amplitude and low frequency signals and can be easily affected by coupling noise running through wires on breadboard and in the surrounding. The final testing requires PCB fabrication with proper noise reduction. It is a much time consuming and costly process as it requires multiple PCB to be fabricated for testing of each design. To solve this issue a single simulation board is designed in which all the stages in Bio-Signal amplifier stages are designed with proper noise reduction techniques. Multisim™ is used for simulation of each stage and final PCB is designed with proper noise reduction.**

***Index Terms*— RFI/EMI noise, Right Leg Drive (RLD) implementation for better CMRR, Filter Design and Decoupling in amplifier stages**

I. INTRODUCTION

BIO-SIGNAL are the measurement of time-varying magnitude of electric field generated by different regions of body. The purpose of the amplifier board design is to amplify these signals up to a level from which it can be converted to readable data and also to remove the noise signals that come at the electrode surface. While designing EEG amplifier board I found that many stages are common in every Bio-signal amplifier board design.

After understanding the concepts of all the stages and the requirements for changing in the design stages improvements. A simulation board is designed with all the design considerations stacked up together where different design changes can be implemented and tested. For explaining the design requirements a low cost amplifier board with filter designs is simulated for EEG to reduce coupling effect, low frequency noise and to remove RFI/EMI noise. Proper grounding techniques are implemented in PCB Layout Design to minimize the RFI/EMI noise.

This paper is divided as follows: chapter II specifies the problem definition; chapter III gives the motivation for this design; chapter IV outlines the literature review; chapter V details the actual design and the tests that are run to verify the design; chapter VI briefly outlines the PCB design; chapter VII discusses the result and finally, the chapter VIII gives the conclusion.

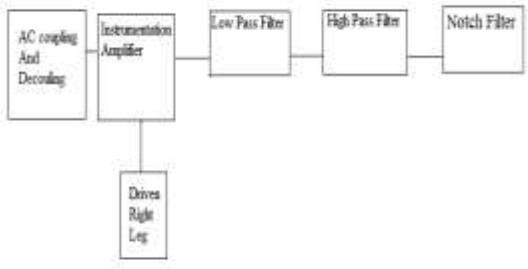

Fig. 1. Simulation board system diagram

Problem statement

Bio-signal Amplifier boards require hardware testing before fabrication for multiple designs. This simulation board provides a solution to reduce the cost and time requirement for PCB Fabrication for testing of multiple designs.

Motivation

While working on my EEG amplifier board I faced the issue of lack of Hardware board that can be used for testing of my Amplifier board designs. Breadboards are highly susceptible to noise and were useless in proper testing of design. Thus a proper simulation board was required for testing.

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Literature survey

For understanding the concepts of medical instrumentation [1] [2] are referred to understand the basic concepts for designing an acquisition board for making proper modifications in available designs. [10] This paper gives the design information of different stages in acquisition board design and their simulation. For designing the filter stage[9] is referred, it gives information about multi feedback filter design and equations for easy calculation of components. For designing RLD [3] [4][5] are referred. Calculation of filter stage and proper implementation inverting stage with high enough gain is necessary for better CMRR. For understanding the concepts of ac coupling and decoupling and there concepts in PCB design [6][7][8][9] are referred. These papers help in proper implementation of amplifier stages and calculation of component values. It helps in reducing the other noise sources like power line noise and coupling noise.

Design and test

EEG signals are very low amplitude (10µV to 150µV) random signals easily affected by noise from different sources. EEG signals come within 100HZ frequency range as given in the table below.

Name	Frequency(Hz)	Association
Delta	1-4	Sleep, repair, complex problem solving
Theta	4-8	Creativity, insight, deep states
Alpha	8-12	Alertness, peacefulness, readiness, meditation
Beta	13-21	Thinking, focusing, Sustained attention
SMR	12-15	Mental alertness, physical relaxation
High Beta	20-32	Intensity, hyper alertness, Anxiety
Gamma	30-70	Cognitive processing, Learning

The design consists of following subsections:

AC coupling and decoupling capacitors

Any DC level shift at input results in a high shift at output stage that can make the signal not detectable. Also various RFI/EMI noise and low frequency noise can attenuate the signal.

To solve DC level shift AC coupling capacitors are used at the input stage with proper DC return path through resistor connected to ground. Design requires a large capacitor for small impedance at frequency of interest.

$$Z_c = 1/jwc \qquad (1)$$

Also it requires capacitor to be small enough to avoid self resonance.

With a low resistor value and higher input capacitors it provides the 3db corner frequency (F-3db = 1.59Hz).

$$F_{-3db} = 1/2\pi RC \qquad (2)$$

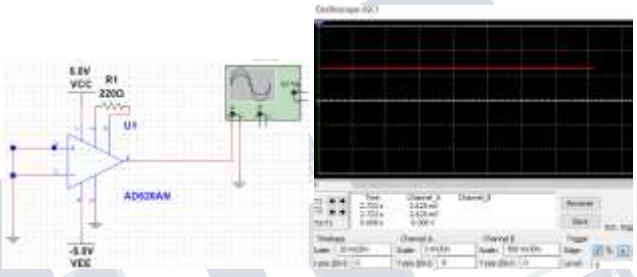

Fig. 2.Simulation is done using AD620 instrumentation amplifier in multisim™ that shows a DC offset of 2.6mv without any AC coupling at input.

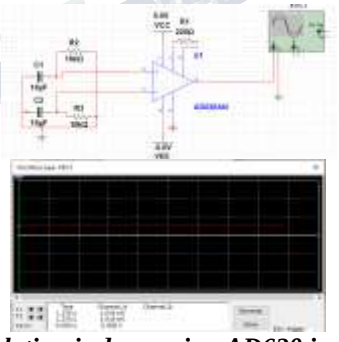

Fig. 3.Simulation is done using AD620 instrumentation amplifier in multisim™ that shows a DC offset of 1.019mv with AC coupling at input.

Decoupling capacitors are used for removal of RFI/EMI interference. The filter forms a bridge circuit whose output appears across in-amps input pins. Any mismatch between C4/R2 and C5/R3 results in unbalanced bridge that will reduce high frequency CMR. C3 is placed in parallel with the series combination of C4 and C5 for reducing low frequency CMR errors.

The differential bandwidth due to capacitor C3 parallel to the series combination of C4 and C5 is designed to be 400Hz.

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$$BW_{diff} = 1/2\pi R(2C_3 + C_4) \quad (3)$$

The Common mode bandwidth seen between the two inputs with RF inputs is designed to be 40 KHz.

$$BW_{cm} = 1/2\pi R_2 C_4 \quad (4)$$

Gain of instrumentation amplifier stage is 47dB.

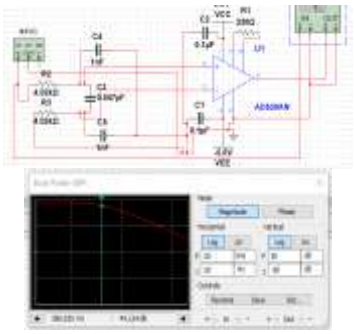

Fig. 4. Simulation of AD620 in differential mode with decoupling capacitors in multisim™ cut off is observed above 400Hz as can be seen in the bode plot.

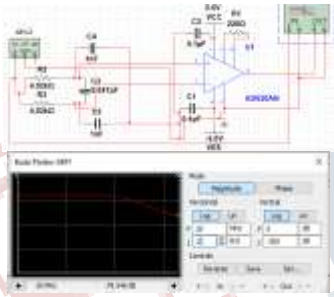

Fig. 5. Simulation of AD620 in common mode with decoupling capacitors in multisim™ cut off is observed above 40KHz gain is reduced from -38.719db at that frequency to -79.546db at higher frequency as can be seen in the bode plot.

II. INSTRUMENTATION AMPLIFIER

Instrumentation amplifiers are used in designing biomedical signal processing devices for their high CMRR and PSRR.

In this design AD620AN is used having the CMRR and PSRR above 100db. Different protection and filter circuits are implemented at this stage. Different parameters related to noise and gain at this stage is calculated. These calculations are necessary for understanding DC offset effect, effect of Johnson noise due to resister and current and voltage noise.

Since the EEG signals are very low amplitude signals proper checking of noise is necessary. Different noise sources associated with instrumentation amplifier is calculated using AD620 datasheet.

Gain equation is

$$G = \frac{49.4k}{R_G} + 1 \quad (5)$$

$RG = 220\Omega$.

Gain = 225(47dB).

Input noise $eni = 9nV/\sqrt{Hz}$

Output noise $eni = 72nV/\sqrt{Hz}$

Total noise is calculated as:

$$\text{Total noise} = \sqrt{(rnoise)^2 + (inoise)^2 + (vnoise)^2} \quad (6)$$

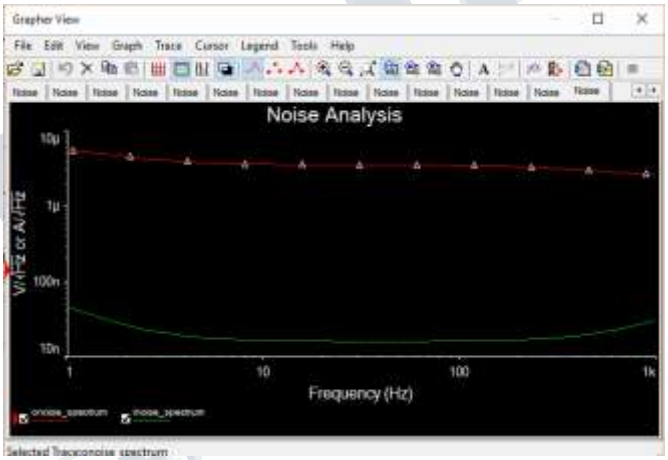

Fig. 6. Input and output Noise analysis of AD620 in multisim™ with ac coupling, decoupling and protection circuit.

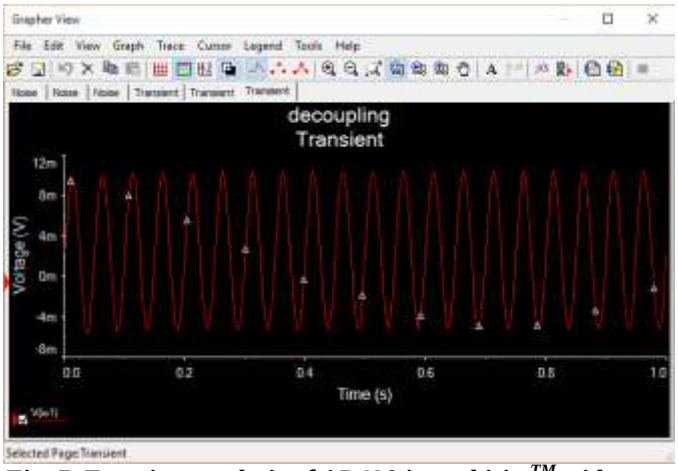

Fig. 7. Transient analysis of AD620 in multisim™ with ac coupling, decoupling and protection circuit.Vpp = 15.8mV(RMS voltage = 5.58mV).

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Observation:
Input RMS voltage = $25\mu V$
Maximum input noise = $35nV$
Maximum Output noise = $4.5\mu V$
Signal to noise ratio is calculated as:

$$SNR = SignalRMS]/[NoiseRMS] \quad (7)$$

$$SNR_{db} = 20\log([SignalRMS]/[NoiseRMS]) \quad (8)$$

Observed SNR at output = 1250(61.93dB).
Which is acceptable.

Right Leg Drive

Right leg drive is used to amplify the common mode voltage from the instrumentation amplifier and invert the signal. This signal is then feed back to the body.
Usually mastoid region or ear lobe is used in EEG acquisition system. This signal cancels out the common mode noise present inside the body thus improves the CMRR. Usually 50Hz power line noise is main noise source in India.

The first op-amp acts as a buffer and the second stage acts as a low pass filter and an inverting gain amplifier.

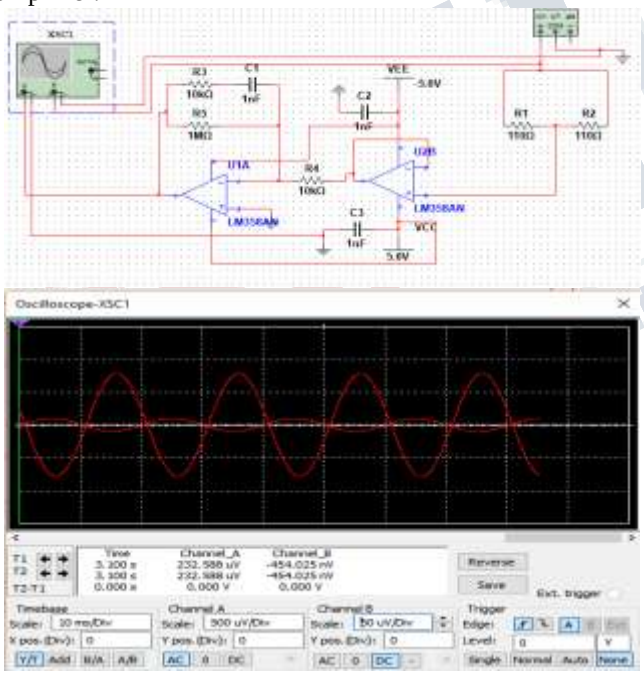

Fig. 8. RLD using LM358AN op-amp and simulation results in multisim^{TM}. The resistors R1 and R2 are connected to pin1 and pin8 of AD620AN. Simulation shows the common mode input signal is amplified and inverted(Channel A is common mode input and channel B is amplified output) .

Low Pass Filter

Low pass filters are designed and tested with cutoff frequency of 100Hz. Multifeedback topology and Sallen key topology both are designed and simulated using multisim.

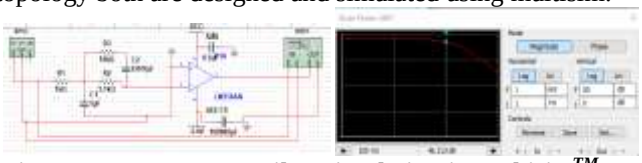

Fig. 9. MFB Low Pass Filter simulation in multisim^{TM}. As seen in the simulation 3dB cutoff is observed at frequency of 100Hz.

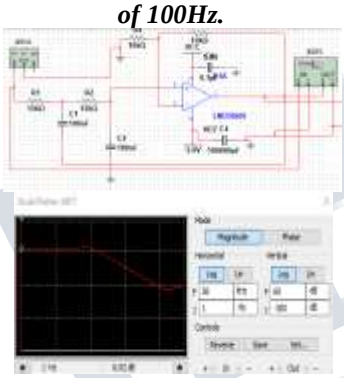

Fig. 10. Sallen Key Low Pass Filter simulation in multisim^{TM}. As seen in the simulation 3dB cutoff is observed at frequency of 100Hz.

High Pass Filter

A first order active High Pass is designed and tested with available components for a cut-off frequency of 0.72Hz and a gain of 10.

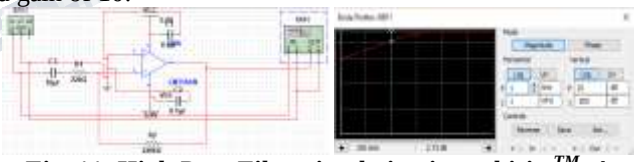

Fig. 11. High Pass Filter simulation in multisim^{TM}. As seen in the simulation 3dB cutoff is observed at frequency of 0.72Hz.

Notch Filter

Twin T notch filter is designed and tested with available components for a cut-off frequency of 50Hz and gain of 1. This stage is required to remove the 50Hz power line noise.

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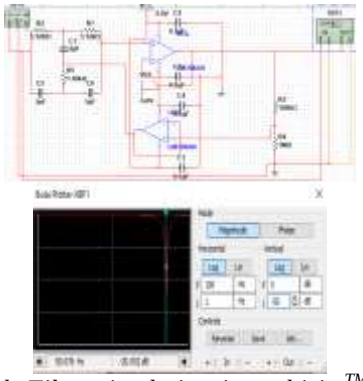

Fig. 12. Notch Filter simulation in multisim™. As seen in the simulation cutoff is observed at frequency of 50Hz.

PCB design

Proper placement of decoupling capacitors is done also no two signal lines are overlapping in different layers. The ground wires are placed in bottom layer and they are the only lines overlapping signal lines. This design strategy provides extra RFI reduction and protects signal line from coupling. PCB dimension is 4.169x3.7 inch (fig13) and 3.221x3 inch (fig14).

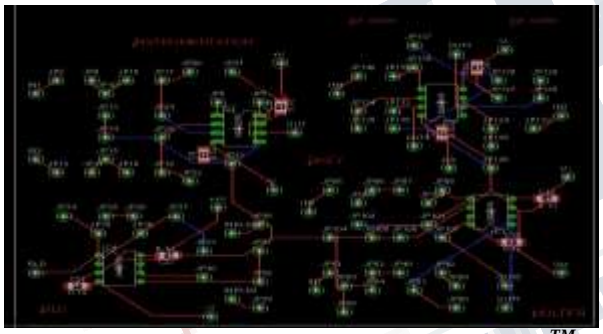

Fig. 13. PCB layout of designed circuit in Eagle™

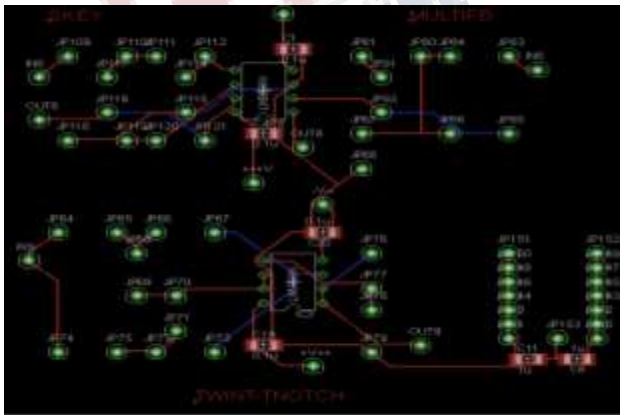

Fig. 14. PCB layout of designed circuit in Eagle™

III RESULT

The final PCB board is designed with each stage placed properly on the board for easy implementation of design. Proper noise reduction techniques are implemented in PCB layout. Each stage and power supply is properly decoupled.

IV CONCLUSION

The Simulation Board is compatible with 8DIP instrumentation amplifier. Various filter designs can be implemented with 1st order and 2nd order Multiple Feedback/Sallen key topology for up to 10th order. There are two filters designs are provided for each of the three topology. All the stages can be designed and tested separately and also in combination and improvements can be done at any design stage.

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