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Study & Performance of a Low Power High Speed Full Adder Using GDI Multiplexer

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Abstract:- **The binary adder is a critical element in the most digital circuit design including the digital signal processors (DSP) and the microprocessor data path units. As such as extensive research that continues to be focused on improving power delay performance of an added. This paper proposes new technology for implementing the low power full adder by using a set of Gate Diffusion Input (GDI) cell based multiplexers. Full adder is the very common example of combinational circuits and is most widely used in the Application Specific Integrated Circuits (ASICs). It is always advantageous to have low power action for sub components that can be used in VLSI chips. The explored technique of this realization achieves a low power high speed design for the widely used sub component full adder. Simulated outcome using state of art simulation tool represents very finer behavioral performance of a projected method over standard CMOS based full adder approach. Power, area and speed comparisons between conventional and proposed full adder are also presented.**

Keywords— **Low power full adder, 2-Transistor GDI MUX, ASIC (Application Specific Integrated Circuit), 12-TFA, CMOS (Complementary Metallic Oxide Semiconductor).**

I. INTRODUCTION

The binary addition is the basic arithmetic operation in digital circuits and it became critical in most of the digital systems including Arithmetic and Logic Unit (ALU), microprocessors and Digital Signal Processing (DSP). At present, the research keeps on increasing the adder's delay overall performance. In lots of realistic applications like mobile and telecommunication, with the tremendous progress of modern-day electronic system and the evolution of the nanotechnology, the low- power & high speed microelectronic devices have come to the leading edge. Now a day, as developing applications (better complexity), speed and portability are the fundamental concerns of any smart device it always demands for small-size, low-energy high throughput circuitry. So, sub circuits of any VLSI chip needs high speed operation at the side of low-power intake. Now a day logic circuits are designed using pass transistor logic techniques.

In PTL based VLSI chips MOS switches are used to propagate specific logic values in various node factors, as it reduces area and delay compared to any other switches type [1]. It reduces the variety of MOS transistors used in circuit, however it suffers with a major problem that output voltage levels is no longer identical as the input voltage level. Each transistor in series has voltage decrease at its output than at its input [2]. That allows you to minimize sneak paths, charge sharing, and switching delays of the circuit all of the sub-circuit component must be arranged obeying the VLSI layout regulations. Ensuring this simulation of circuit schematics affords a platform to verify circuit overall performance [3]. To get higher speed and power intake effects lot of procedures have been recently proposed [4]-[7]. Among them, they have been established by Hitachi CPL [4] and DPL [6]. In 1993 Hitachi demonstrated a 1.5ns 32-bit ALU in 0.25μm CMOS technology [6] and 4.4ns 54X54 bit multiplier [7] by the usage of DPL method. Like Pass Transistor Logic (PTL), Domino logic, NORA logic, Complementary Pass Logic (CPL), Differential Cascaded Voltage Switch (DCVS), MOS Current Mode Logic (MCML), Clocked CMOS (C2MOS etc.[8][9] are also different approach for reducing the circuit power. In 2002, A.Morgenshtein, A. Fish, and Israel A. Wagner introduced a new method for low-power digital combinational circuit design known as Gate Diffusion Input (GDI) [10]. The primary reason of this work is to implement a low power GDI based full adder & to draw an in depth comparative study with a CMOS full adder.

The purpose of implementing the low power full adder is to expose that the use of fewer numbers of transistors in evaluation to the conventional full adder, the propagation delay time & power intake gets reduced. It also

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facilitates in reducing the layout area thereby lowering the entire size of a device where this adder is used. Power consumption is turning into the foremost tailback in the design of VLSI chips in cutting-edge system technologies. Those are evaluated from an industrial product development perspective.

II. EXISTING DESIGN

While taking account of full adder the sum and carry outputs are represented as the sub sequent combinational Boolean functions of the three input variables A, B and C.

Sum = A xor B xor C ---------- eqn.1
Carry = AB + AC + BC ------- eqn.2

GDI approach primarily based full adder have advantages over full adder using pass transistor logic or CMOS logic and is classified via tremendous speed and low power. The technique has been described below

Thus the functions can be represented by using CMOS logic as follows in fig.1,

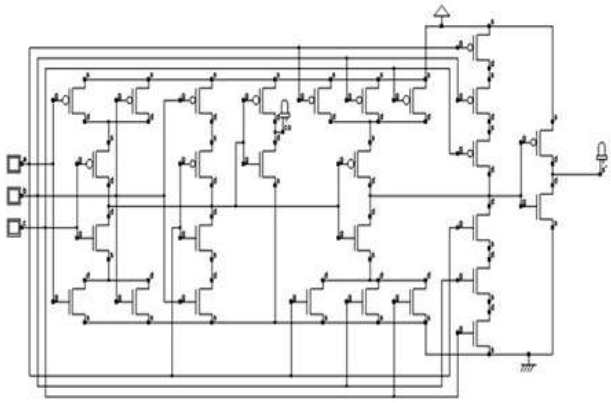

Fig.1. Conventional 28-T CMOS 1 bit full adder

III. GATE DIFFUSION INPUT (GDI)

GDI cell:

The GDI technique offers realization of giant variety of logic functions using two simple transistor based circuit association. This scheme is appropriate for fast and low strength circuit design, which reduces variety of MOS transistors in comparison to CMOS and other existing low power strategies, while the logic stage swing and static power dissipation improves. It also permits easy top- down approach by means of small cellular library [5]. The primary cellular of GDI is shown in Fig. 2.

1) The GDI cell consists of one nMOS and one pMOS. The structure looks like a CMOS inverter. Although in case of GDI both the sources and corresponding substrate terminals of transistors aren't linked with supply and it could be randomly biased.

2) It has 3 input terminals: G (nMOS and pMOS shorted gate input), P (pMOS source input), and N (nMOS source input). The output is taken from D (nMOS and pMOS shorted drain terminal) [11].

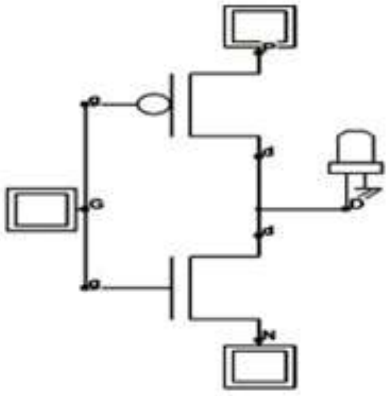

Fig.2. GDI basic cell consisting of PMOS and NMOS

GDI logic style approach consumes much less silicon area in comparison to other common logic styles as it consists of less transistor count number. In view of the fact that, the area is much less, the value of node capacitances might be much less and for this reason GDI gates have faster operation which presents that GDI logic style is a power efficient approach of design.

We can realize different Boolean functions with GDI primary cell. Table I shows how different Boolean features can be realized by means of use of different input arrangements of the GDI cell.

TABLE.I. GDI Cell Based Various Logic Functions Using Different Input Configurations And Corresponding Transistor Counts

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N	P	G	OUTPUT	FUNCTION	TRANSISTOR COUNT
0	1	A	A'	Inverter	2
0	B	A	$A'B$	F1	2
B	1	A	$A'+B$	F2	2
1	B	A	$A+B$	OR	2
B	0	A	AB	AND	2
C	B	A	$A'B+AC$	MUX	2
B'	B	A	$A'B+B'A$	XOR	4
B	B'	A	$AB+A'B'$	XNOR	4

IV.ARCHITECTURE OF PROPOSED GDI FULL ADDER

The primary structure of the 2:1 MUX using GDI technique is shown in the fig. 3. On this configuration we've connected PMOS and NMOS gate along with a SEL line 'A', as in MUX. As we know that PMOS works on active LOW and NMOS works on active HIGH. So, when the SELECT input is low (0) then the PMOS gets activated, and show the input 'B' in the output and because of low input (0) the NMOS stands idle, as it's activated in high input.

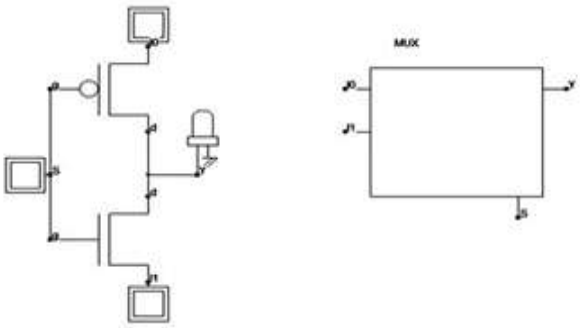

Fig.3.Basic view of 2T MUX using GDI technique

Same for the case, at the same time as the G input is high (1) then the NMOS get activated, and show the input 'C' on the output. Thus this circuitry behaves as a 2-input MUX using 'A' as SEL line, and suggests the favorable output as 2:1MUX.

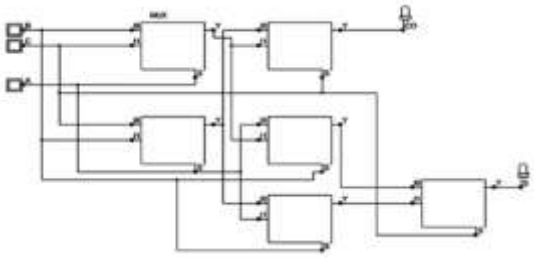

Fig.4. Block Diagram of Low Power Proposed Full Adder using 2T MUX

Now we are implementing the low power full adder circuit with the assist of 2T MUX, made by GDI process. Generally It require 6 numbers of 2T MUX having equal characteristics to design a 12T full adder and connected as above in fig.4 [5]. The truth table for the above circuit taking every MUX into consideration are shown in table II, and from there it generates 6 various outputs of various MUX.

TABLE.II. TRUTH TABLE OF LOW POWER F-A USING 2T MUX

A	B	Cin	MUX1	MUX2	MUX3	MUX4	MUX5	MUX6	SUM	Cout
0	0	0	0(B)	0(Cin)	0(Cin)	0(A)	0(Cin)	0(A)	0(A)	0(Cin)
0	0	1	0(B)	1(Cin)	0(B)	0(A)	1(Cin)	1(Cin)	1(Cin)	0(B)
0	1	0	1(B)	0(Cin)	0(Cin)	1(B)	0(A)	1(B)	1(B)	0(Cin)
0	1	1	1(B)	1(Cin)	1(B)	1(B)	0(A)	0(A)	0(A)	1(B)
1	0	0	0(Cin)	0(B)	0(B)	1(A)	0(B)	1(A)	1(A)	0(B)
1	0	1	1(Cin)	0(B)	1(Cin)	1(A)	0(B)	0(B)	0(B)	1(Cin)
1	1	0	0(Cin)	1(B)	1(B)	0(Cin)	1(A)	0(Cin)	0(Cin)	1(B)
1	1	1	1(Cin)	1(B)	1(Cin)	1(Cin)	1(A)	1(A)	1(A)	1(Cin)

V.LOGIC ANALYSIS

The digital circuit shown within the fig. 4 may be analyzed logically with the assist of simple Boolean algebra. The outputs of each MUX can be analyzed to get the sum & carry.

Logic transition, short-circuit current and leakage current are the 3 most important sources of power dissipation in CMOS VLSI circuits [6], [7]. At the stage in the transition of output from one logic level to different each the NMOS and PMOS transistors become active and offers a short circuit path without delay between supply to

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ground which increases the power intake of the circuit [2], [6].

$$MUX1 = (B\bar{A} + CA)$$
$$MUX2 = (C\bar{A} + BA)$$
$$MUX3 = [(C\bar{A} + BA)\bar{C} + (B\bar{A} + CA)C]$$
$$= AB\bar{C} + \bar{A}BC + AC = AB\bar{C} + \bar{A}BC + AC(B + \bar{B})$$
$$= AB\bar{C} + \bar{A}BC + ABC + A\bar{B}C$$
$$= AB\bar{C} + ABC + \bar{A}BC + ACB + A\bar{B}C + ABC$$
$$= AB(C + \bar{C}) + BC(A + \bar{A}) + AC(B + \bar{B})$$
$$= AB + CB + AC = Cout$$
$$MUX4 = \bar{A}\bar{B} + (\bar{A}B + AC)B$$
$$MUX5 = (C\bar{A} + BA)\bar{B} + AB$$
$$MUX6 = [\bar{A}\bar{B} + (\bar{A}B + AC)B]\bar{C} + [(C\bar{A} + BA)\bar{B} + AB]C$$
$$= A\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}\bar{B}C + ABC = A \oplus B \oplus C = Sum$$

As the proposed 12-T full adder is made from GDI based MUX , it doesn't provide direct connections among supply and ground, so the opportunity of a getting short circuit current during switching may be appreciably decreased; i.e., the energy intake due to short circuit current is considerably small. Again, in the proposed 12T full adder, all the select line of the MUX i.e. the G nodes of the GDI cells are directly connected with the input signals, results a much faster transition (much less delay) in its output alerts. As a result, the energy intake of the final pad out degree is low and it could provide fast Sum and Cout outputs.

VI.SIMULATION RESULTS

All the simulations are achieved on Micro wind and DSCH 3.5. The principle recognition of this work is to meet all challenges faces in designing of full adder circuit, the power and area in proposed MUX primarily based full adder is advanced as compared to conventional full adder. The simulation results are shown in the below figures.

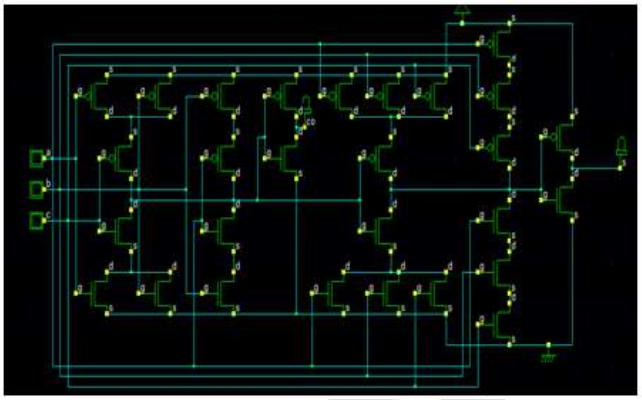

Fig 5: Schematic of 28TFull adder

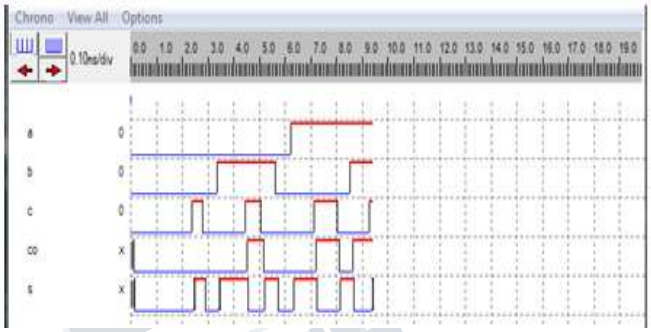

Fig 6: Timing Diagram of 28T Full adder

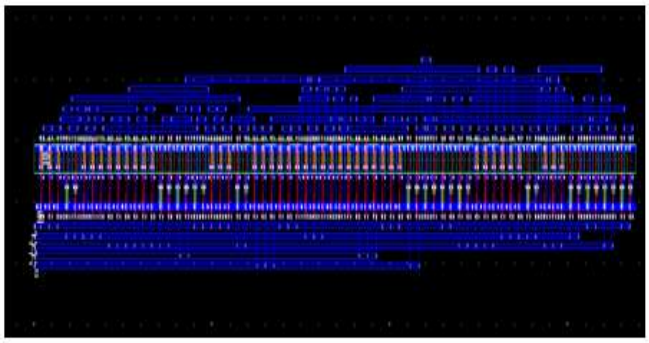

Fig 7: Layout of 28TFull adder

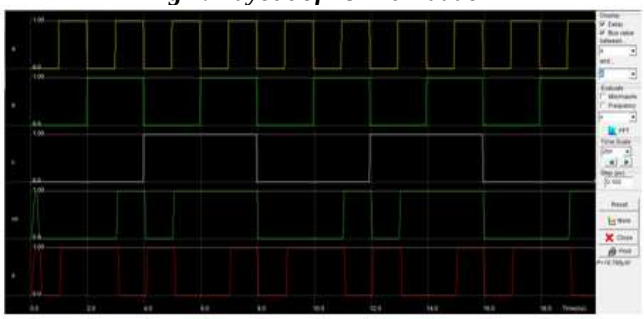

Fig 8: Simulation of Layout of 28TFull adder

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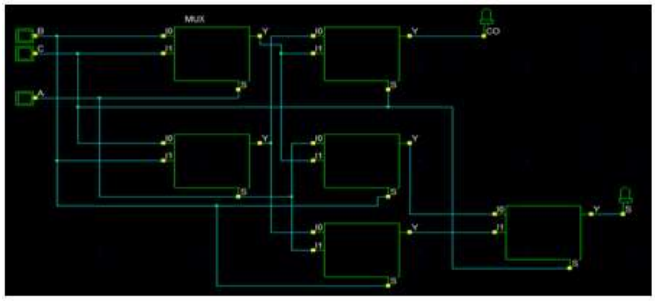

Fig 9: Schematic of 12TFull adder

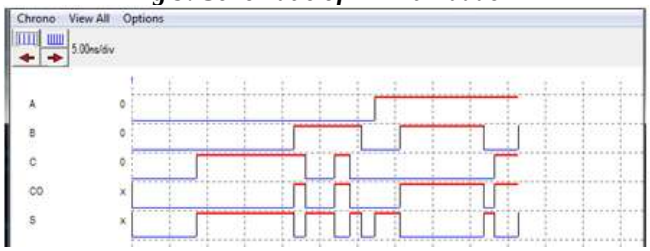

Fig 10: Timing Diagram of 12TFull adder

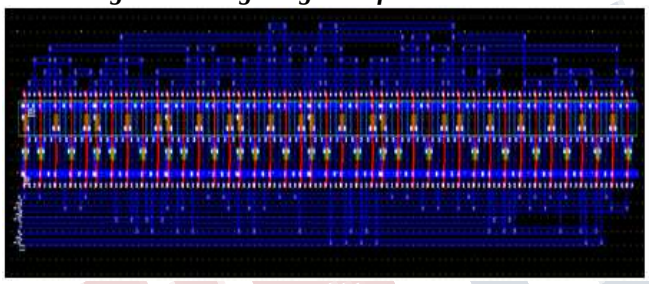

Fig 11: Layout of 12TFull adder

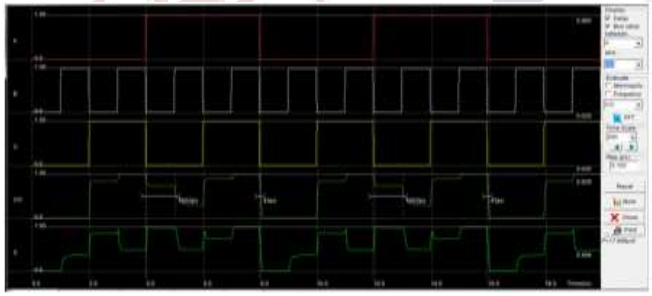

Fig 12: Simulation of Layout 12TFull adder

VII. CONCLUSION

From the above results it could be concluded that our proposed full adder has got higher performance in postpone, energy and area consideration in assessment with conventional full adder. It indicates that during contrast to different conventional strategies, this approach is better and it'll be more suitable for commercial practice in complex procedure technologies.

REFERENCES

[1] Jaume Segura, Charles F. Hawkins CMOS electronics: how it works, how it fails, Wiley-IEEE, 2004, page 132

[2] Clive Maxfield Bebop to the Boolean boogie: an unconventional guide to electronics Newnes, 2008, pp. 423-426

[3] Albert Raj/Latha VLSI Design PHI Learning Pvt. Ltd. pp. 150-153

[4] Yano, K, et al, "A 3.8 ns CMOS 16*16b multiplier using complementary pass transistor logic", IEEE J. Solid State Circuits, Vol 25, p388-395, April 1990

[5] Yingtao Jiang, Abdulkarim Al-Sheraidah, Yuke Wang, Edwin Sha, and Jin-Gyun Chung, "A Novel Multiplexer-Based Low-Power Full Adder" IEEE Transaction on circuits and systems-II: Express Brief, Vol. 51, No. 7,p-345, July- 2004

[6] Makoto Suzuki, et al, "A 1.5 ns 32 b CMOS ALU in double pass transistor logic", ISSCC Dig. Tech. Papers, pp 90-91, February 1993.

[7] N. Ohkubo, et al, "A 4.4 ns CMOS 54X54 b multiplier using pass transistor multiplexer", Proceedings of the IEEE 1994 Custom Integrated Circuit Conference, May 1-4 1994, p599-602, San Diego, California.

[8] Mohamed W.Allam, "New Methodologies for Low-Power High Performance Digital VLSI Design", PhD. Thesis, University of Waterloo, Ontario, Canada, 2000

[9] A.Bazzazi and B.Eskafi, "Design and Implementation of Full Adder Cell with the GDI Technique Based on 0.18µm CMOS Technology", International Multi Conference of Engineers and Computer Scientists (IMES) Vol II, March 17 - 19, 2010, Hong Kong

[10] Arkadiy Morgenshtein, Alexander Fish, and Israel A. Wagner, "Gate Diffusion Input (GDI): A Power-Efficient Method for Digital Combinatorial Circuits", IEEE Transaction on VLSI Systems, Vol. 10

[11] Dan Wang. "Novel low power full adder cells in 180nm CMOS technology", 2009 4th IEEE Conference on Industrial Electronics and Applications, 05/2009.

ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
Vol 3, Issue 7, July 2016

[12]L.Bisdounis, D.Gouvetas and O.Koufopavlou, "A comparative study of CMOS circuit design styles for lowpower high-speed VLSI circuits" Int. J. of Electronics, Vol.84, No.6, pp 599-613,1998. Anu Gupta, Design Explorations of VLSI Arithmetic Circuits, Ph.D. Thesis, BITS,Pilani, India, 2003.

[13]R.Uma and P. Dhavachelvan," Modified Gate Diffusion Input Technique: A New Technique for Enhancing Performance in Full Adder Circuits" 2nd International Conference on Communication, Computing & Security [ICCCS-2012].

[14] R.uma, Vidya Vijayan, M. Mohanapriya, Sharon Paul, Area, Delay and Power Comparison of Adder Topologies

[15] M. Aguirre and M. Linares, "An alternative logic approach to implement high-speed low-power full adder cells," in *Proc. SBCCI*, Florianopolis,Brazil, Sep. 2005, pp. 166–171.

[16] A. M. Shams and M. Bayoumi, "Performance evaluation of 1-bit CMOS adder cells," in *Proc. IEEE ISCAS*, Orlando, FL, May 1999,vol. 1, pp. 27–30.

[17] I. S. Abu-Khater, A. Bellaouar, and M. I. Elmastry, "Circuit techniques for CMOS low-power high-performance multipliers," *IEEE J. Solid-State Circuits*, vol. 31, pp. 1535–1546, Oct. 1996.

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