

Detection and Correction of Multiple Bit Errors in SRAM Based FPGA Frame

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Abstract: -- Recent studies suggest that multiple bit upsets (MBUs) are a significant part of the error events in advanced memory technologies and that they will continue to grow in the next technology nodes. The errors in an MBU are normally caused by the same physical event and therefore affect memory cells that are close together. Existing techniques employ error correction codes with considerably high overhead to mitigate MBUs in configuration frames. In this paper, we present a low-cost error-detection code to detect MBUs in configuration frames as well as a generic scrubbing scheme to reconstruct the erroneous configuration frame based on the concept of erasure codes. The proposed scheme does not require any modification to the FPGA architecture. Implementation of the proposed scheme on a Xilinx Virtex-6 FPGA device shows that the proposed scheme can detect 100% of MBUs in the configuration frames with only 3.3% resource occupation, while the recovery time is comparable with the previous schemes.

Index Terms— FPGA, Multiple bit upsets, Reliability, Soft errors

I. INTRODUCTION

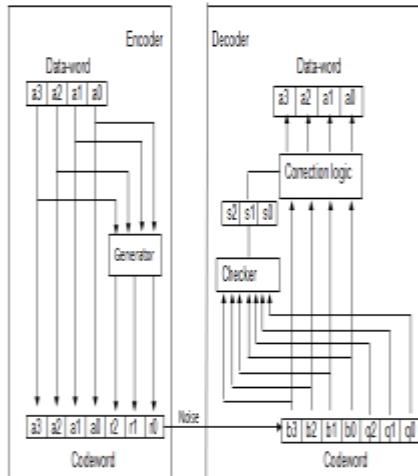
SRAM-BASED field-programmable gate arrays (FPGAs) are widely used in a variety of application domains due to short time-to-market time, flexibility, high density, and cost efficiency. However, increasing transistor count per chip (i.e., Moore's law) coupled with the reduced operating voltage in the past years results in an exponential growth in soft error rate (SER) of digital circuits. More specifically, SRAM-based FPGAs are more prone to soft errors as a particle strikes in a configuration frame has a permanent impact on the functionality of the mapped design. Based on the fact that error detection can be done at much lower cost than error correction, we propose the MBU detection technique to detect the erroneous configuration frame during configuration scrubbing. Once an error is detected, by taking advantage of erasure codes and using the data stored in a redundant frame, the correct contents of the affected configuration frame are reconstructed.

Error detection and correction or error control is the techniques that enable reliable delivery of digital data over unreliable communication channels. Many Communication Channels are subject to channel noise, and thus errors may be introduced during transmission from the source to a receiver. Error detection techniques allow detecting such errors, while error correction enables reconstruction of the original data in many cases. Error

detection is the detection of errors caused by noise or other impairments during transmission from the transmitter to the receiver. Error correction is the detection of errors and reconstruction of the original, error-free-data. The general idea for achieving error detection and correction is to add redundant bits that are some extra data to the message, where receivers check consistency of the delivered message, and to recover data determined to be corrupted.

II. PROPOSED SYSTEM

In order to reduce the effects of errors in the SRAM memory cell, we need to establish new proposed system to determine the errors and locate the errors. Hamming code technique is the proposed technique to identify the errors which is single, double, double adjacent errors, triple and quadruple errors with low cost. In existing system, more than two errors are not determined. Hamming code technique is the most well known for finding the faults in the system memory. In the proposed system, the encoded message consists of 16 message bits and the 6 parity bits. By adding the message and parity bits we get total of 22 bits. Those 22 bits can be corrected with the help of Parity check sum calculation and syndrome calculation.



*Simulation result for single bit error
Double and Parity Error*

Hardware kit consists of Zigbee transmitter, Zigbee receiver, Spartan 3E, encoder section and decoder section. The encoder section and decoder section are used to display the errors and the location of errors in the decoding section. In two way communication, hamming code with single bit error correcting and detecting is useful i.e land line communication but the hamming code technique with detection of more but with low cost is more advanced to determine errors with error free concept and location of errors occurred on the SRAM based FPGA configuration frame.

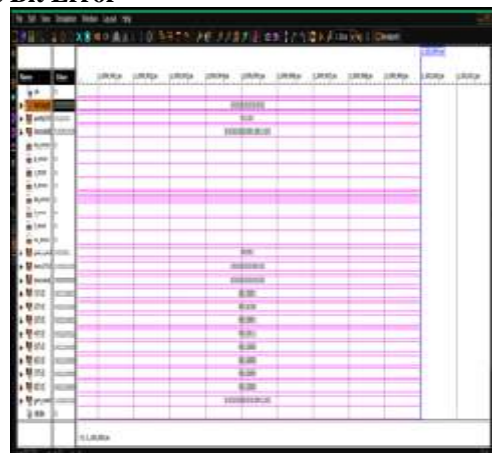
III. RESULTS

The design and implementation of multiple bit error detector and corrector by using hamming code technique is performed. The proposed hamming code decoder is used to determine the errors and location of the information bits. The simulation and synthesis was done in Xilinx ISE tool. The simulation and synthesis results are shown below. The simulated files are bringing into the synthesized tool and corresponding values of delay and area note down. The proposed scheme reduces the area and delay to a great extent.

1. Simulation Results Single Bit Error



*Simulation result for double and parity bit error
Double Bit Error*



Simulation result for double bit error

Triple Bit Error


Simulation result for triple bit error

Four Bit Error


Simulation result for four bit error

IV. ANALYSIS

Transmitter

The transmitter is used to send the information from the hyper terminal communication port in the system. The transmitted message is of 16 bits according to the ASCII table.

For example: Input message: 0100 0001 0100 0010

Receiver: The receiver section is used to receive the message bits, determine the errors and compares with the original message. The receiver section consists of encoder and decoder sections. The encoder section is used to display the single, double, triple or quadruple errors. The decoding section is used to display the location of errors and corrects the errors at particular place.

Encoder Section: The encoder section displays the message with single, double, triple, quadruple, no errors and parity errors. The original message signal is also displayed in this section.

Decoder Section: The decoder section is used to display the message on the LCD module with error location section. It

displays the error with the particular location. The decoder section is mainly used to locate the errors with 4 bit positions.

Device Utilization Summary			
Logic Utilization	Used	Available	Utilization
Number of Slice Registers	94	4800	1%
Number of Slice LUTs	117	2400	4%
Number of fully used LUT-FF pairs	58	153	37%
Number of bonded IOBs	91	102	89%
Number of BUFG	1	16	6%

Device Utilization Summary for Proposed system

V. CONCLUSION

The main objective of this project is to determine the errors in the memory cell whenever the sender sends the information and it adds to the redundancy bits to check whether it is wrong message or correct message. Most of them wants error free message. This paper is implemented for detecting and correcting the bits which have errors in the encoded message. This is mainly used in space communication, telecommunication and mobile communication systems.

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