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Dynamic Power Reduction of LFSR with Clock Gating Technology

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Abstract: **-- A modified Linear Feedback Shift Register is designed in which power consumption reduction by deactivating the clock signal to Flip Flop when the output signal is same as input signal. The power consumption of the new LFSR is reduced due to the reduced switching of Flip Flop. To verify, the maximum, minimum and average. Dynamic power management (DPM) is a design methodology for dynamically reconfiguring systems to provide the requested services and performance levels with a minimum number of active components or a minimum load on such components. DPM encompasses a set of techniques that achieves energy-efficient computation by selectively turning off (or reducing the performance of) system components when they are idle (or partially unexploited). In this paper, we survey several approaches to system-level dynamic power management. We first describe how systems employ power-manageable components and how the use of dynamic reconfiguration can impact the overall power consumption. We then analyze DPM implementation issues in electronic systems, and we survey recent initiatives in standardizing the hardware/software interface to enable software-controlled power management of hardware components.**

***Keywords*:-- LFSR optimization, low power, test pattern**

I. INTRODUCTION

Today pseudo random generators are (PRBGs) are widely used in many electronic equipment. A good PRBG must be characterized by repeatability and randomness. Today, hardware implementation of the PRBGs is almost always made up of the well-known linear-feedback shift register (LFSR) whose generic circuit is reported. This circuit is very simple to be implemented, but since the clock-path of all flip-flops (FFs) toggle at every clock cycle, they consume a significant amount of power. In this paper, we present the gated clock design approach for LFSRs which can lead to power reduction without complicating the traditionally simple topology. The main challenging areas in VLSI are performance, cost, testing, area, reliability and power. These demands for portable computing devices and communications system are increasing rapidly. These applications require low power dissipation for circuit implementation. The power dissipation during test mode is 200% more than the normal mode. Hence it is important aspect to optimize power during testing. Power optimization is one of the main challenges. There are various factors that affect the cost of chip like packaging, application, testing. In VLSI, according to thumb rule 5000 of the total integrated circuits cost is due to testing. During testing two key challenges are, Cost of testing that can't be scaled. Engineering effort for generating test vectors increases as complexity of circuit increases. Based on 1997 SIA data, the upper curve shows the fabrication cost of transistor and lower curve shows the testing cost of transistor. Figure 1 shows that the fabrication cost transistor decreases over the decades according to but the testing cost as constant..

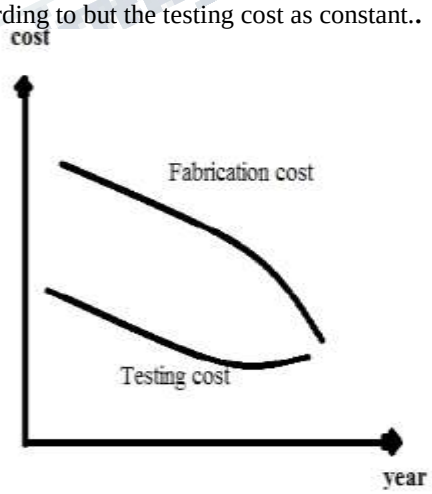

Fig: 1 Fabrication and testing cost curve

There are main two sources of power dissipation in digital circuits; these are static and dynamic power dissipation. Static power dissipation is mainly due to leakage current and its contribution to total power dissipation is very small. Dynamic power dissipation is due to switching i.e. the

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power consumed due to short circuit current flow and charging of load capacitances is given by equation: **P= 0.5 VDD 2E(SW)CL fclk** Where **VDD** is supply voltage, **E(SW)** is the average number of the main challenges. Output transitions per fclk Is the clock frequency and CL is the physical capacitance at the output of the gate. Dynamic power dissipation contributed to total power dissipation. The above equation shows the dynamic power depends on three parameters: Supply voltage, Clock frequency, switching activity. Power reduction using the switching activity doesn't degrade the performance of the circuit. During testing large power is dissipated compare to the normal mode. This is due to lack of correlation between the Successive test patterns generated by ATPG or LFST and this large power dissipation cases following effects: The increased power may be responsible for cost, reliability, performance verification, autonomy and technology. Low power dissipation during test application is thus becoming an equally important figure of merit in. For complex circuits we use hierarchical approach. The advantage of hierarchical approach is that every block is tested separately. Test input is given to each block and output is observed and verified. DFT (Design for Testability) is the action of placing features in a chip design process to enhance the ability to generate vectors, achieve a 3 measured quality level or reduce cost of testing. The conventional DFT approaches use scan and BIST. In this paper a modified low power LFSR are used in which the number of transitions of test pattern are reduced.

II.CLOCK GATING AT REGISTER TRANSFER LEVEL

Power should be optimized at all stages, but it is generally convenient to address it after Register Transfer Level (RTL).RTL clock gating is the most commonly used optimization technique for improving power consumption, but depends critically on how well a design is clock gated. At this point in the design flow, designer has flexibility in the implementation to make significant increment in the energy saving.

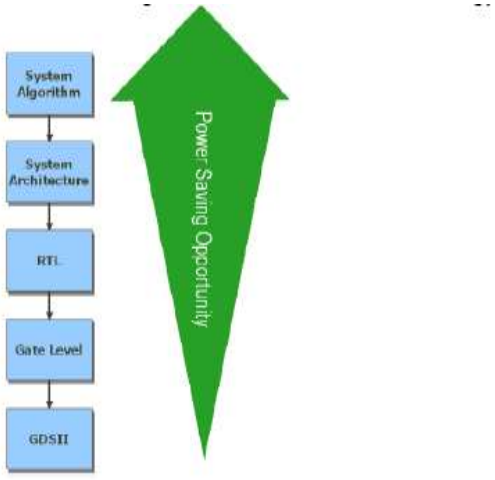

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Fig:2 various types of LFSR

Fibonacci LFSRs:In a 16-bit Fibonacci LFSR the feedback tap numbers in white correspond to a primitive polynomial so the register cycles through the maximum number of 65535 states excluding the all-zeroes state. The state shown, 0xACE1 (hexadecimal) will be followed by 0x5670. The bit positions that affect the next state are known as taps. In the diagram the taps are . The rightmost bit of the LFSR is called the output bit. The taps are sequentially with the output bit and then fed back into the leftmost bit. The sequence of bits in the rightmost position is known as output stream.

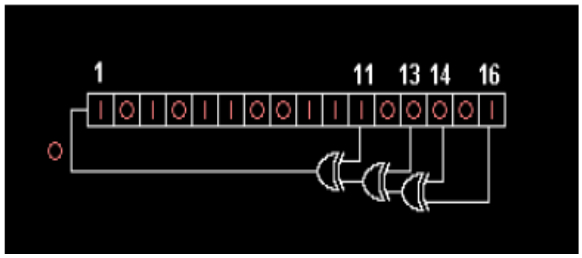

Fig 3 Linear feedback shift register

A maximum-length LFSR produces an m-sequence unless it contains all zeros, in which case it will never change. As the XOR based feedback in an LFSR, one can also use XNOR This function is an affine map, not a linear map, but it results in an equivalent polynomial counter whose state of this counter is the complement of the state of an LFSR. A state with all ones is illegal when using an XNOR feedback, same as a state with all zeroes is illegal when using XOR. This state is considered illegal because the counter would remain "locked-up" in this state. The sequence of numbers generated by an LFSR or its XNOR counterpart can be considered a binary numeral system just as valid Gray code or the binary

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code. The arrangement of taps for feedback in an LFSR can be expressed in finite field arithmetic as a polynomial mod. This means that the coefficients of the polynomial must be one's or Zeroes. This is considered as the feedback polynomial or characteristic polynomial. For example, if the taps are at the 16th, 14th, 13th and 11th bits (as shown), the feedback polynomial is The 'one' in the polynomial does not correspond to a tap — it corresponds to the input to the first bit (i.e. x0, which is equivalent to 1). The powers of the terms represent the tapped bits, counting from the left. The first and last bits are always connected as an input and output tap respectively. There can be more than one maximum-length tap sequence for a given LFSR length once one maximum-length tap sequence.

Galois LFSRS:

An LFSR in Galois configuration, which is also known as modular, internal XORs as well as one-to-many LFSR, is an alternate structure that can generate the same output data as a conventional LFSR. In this configuration, when the system is clocked, bits that are not taps are shifted one position to the right unchanged. The taps, on the other hand, are XOR with the output bit before they are stored in the next position. The new output bit is the next's input bit. when the output bit is zero all the bits in the register shift to the right unchanged, and the input bit becomes zero. When the output bit is one, the bits in the tap positions, and then the entire register is shifted to the right and the input bit becomes 1

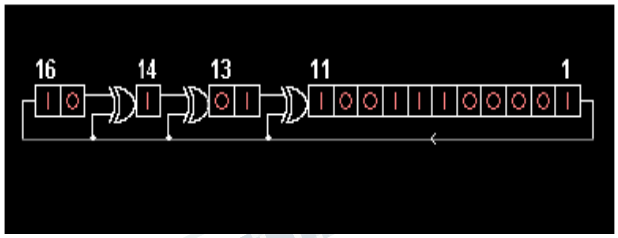

Fig 4 Galois linear feedback shift register

A 16-bit Galois LFSR. The register numbers in white correspond to the same primitive polynomial as the Fibonacci example but are counted in reverse to the shifting direction. This register also cycles through the maximal number of 65535 states excluding the all-zeroes state. The state ACE1 hex shown will be followed by E270 hex. To generate the same output stream, the order of the taps is the counterpart (see above) of the order for the conventional LFSR, otherwise the stream will be in reverse. Note that the internal state of the LFSR is not necessarily the same. The Galois register shown has the same output stream as the Fibonacci register in the first section. Galois LFSRs do not concatenate every tap to produce the new input (the XOR 'in is done within the LFSR and no XOR gates are run in serial, therefore the propagation times are reduced to that of one XOR rather than a whole chain), thus it is possible for each tap to be computed in parallel, increasing the speed of execution.

III.EXPARIMENTAL SETUP

In this we are discussing about the hardware description of the experiment

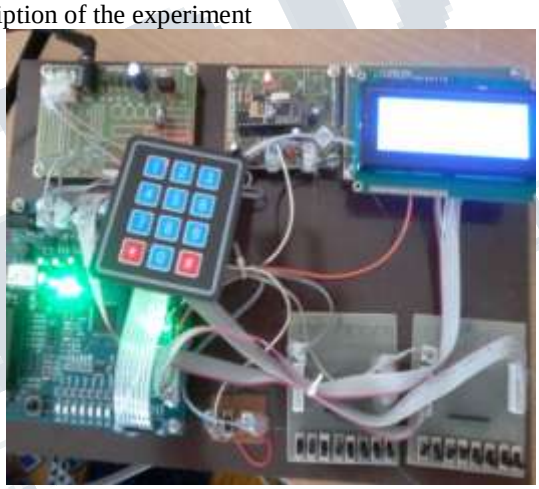

Fig 4: Experimental setup input block

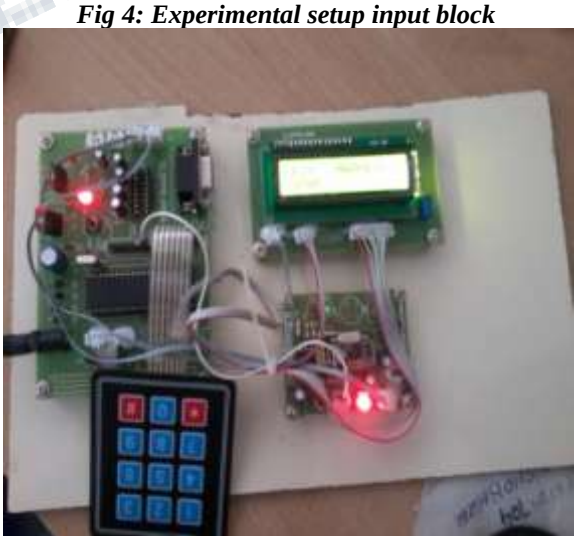

Fig 5: Experimental setup output block

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+69+/The experimental blocks consisting of 8 led displays, zigbee transmitter and zigbee receiver, push button, serial port connector, LCD display, power supply connectors, keypads. In this 8 led displays the four is fixed as high and the remaining four is fixed according to our consideration.

Steps to hardware execution:

First switch on the power supply and then ON the switch button for supplying power to experimental kit first four input is fixed as high and the remaining four inputs is fixed according to our need and generate the keys by using the keypad. and it is displays on input side lcd display and ON the zigbee transmitter, it transmit the generated key to output. and then serial port connector is connected for generating serial inputs and outputs then on zigbee receiver it receives the encrypted keys which are transmitted by zigbee transmitter, the same key is generated. the overall content this experiment is generate the encrypted key securely.

IV.RESULT AND DISCUSSION

a) RTL (register transfer logic) of LFSR

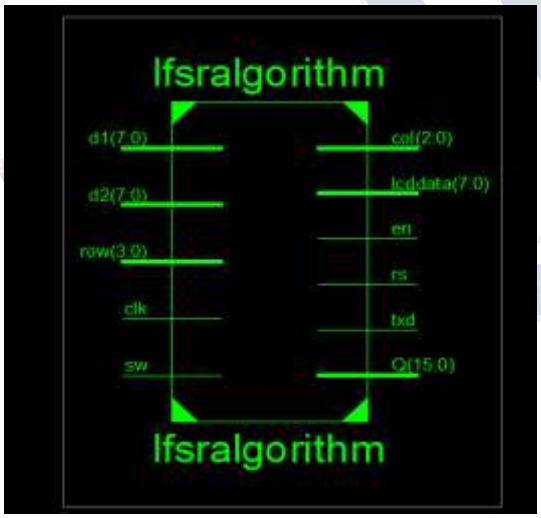

Fig 6: RTL schematic of LFSR

RTL stands for register-transfer level and its abstraction is used in hardware description language like Virology and VHDL to create high-level representation of circuit, from which lower-level representation & ultimately actual wiring can be derived. Design at the RTL level is typically in modern digital design. Whenever check syntax completed successfully click the Xilinx synthesis technology in RTL schematic it shows the main figure of converter module. The below figure shows register transfer level schematic.

b).Technological schematic:

The fallowing shows the technological schematic for linear feedback shift register

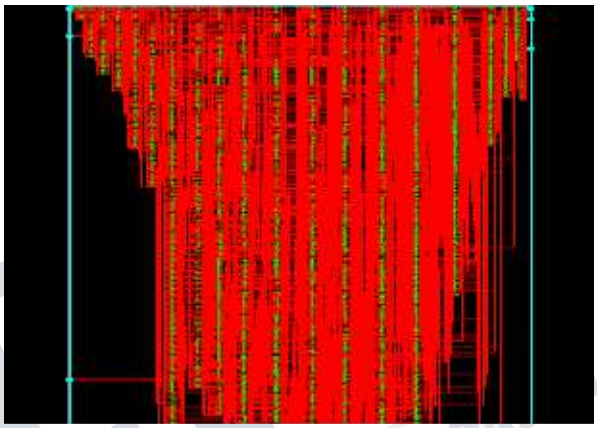

Fig 7: Technological schematic

The technology schematic is shown in below figure 6.2.it consisting of inner sub modules of register-transfer level blocks. It gives each sub block schematic of main register level main module. In this number of gates used as logic levels, number of LUTs used all things shown in this technology of sigma-delta ADC and ASIC file also generated d)Area utilization report: the fallowing shows the area utilization report fo r the linear feedback shift register.

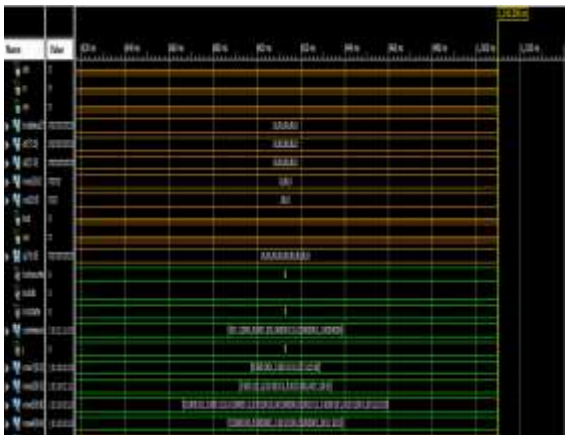

Fig 8: area utilization report or LFSR

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V.CONCLUSION

Dynamic power reduction of LFSR with clock gating technology used to overcome the problems of BIST architecture. This system can also reduce the power consumption. By using this project to provide secure data. It has low cost and less time consumption. In order to evaluate the power reduction obtained by applying clock gating in LFSR, we have evaluated the power consumption in 16 bit Traditional LFSR and power consumption in 16 bit LFSR with clock gating for same input vector and same clock cycles. VHDL code of traditional 16 bit LFSR was simulated in Xilinx 13.2 ISE Navigator and then VHDL code of 16 bit LFSR with gated clock was simulated and synthesized and the Power was obtained using Xilinx Power Analyzer. The results obtained from the Xilinx 13.2 implementation with the device in which, we have generated NCD, PCF, SAIF files after the post simulation. Power is used to calculate the with the simulation file. Reduced power Linear Feedback Shift Register with gated clock is here designed. There is **52% reduction** in Dynamic power, **1.5% reduction** in total power achieved. In contrast to the above results, that may be due to Power Optimization of Linear Feedback Shift Register Using Clock Gating 115 power consumed in initial transitions and that is in order of mili-watts, which is too small as compared to power reduction in Dynamic power and total power.

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