ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
Vol 3, Issue 8, August 2016

Design of Sequential Adder by Using Multi Bit Flip-flop for Power Reduction Technique

[1] G. Sravani
Siddharth Institute of Engineering & Technology College
Puttur, Chittoor Dist, A.P, India

Abstract: **-- In VLSI design the power consumption is increased for more transition memory elements. Flip-flop (FF) are the basic sequential components used for memory applications. An adder and multiplier are designed using Multi-Bit Flip-Flop (MBFF). In the proposed work one of the promising ways to improve performance of FF is merging of clock pulse. Operating memory arrays with less clock cycle will reduce the power taken by the FF which leads to total power reduction and maximum internal delay can also be reduced. Besides, reducing number of FF in the circuit design the total wire length reduces the complexity of MBFF. For dynamic storage the required number of FF selected by transformation check method. Transformation check method can be effectively enabled by dynamic combinational block with check task in the proposed work**

Key Words**---- Power reduction, MBFF, Merging, Synthesis for low power, Wire length, Transformation check method.**

I. INTRODUCTION

The power plays a major role in any design one may need to concentrate on power reduction techniques. To reduce the power consumption, many low-power design techniques have been introduced, such as clock gating, power gating creating multi-supply-voltage designs, dynamic voltage/frequency scaling, and minimizing clock network. Among these techniques, minimizing and merging the clock network is very important in reducing power consumption of a SoC (System on Chip). By reducing the power in circuit design it automatically reduces the complexity and wire length. Thus, different techniques have been proposed to reduce the power consumption in design.

The power had been increased for different stages are static and dynamic power. In dynamic power, change in input signal at different logic level will cause switching and short-circuit power in the design. In static power, it does not have any effect of level change in input and output. The Multi-bit Flip-flop (MBFF) is an effective power reduction methodology. It is used to reduce the number of Flip Flop in storage phase. Sending many bits of data with single FF using single clock pulse is called MBFF. The concept of MBFF is introduced in adder application which is used to reduce the number of FFs which are not enabled in the circuit design. MBFFs have advantage over SBFF as smaller design area, controllable clock, less delay on clock network and efficient utilization of routing resources.

The working of multi-bit flip flop is same as single-bit flip flop, whenever the clock gets active state flip flop latches all input to output. For inactive state the flip flop holds the data. The basic structure of multi-bit flip flop is given in Fig. 1, it shows that instead of using single bit FF we can replace into multi bit FF as 2-bit FF, 4-bit FF and 8-bit FF are developed as a separate task. When will the required bit of storage FF is needed the particular task is being used to reduce power in the post-placement stage. In this work a graph based technique is used in order to reduce the clock power. The flip-flop is represented for each node in the graph. The flip-flop corresponding to the nodes in an m-clique can be replaced by a m-bit flip flop. The algorithm is used to find m-cliques in a graph are branch-and-bound and backtracking algorithm. Another algorithm is also used to find the maximum independent group of called in active region and others will be in-active (sleep mode) region.

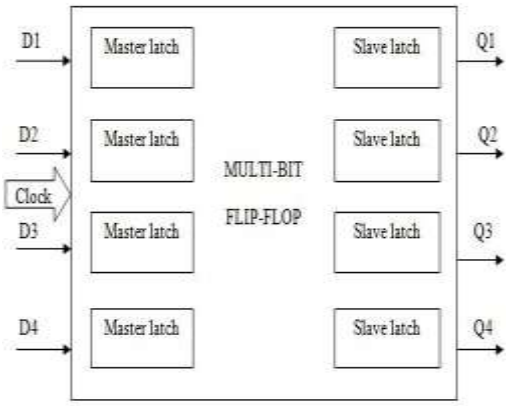


Fig. 1 Block diagram of MBFF

ISSN (Online) 2394-6849
International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
Vol 3, Issue 8, August 2016

In the proposed work it follows that it is used to store the number of bits that are enabling in particular flip-flop using single clock and others are in sleep mode. It doesn't consume power for other flip-flop which is not enabled during the storage phase. The multi smaller FF is replaced by larger MBFF using the less clock source; more over device variations in the corresponding circuit can be effectively reduced. The FF can be merged with the help of combinational table which is dynamically enabled based on the number of bit storage requirement with power consideration. The FF about to be merged can be used for memory arrays. By reducing the number of FFs, the clock sinks area and clock dynamic power have been effectively reduced.

II. RELATED WORK

Ya-Ting Shyu et al had used the many single bit flip-flop are replaced by multi bit flip-flop. Due to this power is increased and complexity in design. The methodology cliques is greedy heuristic algorithm. In this work there is a possibility of finding impossible combination of flip flop in a library. Due to this it may lead to the wastage of time and more number of FFs is used in every node.

III. PROPOSED WORK

In the previous method the amount of time is wasted by finding the impossible combination of FF and also many single bit FF is used. This may increase the complexity. In order to reduce the power MBFF concept is used. In the Fig. 2, it describes that have to identify a legal placement region for each FF. In first stage, the feasible placement regions of a FF associated with different pins are found based on the timing constraints defined on the pins. Then, the legal placement region of the FF can be obtained by overlapped area of these regions.

However, because these regions are in the diamond shape, it is not easy to identify the overlapped area. Therefore, the overlapped area can be identified more easily if it can transform the coordinate system of cells to get rectangular regions. In the second stage, it would like to build a combination table, which defines all possible combinations of FF in order to get a new multi-bit FFs provided by the library.

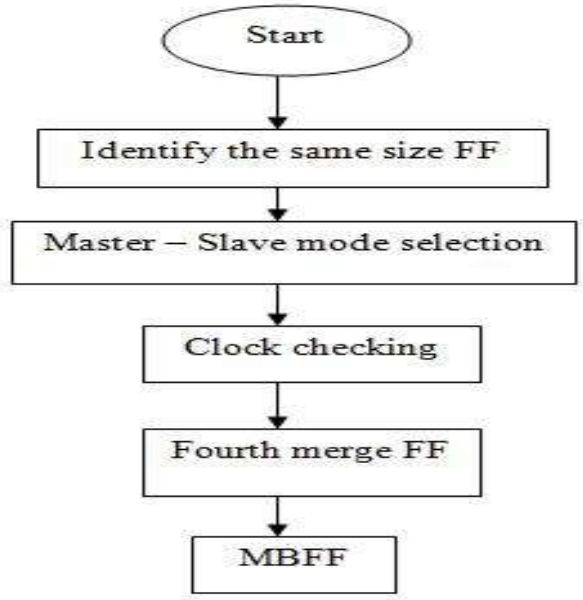


Fig. 2 Flow-chart of merging flip-flop

The flip-flops can be merged with the help of the table. After the legal placement regions of flip-flops are found and the combination table is built, we can use them to merge flip-flops. To speed up our program, we will divide a chip into several bins and merge flip-flops in a local bin.

However, the flip-flops in different bins may be mergeable. Thus, we have to combine several bins into a larger bin and repeat this step until no flip-flop can be merged anymore. In this section, we would detail each stage of our method. In the first subsection, we show a simple formula to transform the original coordination system into a new one so that a legal placement region for each flip-flop can be identified more easily. The second subsection presents the flow of building the combination table. Finally, the replacements of flip-flops will be described in the last subsection.

A. Transformation of placement space

The equations used to transform coordinate system are shown in (1) and (2). Suppose the location of a point in the original coordinate system is denoted by (x, y). After coordinate transformation, the new coordinate is denoted by (x'', y''). In the original transformed equations, each value

ISSN (Online) 2394-6849
International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
Vol 3, Issue 8, August 2016

needs to be divided by the square root of 2, which would induce a longer computation time. Since we only need to know the relative locations of flip-flops, such computation are ignored in our method. Thus, we use *x*"and *y*", to denote the coordinates of transformed locations.

$$x'' = \frac{x+y}{\sqrt{2}} \Rightarrow x'' = \sqrt{2}\,x'' = x+y \longrightarrow (1)$$

$$y'' = \frac{-x+y}{\sqrt{2}} \Rightarrow y'' = \sqrt{2}\,y'' = -x+y \longrightarrow (2)$$

B. Combination table

Several flip-flops can be replaced by multi-bit flip-flop. In this proposed approach, the combination table is build, which is used to get feasible flip-flops before replacement. This makes to use for identifying the particular flip-flop which is enabled in active region and cannot be overlapped. Using this combination table, the flip-flop can be gradually replaced and this makes reduces the complexity of the design. Since only one combination of flip-flop need to be considered in each time, the clock signal can be effectively reduced.

C. Application Developed

The 1-bit, 2-bit, 4-bit and 8-bit FFs are developed as separate task as shown in Fig. 3. The two inputs are „a" is represented as input1 and „b" is represented as input2.

These two inputs are added and stored in the FF updation. After that it checks the bits that are available in the region. The selected FFs are accessed when it is enabled and output is displayed. This makes reduces the power and delay in the design. The low power impacts in the cost, size, weight, performance and reliability.

The multiplier application can also be done in this proposed work. Instead of adding the bits, multiplying can be done and it is stored in the particular enabled flip-flop. For example, assume that a library only supports two kinds of flip-flops whose bit widths are 1 and 4 means the particular flip-flop is selected and it is enabled in the region and will be in sleep mode (in-active region).

The D-FF is used in this proposed work. It provides synchronous data transfer and used for storage purpose. However, unlike latch elements, a FF only copies the data from the input pin to the output once per clock period and does not allow multiple logic values to be passed in a clock cycle. Data is transferred at either the rising or the falling clock edge, depending on the flip-flop configuration. Unlike the latch, a FF is not level-sensitive, but rather edge-triggered. In other words, data gets stored into a FF only at the active edge of the clock. The 16 bit FF can also be developed as shown in Fig. 4, it reduces the power and memory devices compared to single bit flip flop. Generally, the adder libraries consists AND, XOR and OR as majority gates. The register banks are used to store the bit when it is enabled.

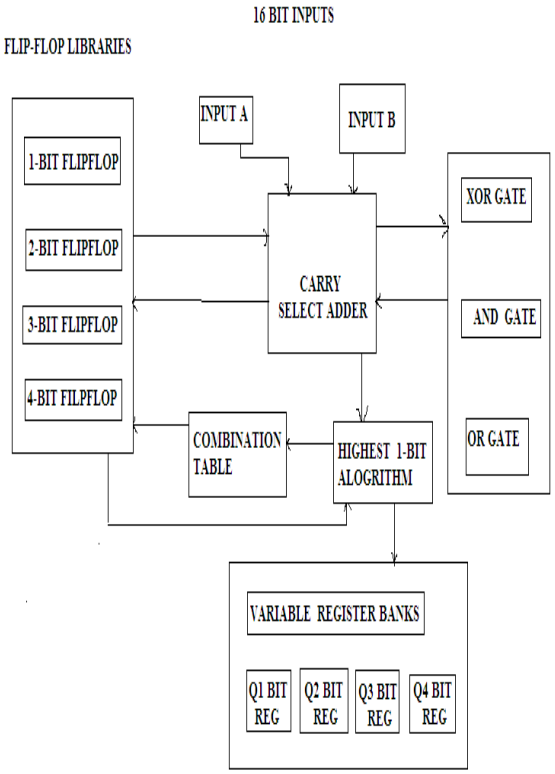


Fig. 3 Block diagram for MBFF using adder application

This section shows our experimental results. We implemented our algorithm in Verilog HDL language, and is carried out using Xilinx ISE Design suite. Our experiment can be divided into two parts. In the first part, we compare our method with Chang et al. [4] and the results are shown in the first subsection. However, some conditions cannot be verified by their test cases.

ISSN (Online) 2394-6849
International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
Vol 3, Issue 8, August 2016

IV. SIMULATION OUTPUT

TABLE I
Comparison results on Static and Dynamic power for MBFFs

Flip-Flop	Static power dissipation	Dynamic power dissipation
1-bit	2.498ns	0.825ns
2-bit	2.498ns	1.520ns
4-bit	2.498ns	1.527ns
8-bit	2.498ns	1.542ns

TABLE II
Comparison results on total power analysis for MBFFs

Flip-Flop	Total power analysis
1-bit	324.95mW
2-bit	328.17mW
4-bit	328.18mW
8-bit	328.19mW

The design is done by using ModelSim, it is easy to use and supports behavioral, register transfer level and gate-level modeling. The Quartus is mainly used to analysis the difference of MBFF that are produced in the region. It is easy to analysis the power consumption for various MBFF

V. EXPERIMENTAL RESULTS

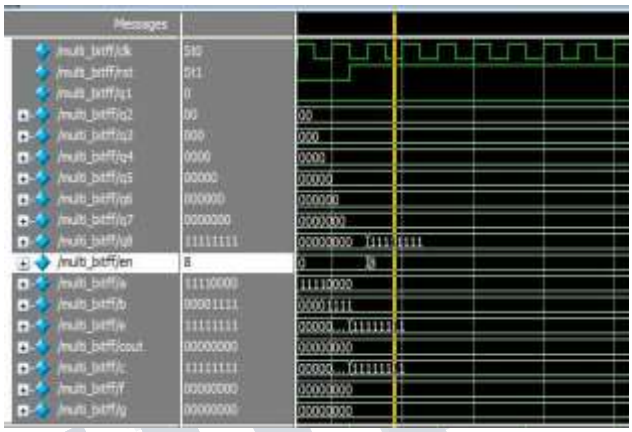


Fig.4 Enabled 1 bit flip flop

In Fig. 4, it explains that initially reset to be „0" and run it, this makes already stored values will be zero. After that change reset as „1" and add any two 8-bits input values a and b then run it. By adding two inputs, it gets output(e) as single bit. So, an single bit FF is enabled and other FFs is in sleep mode.

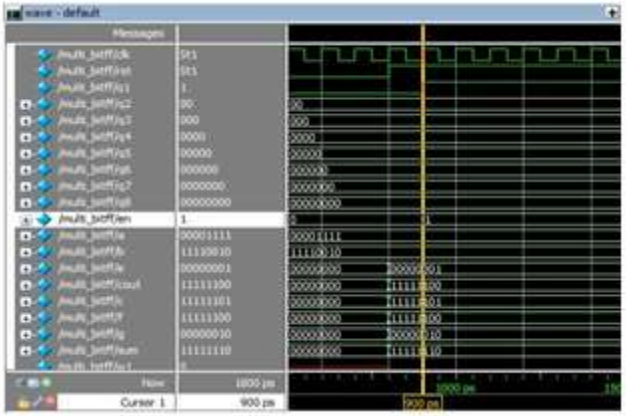
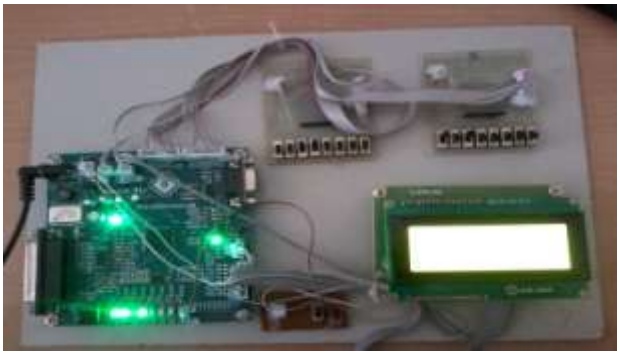


Fig.5 enabled 8 bit flip flop

ISSN (Online) 2394-6849
International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
Vol 3, Issue 8, August 2016



Hardware kit

Output

V. CONCLUSION

The MBFF is used for power reduction in digital integrated circuit design. The MBFF are mainly used to store large data bits. The above MBFF concept has implemented in an adder application which deals with the number of bits that are enabled in the design. Depends on the number of output bits, the required particular enabled FF is stored and remaining will be in sleep mode. So, the transition between the successive outputs bits are less compared to the actual one. The power consumption has been very much reduced. It shows that it is used to reduce the switching activity in the design. The merging FF to be done with the help of combination table. In the proposed work used D-FF this makes low power when compared to other FF and the output will be easy to processed. Finding that number the particular bits of FF storage is getting enabled. It reduces the power consumption and wire length for the MBFF. It can be applicable for counters and shift register

REFERENCES

1. R. Khan, Y. Ali Shah, Z. Khan, K. A. Muhammad and A. M. Amjad Ali, "Canny Car Parking Management System on FPGA," IJCSI International Journal of Computer Science Issues, Vol. 10, No. 1, 2013, pp. 171-173.

2. J. R. Millan-Almaraz, I. Torres-Pacheco, C. Duarte-Galvan, R. G. Guevara-Gonzalez, L. Miguel Contreras-Medina, R. de Jesus Romero-Troncoso and J. R. Rivera-Guillen, "FPGA-Based Wireless Smart Sensor for Real-Time Photosynthesis," Computers and Electronics in Agriculture, Vol. 93, 2013, pp. 58-69.

3. S. J. Bellis, K. Delaney, B. O'Flynn, J. Barton, K. M. Razeeb and C. O'Mathuna, "Advancement of Field Programmable Modular Wireless Sensor Network Nodes for Ambient Systems," University College Cork, Cork, 2005.

4. J. Wei, L. Wang, F. Wu, Y. Chen and L. Ju, "Configuration and Implementation of Wireless Sensor Node Based on Open Core," Proceedings of the IEEE Youth Conference on Information, Computing and Telecommunication, Beijing, China, 20-21 September 2009, pp. 102-105

5. Institute of Electrical and Electronics Engineers, Inc., IEEE Std.802.15.4-2003, "Remote Medium Access Control (MAC) and Physical Layer (PHY) Specifications for Low Rate Wireless Personal Area Networks (LRWPANs)," IEEE Press, New York, 2003.

6. P. Baronti, P. Pillai, V. WC. Chook, S. Chessa, A. Gotta and Y. Fun Hu, "Remote Sensor Networks: A Survey on the State of the Art and the 802.15.4 and ZigBee Standards," Computer Communications, Vol. 30, No. 7, 2007, pp. 1655-1695.

7. K. Scott, "Configuration and Performance of IEEE 802.15.4. Agreeable MSE Receivers," Asilomar Conference on Signals, Systems and Computers, Vol. 2, November 2004, pp. 2051-2055.

Project associate:

G.Sravani persuing M.Tech in Siddhartha engineering college, puttur. Completed Btech in kkc institute of engineering puttur in 2009-2013.Completed Intermediate

in Narayana junior college, tirupathi in2007-2009.compledc in Vijayavani residential school, chowdepalle in 2007.

***Project Guide*:**

Mr. D.Muneendra, M.Tech, Assistant Professor in Department of Electronics & Communication Engineering, Siddhartha Institute of Engineering and Technology, Puttur.