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Power Efficient and Minimum Delay Parallel Self Timed Adder

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Abstract: **-- This paper is about a parallel single-rail self-timed adder. It is based on a recursive formula method for performing 4-bit binary addition. we can have the parallel operation for the bits that do not need any carry chain propagation. Hence the design having logarithmic performance over random operand conditions without any special speedup circuitry or carry look-ahead schema. We can have a practical implementation is provided along with a completion detection unit. The implementation is regular and does not have any practical limitations of high fan-out. A high fan-in gate is required and we can avoid for asynchronous logic by connecting the transistors in parallel. Simulations have been performed using an industry standard toolkit h-spice that verifies the practicality and superiority of the proposed approach over existing asynchronous adders.**

Key words **— Synchronous, Asynchronous circuits, CMOS design, binary adders, Ripple carry adder**

I. INTRODUCTION

Binary addition is very important operation that a processor performs. Many adders have been designed for synchronous circuits even though there is a strong interest in (clock less/Asynchronous) circuit. They do not assume any quantization of time. Hence, they hold great potential for logic design as they are free from several problems of clocked (synchronous) circuits. The logic flow in asynchronous circuits is controlled by a request-acknowledgment handshaking protocol to establish a pipeline in the absence of clocks in principle. Explicit handshaking blocks for small elements, such as bit adders, are expensive. So that, it is implicitly and efficiently managed using dual-rail carry propagation in adders. A valid dual-rail carry output also provides acknowledgment from a single-bit adder block. Thus, asynchronous adders are either based on full dual-rail encoding of all signals (more formally using null convention logic that uses symbolically correct logic instead of Boolean logic) or pipelined operation using single-rail data encoding and dual-rail carry representation for acknowledgments. While these constructs add robustness to circuit designs, they also introduce significant overhead to the average case performance benefits of asynchronous adders. Therefore, a more efficient alternative approach is worthy of consideration that can address these problems. This paper brief presents an asynchronous parallel self-timed adder (PASTA) using the algorithm originally. The design of PASTA is regular and uses half-adders (HAs) along with multiplexers requiring minimal interconnections. Thus, it is suitable for VLSI implementation. The design works in a parallel manner for independent carry chain blocks. The implementation in this brief is unique as it employs feedback through XOR logic gates to constitute a single-rail cyclic asynchronous sequential adder Cyclic circuit scan be more resource efficient than their acyclic counterparts.

Here there is another technique wave pipelining (or maximal rate pipelining) is a technique that can apply pipelined inputs before the outputs are stabilized. The proposed circuit manages automatic single-rail pipelining of the carry inputs separated by propagation and inertial delays of the gates in the circuit path. Thus, it is effectively a single rail wave-pipelined approach and quite different from conventional pipelined adders using dual-rail encoding to implicitly represent the pipelining of carry signals.

II.CONVENTIONAL RIPPLE CARRY ADDER

The structure of an 4-bit Conventional-RCA, which is based on blocks of the FA (Full Adder blocks), is shown in Fig. 1.

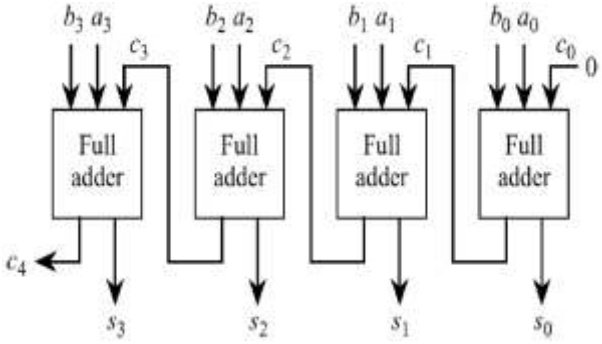

Fig.1. Conventional structure of the RCA

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Here there is carry skip logic in addition to the chain of FAs in each stage. For an RCA that contains N cascaded FAs, the worst case propagation delay of the summation of two N-bit numbers, A and B, belongs to the case where all the FAs are in the propagation mode. It means that the worst case delay belongs to the case where

Pi=Ai ⊕Bi=1 for i=1, 2……, N

Where Pi is the propagation signal related to Ai and Bi. This shows that the delay of the RCA is linearly related to N. In the case, where a group of cascaded FAs are in the propagate mode, the carry output of the chain is equal to the carry input.

III. DELAY OF THE RIPPLE CARRY ADDER

The gate delay can easily be calculated by inspection of the full adder circuit. Each full adder requires three levels of logic. In a 32-bit ripple-carry adder, there are 32 full adders, so the critical path (worst case) delay is 3 (from input to carry in first adder) + 31 * 2 (for carry propagation in later adders) = 65 gate delays. The general equation for the worst-case delay for a *n*-bit carry-ripple adder is

$$T_{CRA}(n) = T_{HA} + (n-1)T_C + T_S = T_{FA} + (n-1).T_C$$
$$= 6D + (n-1).2D$$
$$= (n+2).2D$$

- The delay from bit position 0 to the carry-out is a little different:

$T_{CRA[0:C_{out}]} = T_{HA} + n.T_C$=3D+n.2D

- The carry-in must travel through *n* carry-generator blocks to have an effect on the carry-out

$T_{CRA[0:C_n]}(n) = n.T_C$=n.2D

The overall delay of the Full adder is given as 16 ns

IV.PROPOSED PASTA STRUCTURE

In this section, the architecture and theory behind PASTA is presented. The Half adder first performs half additions for each bit by accepting two input operands. Similarly, it iterates using earlier generated carry and sums to perform half-additions repeatedly until all carry bits are consumed and settled at zero level.

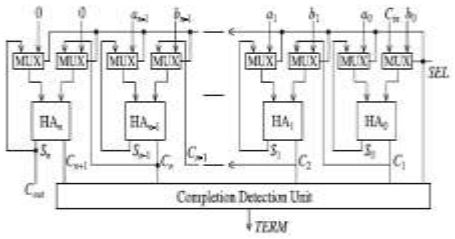

Fig. 2. Proposed PASTA structure

State diagrams

Two state diagrams are drawn for the initial phase and the iterative phase of the proposed architecture. Each state is represented by (*Ci*+1 *Si*) pair where *Ci*+1, *Si* represents carry out and sum values, respectively, from the *i*th bit adder block. During the initial phase, the circuit merely works as a combinational HA operating in fundamental mode. It is apparent that due to the use of HAs instead of FAs, state cannot appear.

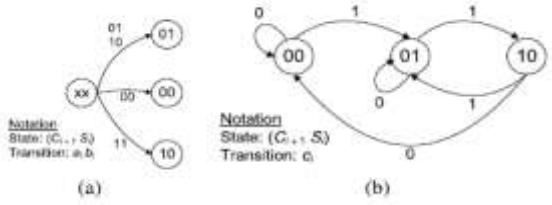

Fig3.State diagram of PASTA

During the iterative phase (SEL = 1), the feedback path through multiplexer block is activated. The carry transition inputs (*Ci)* are allowed as many times as needed to complete the recursion. From the definition of fundamental mode circuits, the present design cannot be considered as a fundamental mode circuit as the input–outputs will go through several transitions before producing the final output. It is not a Muller circuit working outside the fundamental mode either as internally; several transitions will take place, as shown in the state diagram. This is analogous to cyclic sequential circuits where gate delays are utilized to separate individual states during the iterative phase (SEL = 1), the feedback path through multiplexer block is activated. The carry transitions (*Ci*) are allowed as many times as needed to complete the recursion. From the definition of fundamental mode circuits, the present design cannot be considered as a

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Recursive Formula for PASTA

Let $S_i^{\,j}$ *and* $C^{j}{}_{i+1}$ *denote the sum and* carry Respectively, for i^{th} *bit at the* j^{th} *iteration*

$$S_i = A \oplus B$$

$$C_{i+1} = A_i \,.\, B_i$$

The j^{th} iteration for the recursive addition is formulated by

$$S_i^{\,j} = S_i^{\,j-1} \oplus C_i^{\,j-1}, \quad 0 \le i < n$$

$$C_{i+1}{}^{j} = S_i^{\,j}\; C_i^{\,j-1}, \quad 0 \le i < n$$

CMOS implementation of PASTA:

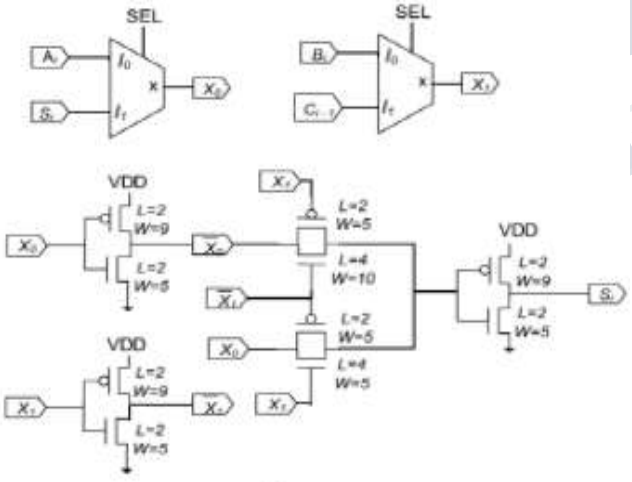

Fig (a) Single bit sum module

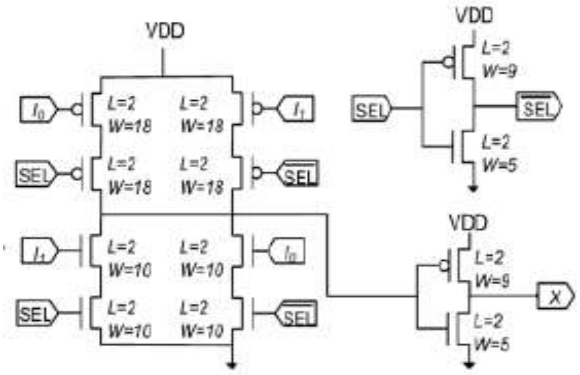

Fig (b) 2x1 mux for 1-bit adder

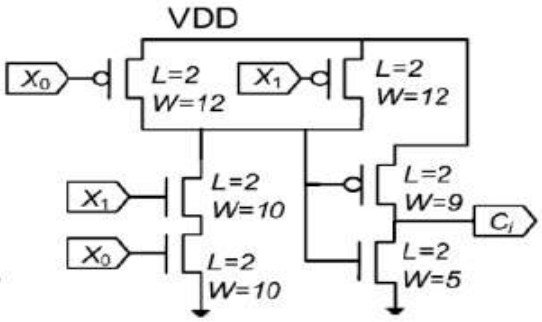

Fig (c) Single bit carry module

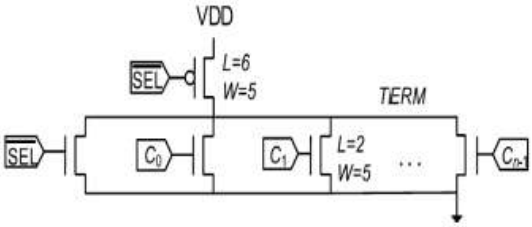

Fig (d) Completion detection unit circuit

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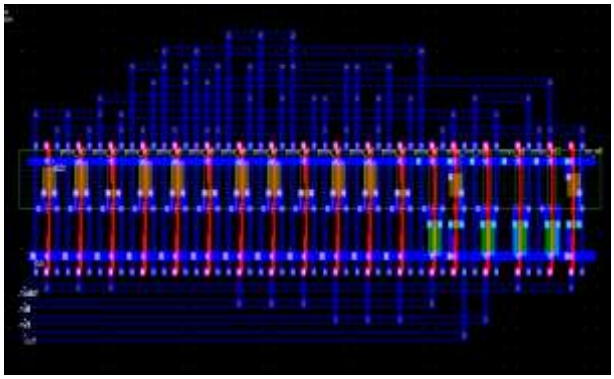


Fig (e) Single bit MUX module

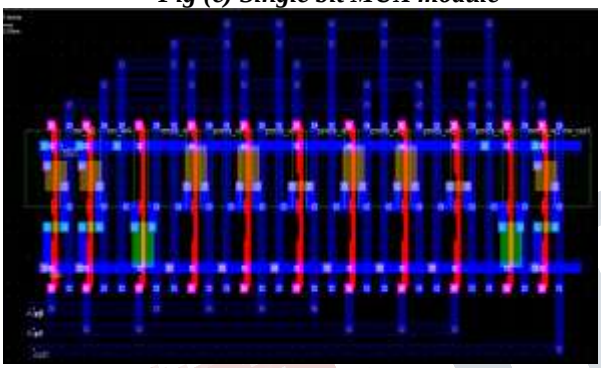


Fig (f) Single bit sum module

V.RESULTS

The RCA and PASTA with the conventional and proposed can be implemented on the h-spice tool

The total delay of Ripple Carry adder 2.8933 ns delay (ns)

Table 1: Delay comparison of different technologies in proposed Parallel Self timed adder

Technology used (for 4-Bit)	Parallel Self timed adder delay(ns)
360nm	0.423ns
180nm	0.210ns
90nm	0.1124ns

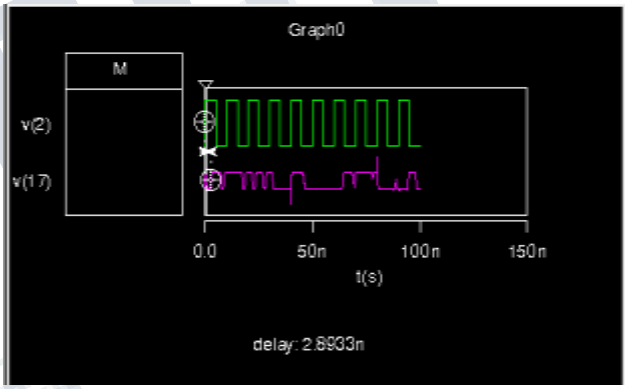
The total adder Power consumption of 4-bit Ripple Carry 3.8754 mw

Table 2: Power consumption comparison of different technologies of proposed Parallel Self timed adder

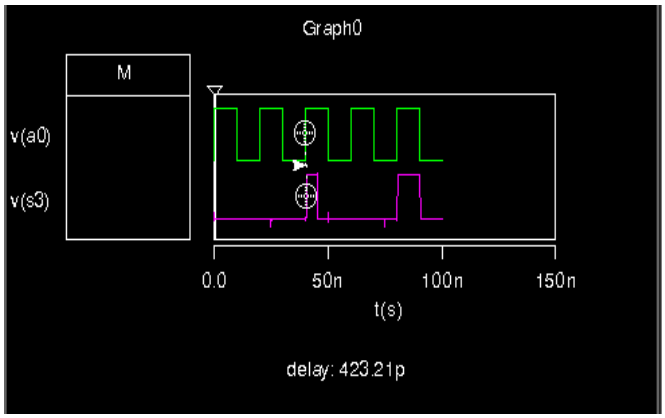
Technlogy used (for 4-bit)	Parallel Self timed adder Power consumption(mw)
360nm	1.9757
180nm	0.3921
90nm	0.349

VI SIMULATION RESULTS

Delay of 360nm RCA



Delay of 360nm pasta



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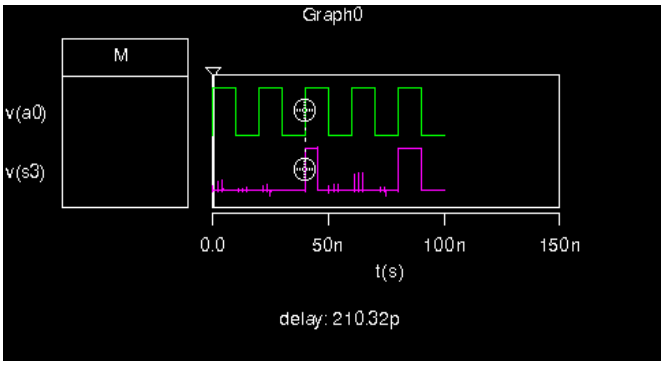
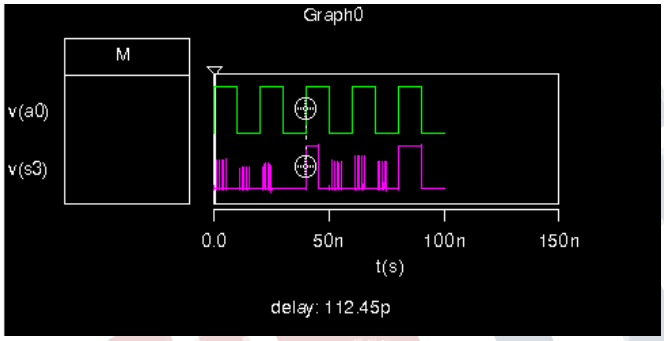
Delay of 180nm PASTA



Delay of 90nm PASTA



VII.CONCLUSION

An efficient adder PASTA was implemented using various techniques in order to get better performance. The circuit works in a parallel manner for independent carry chains. Here for random input values logarithmic average time performance is achieved. For this proposed adder we also obtained practical and efficient completion detection unit. Compare to RCA we could obtain the delay to be reduced by 2.47ns for 4-bit PASTA and Power by 1.89mW which contributes for a greater efficiency. PASTA better performance in delay and power. Simulation results are used to verify the advantages of the proposed approach. The proposed method is implemented using digital HSPICE A-2008 environment

The power consumption of the circuit is also reduced to a large extent and the delay of each technology of PASTA (360nm,180nm and 90nm) is shown in all the simulation results.

Thus the Parallel self-timed adder (PASTA) is having better performance than RCA in low power and delay efficient circuit by changing the technology.

REFERENCES

[1]David. Geer, “Is it time for clockless chips?”, Mar 2005 IEEE.

[2] Steve Furber,Jens Sparso “Principles of asynchronous circuit design”. US Springer 2010.

[3] P. Choudhury, S. Sahoo, and M. Chakraborty, “Implementation of basic arithmetic operations using cellular automaton,” 2008 IEEE,

[4] M. Z. Rahman and L. Kleeman, “A delay matched approach for the design of asynchronous sequential circuits,” Department of Computer Science Syst. Technology University, Malaysia, 2013

[5] M. D. Riedel, “Cyclic combinational circuits,” Ph.D. dissertation, Department of Computer science, California Institute of Technology., USA, May 2004.

[6] Adrianus marinus gerardus Peeters, Single-Rail Handshake Circuits

Bibliographies:

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