ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
Vol 3, Issue 8, August 2016

IR Drop and Electro Migration Reduction Techniques in Deep Sub-Micron technologies

[1] D. Paramesh Kumar, [2] Mr. D. Raja Ramesh
[1] M.Tech [2] M.Tech (Ph.D)
[1][2] Department of ECE, MVGR College of Engineering, Vizianagaram

Abstract: **-- Power is an important parameter in the recent years due to the ramp up of mobile devices, which need to support the device operation for longer times without need for external power source. So the voltage is scaling to help with this along with scaling of transistor. It helps in increasing the cell density in a given area, but needs higher current density and more no. of interconnects. To support this, the wire dimensions are also minimized, which causes more resistance due to which IR drop occurs. If enough voltage is not available at the cells, it affects timing; if available voltage is even lesser, it will lead to functional failure. If it happens on clock network, it causes skew. Increase in current density and decrease in dimensions of wire cause Electro migration which occurs due to the momentum transfer from electrons to the atoms in the wire. If more current is flowing and if it exceeds the current density limit of the interconnect, it leads to Electro migration. Due to this, the wire dimensions will decrease even more and cause more resistance, heat and current density. The project IR Drop and Electro migration Reduction Techniques in Deep Sub-Micron Technologies, discusses the techniques to find out the whether it is resistance or current which is causing the IR Drop in a region, and shifting the timing window of the instances in high IR drop region to avoid simultaneous switching. It also implements the techniques to find out the minimum width which is necessary in the present metal layer as well as in higher metal layer in order to avoid the Electro migration.**

Index Terms: **- ENCOUNTER POWER SYSTEM (EPS), TIMING WINDOW FILE (TWF)**

I. INTRODUCTION

In the deep sub-micron CMOS technologies, the problem of the voltage drop on the integrated circuit supply rails has become significant. The supply voltage has dropped from 5v with 0.6um technology to 0.8v at 14nm technology. But the power consumption has remained about the same or higher than it used to be, because integrated circuits have more gates and run at higher frequencies. This means, for the same power, the currents flowing in the power supply are proportionately higher. At the same time, the voltage drop which can be tolerated along the supply rails has also decreased. This is typically expressed as a percentage of the power supply, often 5%. This means, a 5V power supply could tolerate a 250mV drop, but 0.8V power supply could only 40mV.

This drop is V = IR, where R is the supply rail resistance, which must then scale proportionately with the supply voltage. This means that for the same supply current, the power supply resistance going from 5V to 0.8V needs to be (0.8/5) times the resistance at 5V technology.As the size of standard cells is decreasing, it allows more cells that can be placed in the same area. So, the density of cells is increasing and so the required current. That means, the current required is either same or more than before. But as the dimensions of interconnect is also decreasing, the maximum current density that can be supported by the interconnect is reducing. It is causing the Electro migration, which is the gradual displacement of the ions in a semiconductor material in the direction of electron flow due to momentum transfer.

A. Effect of technology shrinking

With scaling in technology to lower node, Cell density increases , Current density increases, Supply voltage decreases, Interconnect widths decreases .

B. IR Drop

IR drop is the reduction in supply voltage that occurs on power supply networks in Integrated Circuits. This reduction in voltage is due to the combination of increasing current density and narrower metal line widths. This causes the voltage available at the standard cells to be lower than what is desired. Due to this, Delays may increase when drop is more & within noise margin .Sometimes, they may not switch at all when drop exceeds noise margins .The following picture shows the resistances between the external power supply and a cell at the center of a chip. IR drop is the sum of the voltage drop across R_{VDD} and R_{VSS}.

ISSN (Online) 2394-6849
International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
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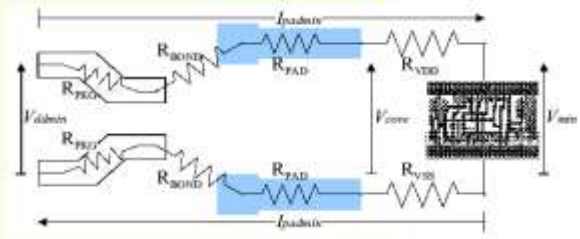

Fig. 1. IR drop illustration

C. IR Drop Concern due to scaling

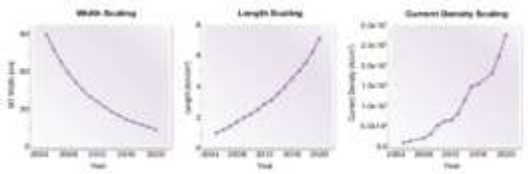

Fig. 2. IR Drop due to scaling

With technology improvement, Interconnect widths are decreasing, total interconnect length is increasing; current is increasing due to increase in no. of cells per unit area.

D. IR Drop Effects

IR drop on power rails can significantly affect cell delays & net delays. IR drop varies with the varying of switching activity of the cells in the design. Both clock and data paths get affected. Sufficient voltage is not available at the standard cells, Timing failure if the drop is more & with in the noise margin Functionality failure if the drop exceeds the noise margins

E. Electro migration

It is the gradual displacement of metal atoms in a semiconductor in the direction of electron flow. It occurs due to the momentum transfer from the electrons moving in a wire. As the structure size in Integrated circuits decreases, the significance of this effect increases.

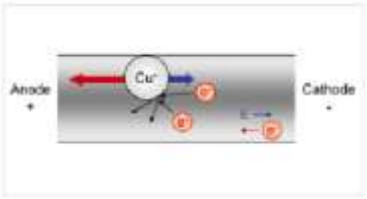

Fig. 3. Illustration of Electro migration

The effect is important in applications where high current densities are used such as in ICs. Cross-sectional areas of wires continue to decrease but not current densities. It creates "Voids" where ions got removed and"Hillocks"where ions got deposited. Due to this effect, the life time of the device will decrease.

F. Failure mechanisms of Electro migration

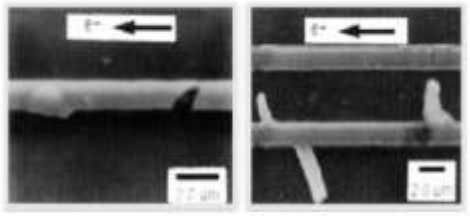

Fig. 4. Void (open circuit) and Hillock (short circuit)

In the left hand side figure, the wire material is washed away due to EM, and in the right hand side figure, the wire material is accumulated.

G. Effects of Electro migration

Decreases the reliability of chips, heating of wire material due to resistance which in turn cause resistance loop, first symptoms are intermittent glitches, causes the eventual loss of connections which leads to failure of a circuit.

Void: open circuit (signal loss)

Hillock: short circuit (faulty operation)

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International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
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H. How it effect the timing?

IR drop is Signal Integrity(SI) effect caused by wire resistance and current drawn off from Power (Vdd) and Ground (Vss) grids.

According to Ohms law,

$$V = IR$$

If wire resistance is too high or the current passing through the metal layers is larger than the predicted, an unacceptable voltage drop may occur. Due to this unacceptable voltage drop, the power supply voltage decreases. That means, the required power across the design is not reaching to the cells. This results in increased noise susceptibility and poor performance.

The design may have different types of gates with different voltage levels. As the voltage at gates decreased due to unacceptable voltage drop in the supply voltage, the gate delays are increased non-linearly. This may lead to setup time and hold time violations depending on which path these gates are residing in the design. As technology node shrinking, there is decrease in the geometries of the metal layers and the resistance of this wires increased which lead to decrease in power supply voltage. During Clock Tree Synthesis, the buffers and inverters are added along the clock path to balance the skew. The voltage drop on the buffers and inverters of clock path will cause the delay in arrival of clock signal, resulting hold violation.

II. VECTOR-BASED AVERAGE POWER CALCULATION

The vector-driven approach uses the VCD output of a logic simulator to obtain the number of transitions for each net. PM requires gate-level VCD with good functional coverage for accurate power calculation results.

We can use VCD information to calculate accurate power consumption figures, if the following conditions apply:

1. Gate-level simulation is possible at the full-chip level.
2. Gate-level simulation provides sufficient functional coverage for the design. The vectors include those that cause the highest power consumption.

A. Dynamic Power Analysis overview

Encounter Power System requires the use of dynamic power-consumption data for each instance and is output by the power calculator when you perform dynamic power-grid analysis. The current is required to calculate the IR drop. Dynamic, or transient, analysis at the gate level is a way to detect power integrity problems, determine the optimal number and placement of decoupling capacitors to minimize power leakage, provide insight into the effect of simultaneously switching outputs, and assess the impact of resistance, capacitance, and inductance due to packaging, bond wire, and C4 bumps on transient IR drop.

Dynamic power-consumption calculation is a method of analyzing a circuit to obtain operating currents and voltages. It is time-based, analyzing the circuit netlist over a specified period, such as a clock cycle.

The power calculator uses two methods to calculate the dynamic power consumption:

1. The vector-driven approach uses the full VCD output of a logic simulator to identify the instances that are switching and when they switch. This method is described in detail in Vector-Driven methodology.
2. The vector-less approach uses timing arrival window information from a STA tool to determine when instances switch. A timing arrival window describes when a signal can change within a clock cycle. An additional algorithm then determines the instances that switch. This method is called the vector-less, timing-windows-based, or pseudo-dynamic approach. This method is described in detail in Vector-less, Timing-Windows-Based methodology.

B. Vector-Driven methodology

As noted earlier, the VCD file is the output from a gate-level simulation of many vectors and contains all the net switching activity information for the design. The VCD simulation approach to dynamic power-consumption calculation uses the same VCD file as that used for static

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International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
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power- consumption calculation, but unlike the static VCD approach, it uses the information in the VCD file on what instances switch and when they switch. Using output load and slew, it creates current profile for the instance based on power arcs defined in .lib for the cell. The calculated dynamic currents are saved for all power nets associated with the instance. These current waveforms can be viewed using SimVision waveform viewer interface.

Generally, the VCD file can be very large in terms of total simulation duration. While static power calculation can process such full VCD file and derive average activity to calculate static power, running dynamic simulation on full VCD is unrealistic due to performance and resource limitation. Hence it is recommended that you identify the power hungry cycles or cycles with high switching activity up-front to perform dynamic power calculation.

It is recommended that VCD window (start and stop time) for dynamic power calculation does not exceed more than five cycles of dominant clock in the design.

The vector-driven approach for dynamic power-consumption calculation offers several advantages:

1. The data that it yields is exact for the given vectors. For a given vector, you know exactly what is switching and when.
2. We can use it to validate the vector-less, timing-windows-based simulation.
3. It is a well-understood methodology, if power-hungry cycles are known and is therefore easy to develop.

C. Vector-less, Timing-Windows-Based methodology

In the vectorless, timing-windows-based approach to dynamic power-consumption calculation, the power calculator generates a virtual worst-case power vector using design information and activity and switching constraints that you supply. The challenge posed by vectorless methods of dynamic power-consumption calculation is to obtain information on what instances to consider for switching and when to schedule them to produce a worst-case vector without using actual simulation. The power calculator's vectorless approach creates a realistic, but not too pessimistic, dynamic profile for the design so that you can analyze worst-case dynamic IRdrop in the design.

To determine the time of switching, the power calculator uses the timing database or timing windows file (TWF) generated by a static timing analysis program like Encounter Timing System. In addition to clock domains, slews, slack and constant, it also includes arrival times for each instance pin. The window of arrival times is not an exact time of transition but it is a union of several arrival times combined into one clock cycle, possibly through different combinational paths, at different clock periods. The power calculator uses Monte Carlo algorithm to schedule(instance's exact switching time) inside this timing window.

To determine how often an instance is switching, the power calculator uses activity propagation along with any user specified activity. The known activity data on primary inputs, sequential output, and clock gates further helps generation of accurate and realistic worst-case dynamic profile.

Once the activity and time of switching is determined, the program uses output load and slew to create a weighted average current profile for the instance based on power arcs defined in .lib for the cell. The calculated dynamic currents are saved for all power nets associated with the instance. These current waveforms can be viewed using SimVision waveform viewer interface. The calculated current waveforms are then fed to dynamic rail analysis engine to perform dynamic IRdrop analysis.

Using a TWF file is less accurate than using a VCD file because it contains ranges of information rather than precise arrival times, however, constructing a worst-case dynamic profile offers great improvement in run time over a vector-based solution which is not scalable for full-chip. Using a TWF file is also faster than using a VCD file, because it requires less preparation. With a VCD file, you must understand how to prepare stimulus to prepare worst case vector that could produce worst-case power and IR drop.

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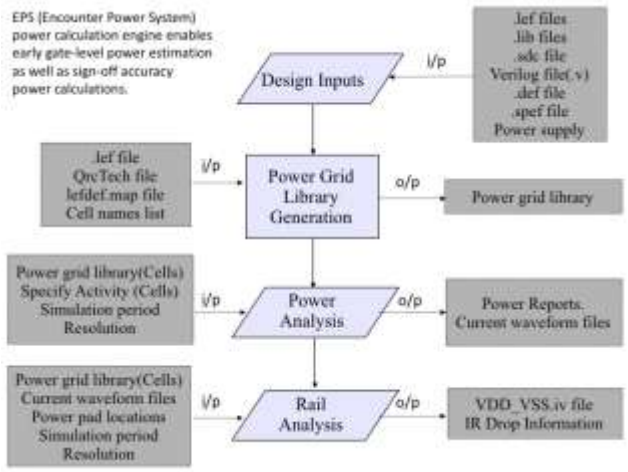

Fig. 6. EPS Flow Diagram

III. TECHNIQUES IMPLEMENTED FOR REDUCING ELECTRO MIGRATION VIOLATION

The EM violation report contains Violation ($J_{required}/J_{limit}$), Location of the violation, Layer in which the violation is present. The ".ict" file contains Variables for equation of maximum current density (J_{max}), Minimum width, Thickness, Multiplication factor for different temperature values.

A. To fix the EM violation when violation > 1 (Using the same layer)

Steps:

1. From the report, take the net with EM violation > 1.
2. Find the $J_{required}$ for that net using the formula.
3. Increase the width and calculate the J_{limit} this width.
4. Repeat the step 3 till the J_{limit} >= $J_{required}$
5. Write the value in a file
6. Do this for all the nets with violation > 1

Report:

violation	width now	layer	net name
1.000002822	0.120000000	M2	VDD
1.000000871	0.110000000	M1	VDD

Fig. 7. Report for EM fix using same layer when violation > 1

Output:

Fig. 8. Output for EM fix using same layer when violation > 1

B. To fix the EM violation when violation > 1 (Using the higher metal layer)

Shifting to higher metal layer may reduce EM due to increased thickness.

Steps:

1. From the report, take the net with EM violation > 1.
2. Find the $J_{required}$ for that net using the formula.
3. Increase the width and calculate the J_{limit} this width for each layer till J_{limit} >= $J_{required}$
4. Write the values in a file
5. Do this for all the nets with violation > 1

Report:

Fig. 9.Violation Report

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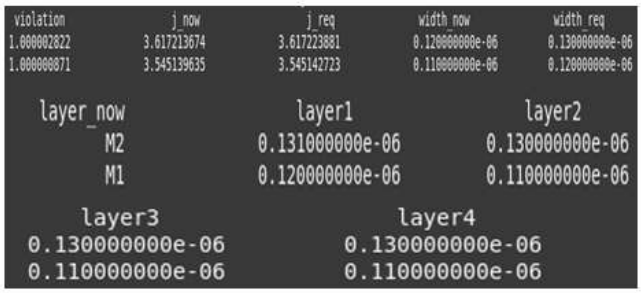
Output:



violation	j_now	j_req	width_now	width_req
1.000002822	3.617213674	3.617223881	0.120000000e-06	0.130000000e-06
1.000000871	3.545139635	3.545142723	0.110000000e-06	0.120000000e-06

layer_now	layer1	layer2
M2	0.131000000e-06	0.130000000e-06
M1	0.120000000e-06	0.110000000e-06

layer3	layer4
0.130000000e-06	0.130000000e-06
0.110000000e-06	0.110000000e-06

Fig. 10. Output for EM fix using higher layer when violation > 1

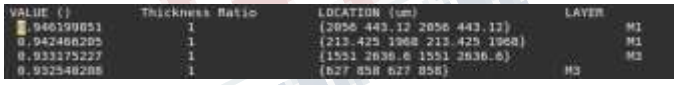
C. To relax the wire width when violation is < 1

If there is timing margin, this technique is useful to give resources to other violating nets.

Steps:

1. From the report, take the net with EM violation < 1.
2. Find the $J_{required}$ for that net using the formula.
3. Decrease the width and recalculate the J_{limit} this width for each layer as long as J_{limit} >= $J_{required}$ is satisfied.
4. Write the values in a file
5. Do this for all the nets with violation < 1

Report:



VALUE ()	Thickness Ratio	LOCATION (um)	LAYER
0.946199851	1	(2056 443.12 2056 443.12)	M1
0.942466205	1	(213.425 1968 213.425 1968)	M1
0.933175227	1	(1551 2630.6 1551 2630.6)	M3
0.932548288	1	(627 858 627 858)	M3

Fig. 11. Report for wire width relaxation when violation < 1

Output:

Fig. 12. Output for wire width relaxation when violation < 1

D. Cells surrounding the EM violation

With the cells in neighboring area, we can know the reason for the large current requirement such as high drive strength buffers.

Steps:

1. From the EM violation report, collect the location of violation.
2. Find out the net name corresponding to that location by comparing the layers with the layer in the report.
3. Collect the instances within 10um distance from the location.

- ❖ Take the location from the report
- ❖ From the lower left corner co-ordinates, subtract 10um
- ❖ To the upper right corner co-ordinates, add 10um
- ❖ If the new co-ordinates are crossing the tile boundaries, assign the corresponding tile co-ordinate to the new co-ordinates.
- ❖ Query the instances in that area.
- ❖ Analyze whether there are any high drive strength cells.

Report:

=violation=	=location=	=layer=	=net_name=	cell names of insts surrounding
0.439189851	{656.84 863 651 863}	M1	VDD	== {dti_hvt_165_7g_buf4 dti_165_7g_eco_fill1 dti_165_7g_eco_fill
0.342496285	{1284.6 1341.8 1285.88 1341.8}	M1	VDD	== {dti_hvt_165_7g_buf4 dti_hvt_165_7g_nor2bp3 dti_165_7g_tapc
0.340175222	{1822.2 889.8 1822.76 889.8}	M1	VDD	== {dti_165_7g_tapc3 dti_165_7g_tapc3 dti_165_7g_eco_fill1 dti_165
0.338248878	{1841.805.4 1841.4 885.4}	M1	VDD	== {dti_165_7g_eco_fill1 dti_165_7g_xnor2bp5 dti_hvt_165_7g_inv
0.33175227	{998.44 1618.6 998.6 1618.6}	M1	VDD	== {dti_165_7g_fillern1 dti_165_7g_fillern2 dti_165_7g_or2x1 dti_16
0.325482881	{592.28 871.4 593.4 871.4}	M1	VDD	== {dti_165_7g_tapc3 dti_165_7g_fillern1 dti_165_7g_fillern2 dti_16

Fig. 13. Report for cells surrounding EM violation

ISSN (Online) 2394-6849
International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
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IV. TECHNIQUES IMPLEMENTED FOR REDUCING IR DROP

A. Current & Resistance for high IR drop instances.

Steps:

1) Take the differential voltage report (VDD_VSS.iv)
2) It contains the voltage available at the standard cell instances in the design.
3) Generate the resistance report for VDD, VSS separately by loading the corresponding state directories.
4) From the VDD_VSS.iv file, for each instance

- ❖ Take the resistance from the resistance report files
- ❖ Add the resistances to get the total resistance
- ❖ Subtract the voltage of the instance from supply voltage to get the drop
- ❖ Divide the voltage drop with total resistance.

Output:

v_drop	restance_total	i_due_to_drop	instance
0.010220000	40.868000000	0.000250073	FE_OFC15_deout
0.010230000	44.268000000	0.000231092	FE_OFC22_vsout

Fig. 15. Resistance and Current for high IR drop instances – conclusion

From the above report, the IR drop is more for the 1st instance due to high current requirement.

B. Cells surrounding the IR drop

If we know the cells surrounding the IR drop region, we can know whether the drop is due to the high current requirement by high drive strength cells or due to the resistance.

- If the cells surrounding the IR drop area are of high drive strength cells, the drop is due to current.
- If the surrounding cells are normal cells, the drop is due to the resistance in the supply rails.

Steps:

1. From the file generated using the script to find the current due to drop, take an instance
2. Find the co-ordinates of the instance
3. Add 10um to the x-coordinates,
4. Add 2 times the row height to the y-coordinates
5. Check whether these new co-ordinates are crossing the tile boundaries.
6. If they are crossing, assign the corresponding tile co-ordinate to the new co-coordinates.
7. Query the instances in that area

Report:

Fig. 16. Report of cells surrounding high IR drop instances

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C. *Shifting Timing Window of High Drop Instances*

Timing Window File:

In vector-less, we use timing-window based approach for dynamic power calculation.The Power Meter (to calculate power) generates power for each instance using

- Design information
- Activity
- Switching constraints
- Later the current waveforms are generated.

To determine the switching time for instances, the power calculator uses the TWF file which was generated by static timing analysis (STA) in encounter.Once the activity and switching times are determined, the EPS uses output load and slew to create the average current profile for the instance.The calculated current waveforms are then supplied to dynamic rail analysis engine for dynamic IR drop analysis.In EPS, the TWF file will be generated automatically by the tool for the analysis.TWF file contains of timing window information (arrival times) for all the instance pins.It contains the information in below format

<pin_name>TW

<is_clock><min_rise><max_rise><min_fall><max_fall><

clk_index>

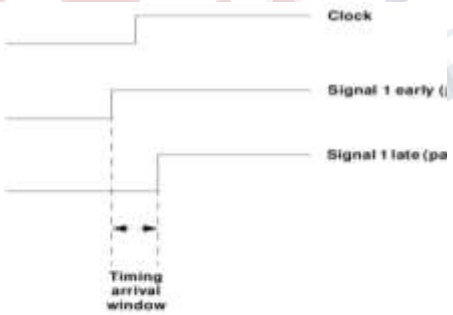

Fig. 17. Timing arrival window for rise signal

V. SIMULTANEOUS SWITCHING INSTANCES

- The .iv file (effective voltages for instances) is generated from the dynamic rail analysis in EPS from this we collect low voltage instances.
- Example : (For collecting simultaneous switching instances)
- For example we have 5 instances with low voltages.

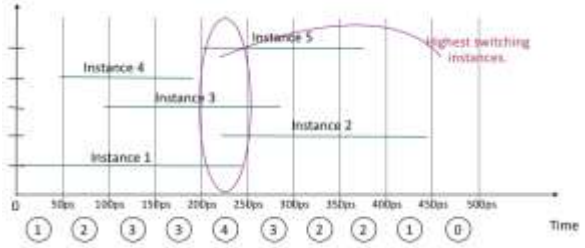

Fig. 18. Simultaneous switching instances

Shifting Timing Windows of instances

If all the instances in a region are switching at a time, they all need the current to charge the capacitance. So, huge amount of current is required and hence, the IR drop will be high. Instead, if the timing window of some of the instances is shifted, they will switch at a different time. So that at a particular time, the current requirement is reduced.In the following experiment, some instances were taken from the high IR drop region and their timing windows are shifted by adding clock buffers at the CLK pins of these instances. It reduced the drop significantly.

IR Drop of Default run:

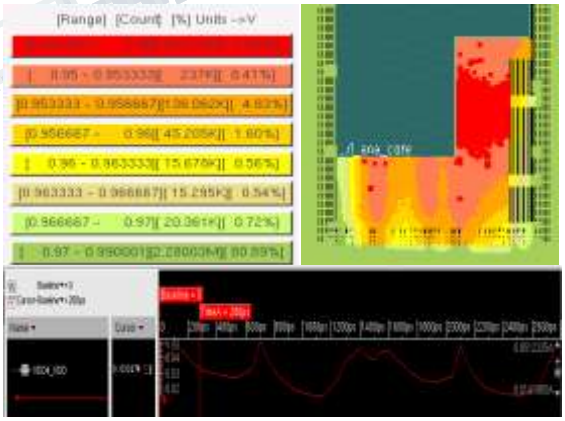

Fig. 19. IR drop of default run

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International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
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IR Drop of run whose timing windows are shifted:

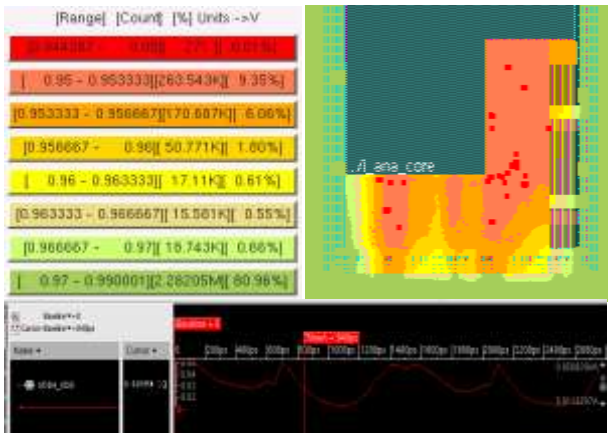

Fig. 20. IR drop of run with shifted timing windows

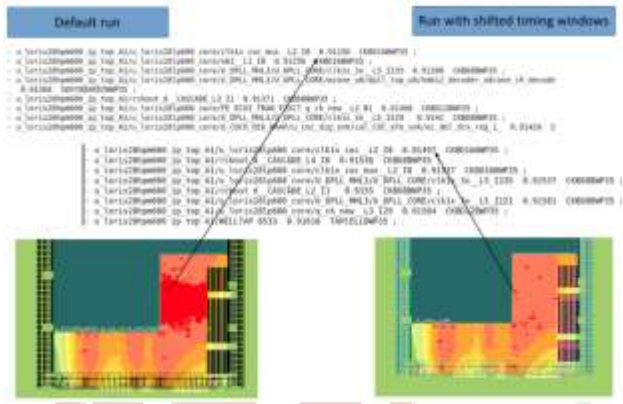

Fig . 21. Comparision of Default and Timing Window shifted Runs

VI. CONCLUSION

In this project, the methods of reducing Electro migration to find the required width based on the current density could be helpful to use the precise value instead of going by trial and error method. When the violation < 1, reducing the width (when there is timing margin) helps in saving resources to other violating nets.The method to reduce the IR drop by shifting the timing windows has significantly reduced the IR drop and Ground bounce. In addition, the cells surrounding the high IR drop region helps in identifying whether the high drop is due to resistance or high current requirement.

Future Scope

In this project, the optimal width needed to avoid Electro migration is calculated after the power and rail analysis are completed, and then the reports are processed. It could be integrated in such a way that the required width values could be generated along with the rail analysis. And the shifting of timing windows could be automated in order to reduce the IR drop.

Acknowledgement

The first author would like to thank M/s VEDA Institute of Information Technology Pvt.Ltd. for providing the opportunity to do internship and to be the part of this work.

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Mr. D. Paramesh Kumar received B.tech degree in Electronics and Communication Engineering from GITAM University. Pursuing M.tech (VLSI) in MVGR college of Engineering

Mr. D. RajaRamesh pursued M.Tech (VLSI) from NIT Suratkal in 2009. Presently working as an Assistant Professor in the Department of ECE in MVGR College of Engineering, Vizianagaram. He had published 7 publications in various International/National Journals/conferences. Areas of interest include VLSI