ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
Vol 4, Issue 11, November 2017

Design of Convolution Using Vedic Multiplier

[1] M.Anusha, [2] P.Srinivasa Rao
[1] CVR College of Engineering
[2] CVR College of Engineering

Abstract:- **In this paper, a novel approach for implementing convolution of two finite length sequences using Vedic multiplier in Cadence tool is proposed. In this, Urdhva Triyagbhyam method is presented. The proposed implementation uses modified hierarchical design approach, which efficiently and accurately speeds up the computation without compromising with area. The 4×4 bit multiplication modules are implemented using small 2×2 bit multiplier. The proposed design is Convolution Using Vedic multiploer has less power and low speed compared other multiplier existed earlier. The design of Convolution is compared different technologies i.e. 45nm,90nm, 180nm and results are compared. When comparing these three technologies, 45nm technology requires less power and delay. The design is implemented using cadence tool in using virtuoso schematic editor, virtuoso symbol editor, and ADEL simulator.**

Index Terms**: Vedic multiplier,Conolution,Cadence tool.**

I. INTRODUCTION

Digital signal processing (DSP) is the technology that is omnipresent in almost every engineering discipline. Faster additions and multiplications are if extreme importance in DSP for convolution, discrete Fourier transform, digital filters, etc. The core computing process is always multiplication routine; therefore, DSP engineers are constantly looking for new algorithms and hardware to implement them. In Ref[1] They proposed to use 4×4 array multiplier as they found it is fastest amongst all other 4×4 multipliers including Booth multiplier. But it is found that Vedic multiplier is more speedy than the proposed multiplier in [1]. Many approaches have been attempted to reduce the convolution processing time using hardware and software algorithms. But they are restricted to specific applications [3]. Ref[4] presented a design for fast convolve for CDMA signals. This is based on avoiding complex operations such as FFT based convolves. They used substitution of the FFT for a Walsh which reduces the operations three times because it uses only real additions but it requires more hardware like counters, and RAM blocks which increases activity factor. Using image processing functions such as convolution filtering, high performance can be achieved by exploiting parallelism and minimizing hardware cost, but different filter widths and this potentially different hardware structures are needed for different applications. It is therefore difficult to make a fixed parallel structure efficient. Implementing the algorithm in parallel hardware will speed up the process but the implementation itself is very complex and requires a huge silicon area.

II. CONVOLUTION

Convolution is said to be the fundamental operation used in most of the signal processing applications Convolution is a mathematical operation performed on two functions. It has applications that include probability, statics, computer vision, language processing, image and signal processing, engineering, and differential equations. So it is necessary to develop a method which improves the speed of convolution operation. Vedic mathematics is an ancient form of mathematics used ny Aryans. It improves the speed of operation, and the algorithms are based on mind calculations. The calculations are based on 16 sutras, of which Urdhva Triyakbhyam sutra for Vedic multiplication. The proposed design uses reversible logic, therefore the power dissipation and delay reduces even more. In this paper, the delay and area existing design compared with proposed design.

DESIGN OF CONVOLUTION VEDIC MULTIPLIER:

The linear convolution is a basic operation in DSP which relates input signal and impulse response to obtain desired output. Convolution is considered to be heart of the digital signal processing. It is the mathematical way of combinig two signals to obtain a third signal, that is a modified form of one of the two signal. Convolution helps to estimate the output of a system with an arbitrary input, with knowing the impulse response of the system. The characteristics of the linear systems are completely specified by the impulse

ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
Vol 4, Issue 11, November 2017

response of the systems, as governed by the mathematics of convolution.

Convolution takes two functions as input and produces a single output. The linear convolution of f(n) and g(n) is y(n)=f(n)*g(n).

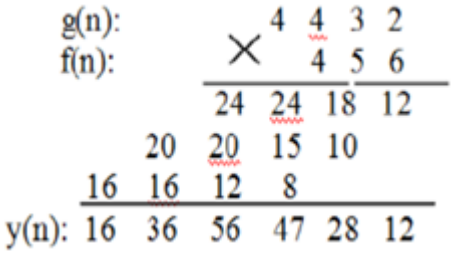


Fig 1: Convolution by Novel method

III. PROPOSED DESIGN OF CONVOLUTION

The convolution of two 4-bit numbers is designed and implemented using reversible logic. The multiplier and multiplicand are selected using two 4:1 multiplexers. Then the multiplication operation, that is, the Vedic multiplication is performed and is stored using 1:16 DE multiplexer. The first two bit of four bit select line of DE multiplexer is the select line of first 4:1 multiplexer. And the last of two bits are the select line of second 4:1 multiplexer. Then the corresponding products are added in the adder section.

The block diagram of the proposed design shown in below

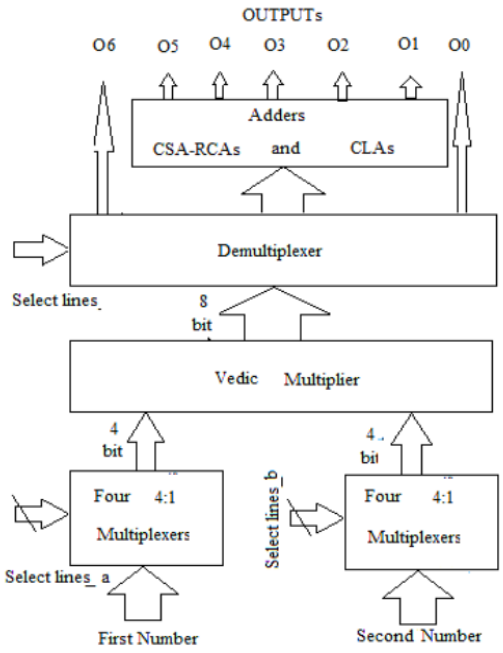


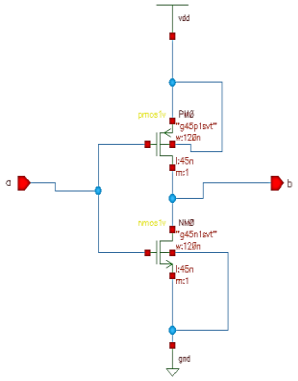
Fig 2: Block diagram of Convolution

For the addition of two 8 bit numbers carry look ahead adder is selected. And for the addition of three and four 8bit numbers carry save adder with last stage built by ripple carry adder is selected.

Design of initial circuit design:

First design initial blocks of multiplexer, de multiplexer, Vedic multiplier and adders this can be design by used initial gates are inverter, nand and nor gates etc. this gates are designed by using CMOS technique.

Schematic diagram of inverter (45nm):



IV. RESULTS

The design of Convolution is implemented in different technologies i.e 45nm ,90nm,180nm and results are compared. When comparing these technologies, 45nm technology requires less power and delay. The design is implemented using cadence tool in using virtuoso schematic editor, virtuoso symbol editor, and ADEL simulator. Comparison of power and delay of Convolution using Vedic multiplier in different technologies.

	45nm	90nm	180nm
Power	39.06uW	168.8uW	1.394mW
Delay	797.3ps	1.01ns	11.4ns

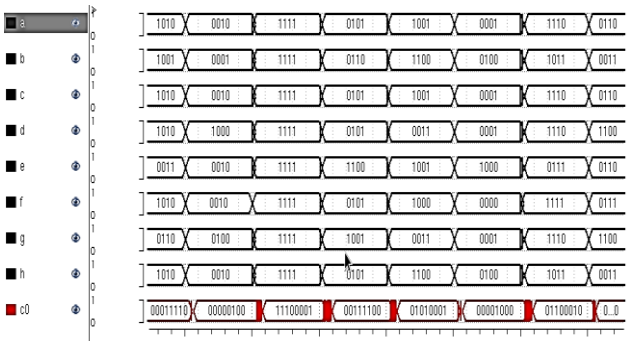
Comparison of power and delay of Convolution Using Vedic multiplier and other multiplier in 45nm

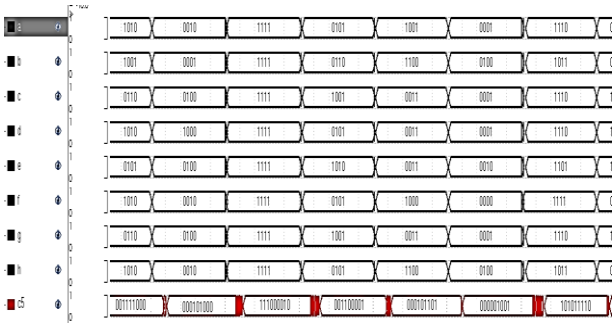
	Convolution Using Vedic multiplier	Convolution Using Wallace multiplier
Power	39.04uW	47.7 uW
Delay	797.3ns	881ns

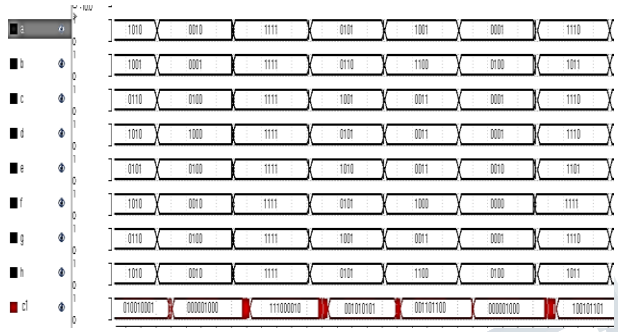
Simulation results of Convolution Using Vedic multiplier:

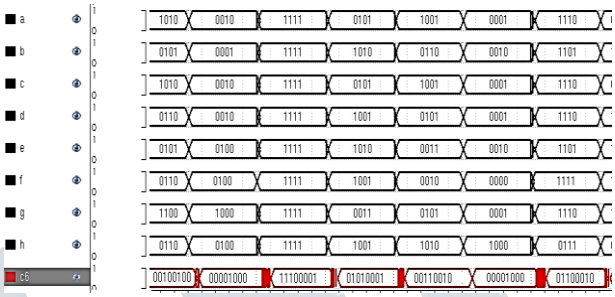
ISSN (Online) 2394-6849

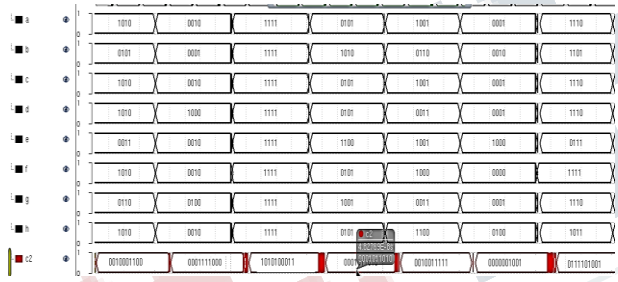
International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
Vol 4, Issue 11, November 2017

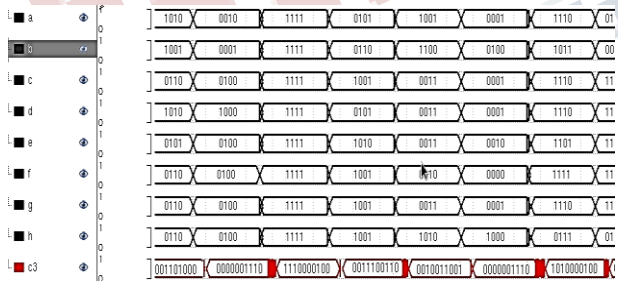


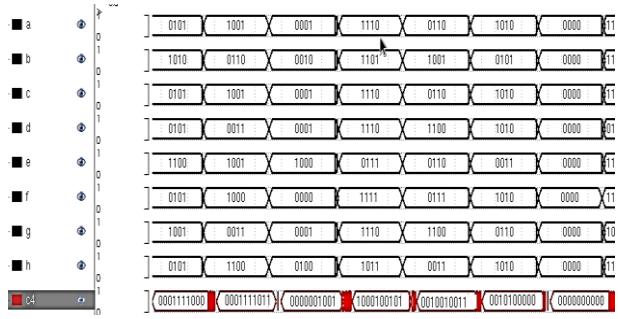












V. CONCLUSION

In this paper, Convolution of two finite length sequence is performed using Vedic multiplier and other multiplier. By comparing both design, It is obtained that Convolution Using Vedic multiplier is efficiency interms of both speed, power
and delay

REFERENCES

[1]. Khader Mohammad ,Sos Agaian, “Efficient FPGA implanting of convolution”, Proceeding of the 2009 IEEE international conference on system , Man, and Cybernetics, San Antonio, TX, USA –October 2009.

[2]. John W.Pierre ,”A Novel Method for Calucating the Convoluion Sum of Two Finite Length Sequences”, IEEE transaction on education, VOL.39, NO. 1,1996.

[3]. Cha Cheng ,Keshab K. Parthi, “Low- Cost Fast VLSI Algorithm for Discrete Fourier Transform”, IEEE, IEEE transaction on circuits and system, VOL. 54, 2007.

[4] Abdulqadir Alaqeeli, Janusz Starzyk, “Hardware implementation for Fast Convolution with a PN Code Using Field Programmable Gate”, Ohio University.