ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
Vol 4, Issue 11, November 2017

Power Reduction Testing Techniques of BIST, LFSR & ATPG for Low Power Circuits

[1] P. Ramesh, [2] Dr. D.N Rao, [3] Dr. K. Srinivasa Rao
[1] Assoc Professor, [2] Principal, [3] Principal
[1] ECE Department Joginpally BR Engg College, [2] Professor of ECE Department DRK Institute of science and Technology, [3] Professor of ECE Department TRR College of Engineering.

Abstract:- **The power techniques that reduce power consumption during test application are generally referred to as power-conscious testing, power-aware testing, power-constrained testing, or low-power testing. These terms will be interchanged for use throughout the chapter whenever fit. Built-in-Self-Test (BIST) is becoming an alternative solution to the rising costs of external electrical testing and increasing complexity of devices Small increase in the cost of the system reduces large testing cost. BIST is a design technique that allows a circuit to test itself Test pattern generator (TPG) using Linear Feedback Shift Register (LFSR) is proposed which is more suitable for BIST architecture. We have implemented Universal asynchronous receiver transmitter (UART) with BIST capability using different LFSR techniques and compared these techniques for the logic utilization in SPARTAN3 XC3S200-4FT256 FPGA device.**

Index terms **– BIST, VLSI Testing, Test Pattern Generation UART, LFSR.**

INTRODUCTION

During the last two decades, the numbers of power reduction techniques for testing have evolved. These techniques either explore the ATPG or deal with the test vectors to be used with external testing or explore the internal structure of design using BIST or DFT. So existing low-power testing scheme is divided into the following two categories.

(i) Low-Power Testing Techniques for Internal Testing using BIST, DFT
(ii)Low-Power Testing Techniques for External Testing using ATPG,ATE

Low-Power Built-In Self-Test Logic built-in self-test (BIST) is a DFT technique in which a portion of the circuit under test (CUT) is used to test itself. Because it can provide self-test ability, logic BIST is crucial in many applications, in particular, Low Power Testing one major objective of logic BIST is to obtain high fault coverage; however, a major issue is that power consumption during BIST can exceed the power rating of the chip or package. Increased average power can cause heating of the chip and increased peak power can produce noise-related failures we discuss a number of low-power BIST architectures and methodologies to reduce power consumption.

A logic BIST controller is required to control the BIST operation. The test pattern generator (TPG) automatically generates test patterns that are applied to the inputs of the circuit under test (CUT) and an output response analyzer (ORA) is used for compacting the circuit's output responses. In practice, in-circuit TPGs constructed from linear feedback shift registers (LFSRs) are commonly used for exhaustive, pseudo-exhaustive, or pseudo-random testing. This is mostly due to the fact that these LFSRs incur little area overhead and can be used as both TPG and ORA.

[1] low-power ATPG method for efficient capture power reduction during scan testing tries to achieve two goals: the primary one being the detection of targeted faults and the secondary one being the minimization of the difference between before-capture and after-capture output values of scan cells. This is achieved by introducing the concept of a capture conflict (C-conflict) in addition to the conventional detection conflict (D-conflict).

A C-conflict occurs when a difference between the before-capture and after-capture output values of a scan cell is created by logic value assignment during ATPG. A C-conflict, in the same manner as a D-conflict, may be avoided through the backtrack operation. However, backtracking for a C-conflict may make fault detection impossible. In this case, the backtracking for the C-conflict is reversed, and the

ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
Vol 4, Issue 11, November 2017

transition at the scan cell is tolerated since the primary goal is fault detection.
The second set of techniques to reduce test power is to use power-aware X-filling heuristics that do not modify the overall ATPG process. Given a set of deterministic test cubes, the main goal of these techniques is to assign values to the don't care bits of each test cube so that the number of transitions in the scan cells is minimized. By reducing the number of transitions in the scan cells during scan shifting, the overall switching activity in the CUT is also reduced; power consumption during test is thus minimized.

Most of the time, the X's are assigned with the help of the following classical non-random filling heuristics:
1.[4]Abstract. Test power is the major issue for current generation VLSI testing. ...
2.Introduction. The power consumption has been a major challenge to both design and test engineers. ...
3.Low-Power Test....
4.Low-Power Testing Schemes. ...

2. power dissipation classification during test application in bist rtl data paths:

This section gives taxonomy of power dissipation during test application in BIST RTL. Data paths. According to the necessity for achieving the required test efficiency, power dissipation is classified into necessary and useless power dissipation, as defined in the following.

1 Definition i) definition introduces spurious transitions when using BIST for RTL data paths.
2 tested modules during each test session and the power dissipated in test registers while
3Necessary power dissipation is compulsory for achieving the required test efficiency, however,
4 the useless power dissipation must be eliminated. In order to introduce useless power
5 dissipation, firstly spurious transitions in BIST RTL data paths are defined. While previous
6 sequential circuits at the logic level of abstraction the following

1 Definition ii) A spurious transition when employing BIST for RTL data paths is a transition
2 which occurs in modules and/or registers which are not used in the current test
3 These transitions do not have any influence on test efficiency since the values at
4 the input and output of modules and/or values loaded in registers are not useful test data.

1 Definition iii) Useless power dissipation is the power dissipated in registers and untested
2 modules due to spurious transitions which cannot be eliminated by any configuration of

3. Control signals of data path multiplexers.
Testing of integrated circuits (ICs) is important to ensure a high level of quality in product functionality in both commercially and privately produced products. In the modern System-on-a-Chip (SoC) design, many cores are integrated into a single chip. Some of them are embedded, and cannot be accessed directly from the outside of the chip. Such SoC designs make the test of these embedded cores become a great challenge. The Built-In-Self-Test (BIST) is one of most popular test solutions to test the embedded cores.[3]

[3]The UART is targeted at broadband modem, base station, cell phone, and PDA designs .In these devices serial data is transmitted via its serial port. It is a connector where serial line is attached and connected to peripheral devices such as mouse, modem, and printer and even to another computer. In contrast to parallel communication, these peripheral devices communicate using a serial bit stream protocol (where data is sent one bit at a time). The serial port is usually connected to UART, an integrated circuit that handles the conversion between serial and parallel data [4]. This paper focuses on implementation of UART with BIST capability using different LFSR techniques on Field Programmable Gate Array (FPGA) technology.

3. BIST CONTROL UNIT:

[5]BIST is an on-chip test logic that is utilized to test the functional logic of a chip. A generic approach to BIST is shown in Figure 1. BIST solution consists of a Test Pattern Generator (TPG), a circuit to be tested, a way to analyze the results, and a way to compress those results for simplicity and handling. With the rapid increase in the design complexity, BIST has become a major design consideration in Design-For-Testability (DFT) methods and is becoming increasingly important in today's state of the art SoCs. Achieving high fault coverage while maintaining an acceptable design overhead and keeping the test time within limits is of utmost importance. BIST help to meet the desired goals. The brief introductions of BIST control unit component are given below.

ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
Vol 4, Issue 11, November 2017

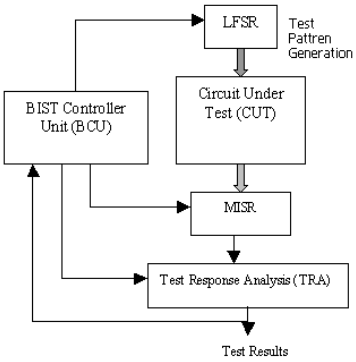

Figure 1: BIST Architecture

[3]BIST Controller Unit (BCU): It controls the test execution; it manages the TPG, TRA and reconfigures the CUT and the multiplexer. It is activated by the normal/Test signal and generates a Go/No go.

Test Pattern Generator (TPG): It generates the test patterns for the CUT. It is a dedicated circuit or a microprocessor.

The patterns may be generated in pseudorandom or deterministically

Test Response Analysis (TRA): It analyses the value sequence on PO and compares it with the expected output

Circuit Under Test (CUT): It is the portion of the circuit tested in BIST mode. It can be sequential, combinational or a memory. It is delimited by their Primary Input (PI) and Primary Output (PO).

4. BIST PATTERN GENERATION:

The following hardware pattern generation approaches have been used.

1.Binary Counters: A binary counter can generate an exhaustive test sequence, but this can use too much test time if the number of inputs is huge

2.ROM.: One method is to store a good test pattern set (from an ATPG program) in a ROM on the chip, but this is prohibitively expensive in chip area.

3 Linear Feedback Shift Register (LFSR): to generate pseudo-random tests. This frequently requires a sequence of 1 million or more tests to obtain high fault coverage, but the method uses very little hardware and is currently the preferred BIST pattern generation method.

4.LFSR and ROM: One of the most effective approaches is to use an LFSR as the Primary test mode, and then generate test patterns with an ATPG program for the faults that are missed by the LFSR sequence. These few additional test-patterns can either be stored in a small ROM on the chip for a second test epoch, they can be embedded in the output of the LFSR, or they can be embedded in a scan chain in order to augment the stuck fault coverage to 100%.

5. LFSR DESIGN:

[2]LFSR counters are design blocks that are used with advantage in many applications. One of their advantages is that the logical expressions for signals on the register inputs are simple and contain small amount of terms as well as signals that are built from. This allows to create large LFSR counters in PLD and FPGA devices without necessity to use multi-level logic.

Therefore, the counter is not slowed down and its speed (maximum clock frequency) is determined by the timing parameters valid for the one-level structure. It is easy to figure out that the radix-N polynomial requires N D-FFs. The coefficient of each exponent denotes the insertion points of exclusive-OR gates in the shifting path. When the LFSR starts, the LFSR is reset to zero first. Then the seed value is applied sequentially from I0. As the LFSR is operating in test pattern generation mode, the I0 is set to 0.

Different structures of LFSR will generate different sequence of test pattern. It means that if the BIST time is limited, the structure of LFSR will affect the BIST time and Fault Coverage (FC) of Circuit Under Test (CUT).

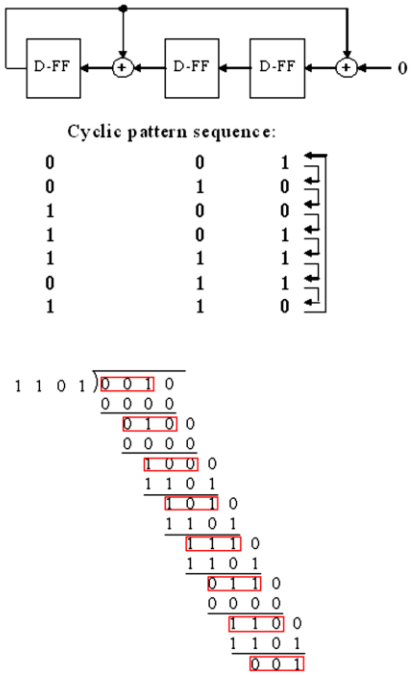

Figure 2 LFSR Design

ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
Vol 4, Issue 11, November 2017

6. UART BIST IMPLEMENTATION:

The BIST techniques with four LFSR based test pattern generation is incorporated into the UART design before the overall design is synthesized by means of recognizing the exiting design to match builtin test requirements as we discussed Test pattern generator is the very important part, which have different possible circuits.[5] Those possible circuits are as follows:

LFSR Type I

LFSR type I is commonly used TPG; it consists of D flip-flops and XOR gates in front of flip-flops. There are n flip-flops, so it is called an n-stage LFSR. LFSR can cycle through 2n-1 distinct states, the only omitted state being the all 0 state.

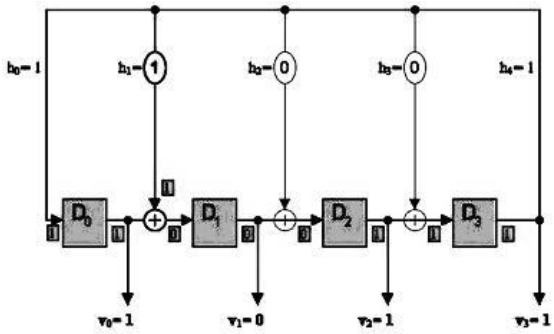

Figure 3 LFSR Type I

LFSR Type II

LFSR type II is commonly used TPG, it consists of D flip-flops and XOR gates in external feedback. There are n flip-flops, so it is called an n-stage LFSR. LFSR can cycle through 2n-1 distinct states, the only omitted state being the all 0 state.

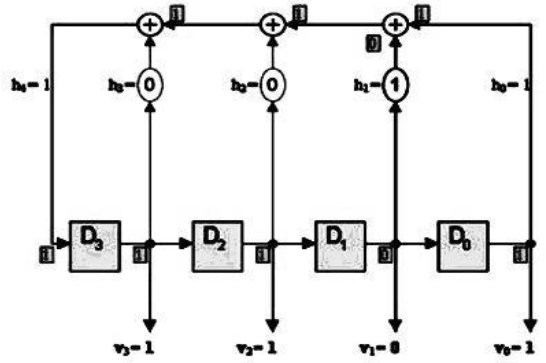

Figure 4 LFSR Type II

Figure 6 Cellular Automatons LFSR

Multiple Polynomial LFSR:

Multiple polynomial LFSR can change characteristic polynomial in determined time. LFSRs are more popular because of their compact and simple design. Cellular Automaton LFSR are more complex to design but provide patterns with higher randomness and perform better in detection of faults such as stuck-open or delay faults, which need two-pattern testing.

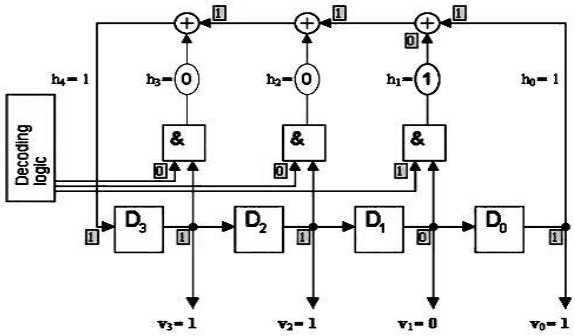

Figure 5 Multiple Polynomials LFSR

7. RESULTS AND CONCLUSIONS

The comparison of LFSR techniques on the basis of hardware is shown in table 1. It was observed that number of configurable logic blocks used after the implementation of the BIST techniques is increased from 74 to 103 slices of the total slices. Area overhead results an increase in delay from 44.7 ns to 74.24 ns. The area overhead is somehow reasonable considering test performance obtained from these methods & gives the choice of the different LFSR methods with minimum area overhead or delay.

TABLE: 1 COMPARISON OF AREA OVERHEAD AND DELAY OF LFSR TECHNIQUES

	COMPARISON OF AREA OVERHEAD AND DELAY OF LFSR TECHNIQUES			
Number of	UART	UART LFSR 1	UART LFSR II	LFSR Multiple polynomial LFSR

ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
Vol 4, Issue 11, November 2017

Slices (CLB) **2448**	74	103	103	108
Slice (FF) **4896**	64	104	104	101
4 input LUTS **4896**	114	155	154	160
Bonded IOBS 66	17	13	12	13
GCLKS **2**	1	2	2	2
DELAY(ns)	44.7	70.24	70.5	64.4

8. REFERENCES:

[1] Mohd Yamani Idna Idris "A VHDL Implementation of UART design with BIST capability" Malaysian Journal of Computer Science, Vol. 19 (1), 2006

[2] Chakrabarty, et. al, "Deterministic Built-in Test Pattern Generation for High-Performance Circuits Using Twisted-Ring Counters," IEEE Trans. of VLSI Systems, Vol. 8, No. 5, pp. 633-636, Oct. 2000

[3] S. Wang and S.K. Gupta, "DS-LFSR : A New BIST TPG for Low Heat Dissipation", IEEE Int. Test Conf., pp. 848-857, October 1997.

[4] P. Girard, "Survey of low-power testing of VLSI circuits," IEEE Design and Test of Computers, vol. 19, no. 3, pp. 80–90, 2002.

[5] S. Kundu and S. Chattopadhyay, "Efficient dont care filling for power reduction during testing," in Proceedings of IEEE International Conference on Advances in Recent Technologies In Communication and Computing, pp. 319–323, 2009.

[6] Sybille Hellebrand, Birgit Reeb, Steffen Tarnick"Pattern Generation for a Deterministic BIST Scheme" ACM/IEEE International Conference on CAD 95 (ICCAD-95), San Jose, Ca., November 1995

[7] http://www.ui.savba.sk/diag/tools/testability.html

P.RAMESH Associate Professor, Joginpally B.R.Engineering College, Hyderabad, Completed his B.E.(CBIT) from Osmania University and Masters of Technology from JNTUH and now he is pursuing PhD from JNTU Hyderabad. He has published 6 International Papers, attended 3 National Conferences and attended many workshops in India. He has total 15 years of experience, 5Yearsof the Industrial Experience and 10 years of the Teaching Experience.. He has Attended as a Judge for many national level Paper & Poster Presentations. He has Conducted a National Conference on "Innovative & Emerging Trends in Engineering Technology"(IETET-2014) and Conducted a workshop on Robo Galaxy-14 Association with IISc- Bangalore,

Dr. D.N RAO B.Tech, M.E, Ph.D, Principal of DRK Institute of Science and Technology Hyderabad. His carrier spans nearly three decades in the field of teaching, administration, R&D, and other diversified in-depth experience in academics and administration. He has actively involved in organizing various conferences and workshops. He has published over 11 international journal papers out of his research work. He presented more than 15 research papers at various national and international conferences. He is currently approved reviewer of IASTED International journals and conferences from the year 2006. He is also guiding the projects of PG/PhD students of various universities

Prof.Dr.K.Srinivasa Rao ME,Ph.D,MIEEE, MISTE, MSEMC, MBESI, FIETE,FIE(I), Principal, TRR College of Engineering. He has 35 years of teaching experience and published 45 technical papers. He is an active member of IEEE, FIE, FIETE, MISTE, MSEMS. He is a resource person of SONET, visiting professor for ISTE and has organized many technical events. He is presently guiding s10 research scholars, two PhD scholars are completed under his guidance.