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Digital Down Converter design to process bit frequency in Ground Penetrating Radar to measure soli profile

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Abstract:- **The designing of Digital Down Converter in matlab simulink is disccuse in this paper.The proposed Digital Down Converter(DDC) of the SFCW Ground Penetrating Radar is designed for the frequency range of 200MHz to 1200MHz. DDC is used for the processes bit frequency and attenuate IF frequency. The DDC model that we are using in GPR is based on orthogonal mixing.**

Keywords: **DDC,Digital filter,GPR**

I. INTRODUCTION

Ground Penetrating Radar (GPR) uses electromagnetic technique. This technique is used for surface exploration, characterization and monitoring. With this technique quickly and non-invasively high resolution image of surface feature is produce. GPR has application in many domains such as archeology, geology, Non-Detective Testing (NDT), civil engineering and defense security. It helps to locate landmine (metallic and non-metallic) and arms pilling. [1] GPR has four part antenna, transceiver, processing unit and display unit. In GPR, electromagnetic signal are transmitted into ground. The dialectic property of soil changes transmitted signal. These signals are processed in processing unit to forms the image of ground. This is the basic working principal of GPR. [2] In radar and communication system receiver is very important and its operation directly affects the performance of the system. DDC is located between the A/D converter and the DSP processor. DDC consist of digital mixer, decimation section and digital filters part. DDC is used for reducing the bit-rate of digital signal i.e. it transfer high bit-rate digital signal to low bit-rate digital signal. The importance of doing this is that the receive signals are processed by the DSP in real-time. As simulink provides Graphical programming environment for modeling, simulating and analyzing multidomain dynamic systems. Its primary interface is a graphical block diagramming tool and a customizable set of block libraries it is practical and efficient to design DDC in matlab simulink.

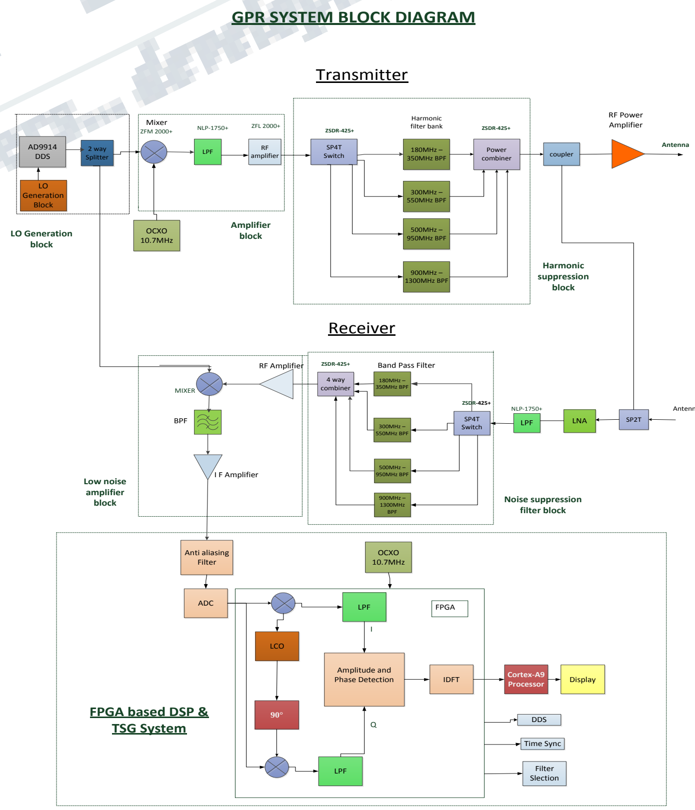

Figure 1 Block diagram of GPR

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II. THEORY OF DDC

The DDC used in GPR is based on orthogonal mixing. In DDC digital signal from A/D converter are mix with signal generated by Numerically Controlled Oscillators (NCO). The NCO generates the signal which has frequency same as that of transmitted signal frequency that is IF frequency and phase difference of π /2[3]. The output signal from NCO mix with received digital signal that will produce the signal of sum and difference frequency component and phase difference of π /2. The output signal of mixer pass through CIC (Cascaded Integrator-Comb) filter, compensation FIR filter, Programmable FIR filter. The importance of digital filtering is that it reduce noise cause by aliasing during decimation and maximize the receive signals signal-to-noise (SNR) ration. This digital filtering is also used to reduce sample rate of digital signal the DDC based on orthogonal processing is shown in figure 2

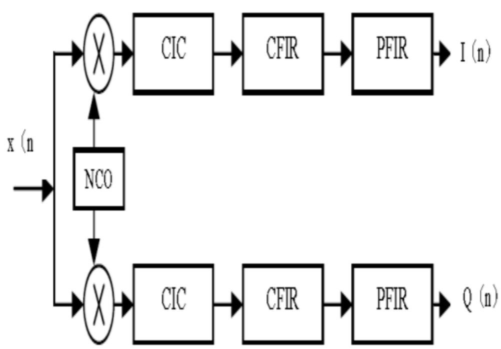


Figure 2 DDC modle based on orthogonal processing

Simulink design of DDC

A Digital mixing section

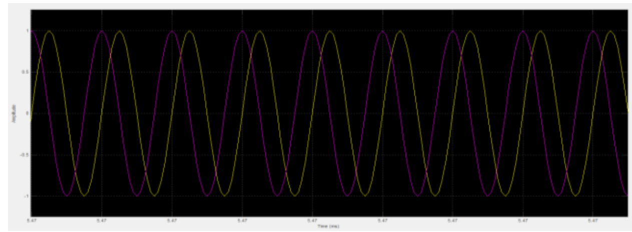
In many digital communication system NCO is very important component. Sine and cosine wave generated by the NCO has a frequency which is given by the equation; $s(n) = \sin(\omega_c n) = \sin(2\pi\, n\, f_c \,/\, f_s)$, where f_c has the frequency equivalent to IF frequency and f_s has the frequency same as the sampling frequency of the input signal.

In NCO f_s = 200MHz, spurious free dynamic range (SFDR) is 96dB and frequency resolution is 0.0233Hz. To generate output frequency of 10MHz the required phase increment is:

$$\Delta\theta = \frac{f_c\, 2^N}{f_s}$$

=(10MHz*2^32)/200MHz = 214748364.8

The digital mixer output is:



Figer 3 NCO output signal

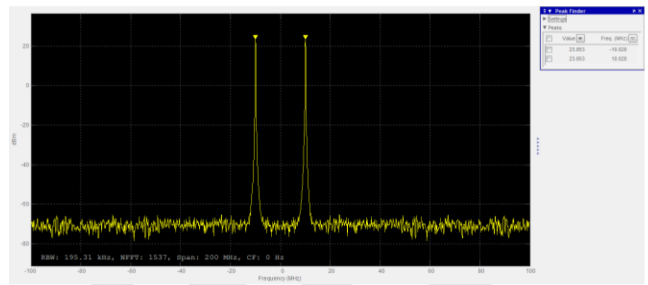


Figure 4 NCO output signal frequency

C CIC filter

CIC filters input impulse response given by:

$$h[n] = \begin{cases} 1, & 0 \le n \le D-1 \\ 0, & \text{else} \end{cases}$$

Where D is the rate change[4]. The CIC filter has a two section, one is the integrator section and como section as shown:

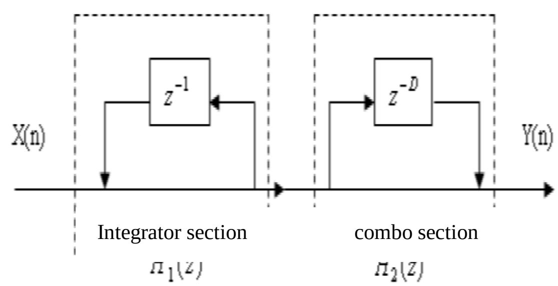


Figure 5 CIC filter

The magnitude response of 5 stage CIC filter is:

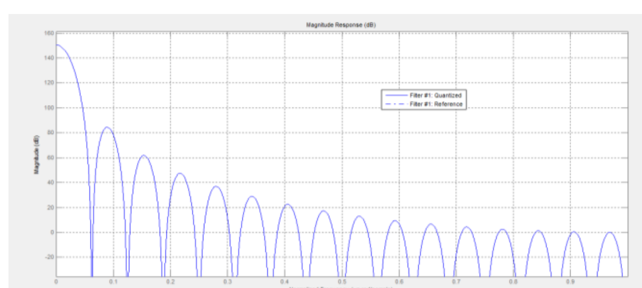


Figure 6 Magnitude response of CIC filter

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In GPR CIC filter is design to reduce sample rate by 32

C CFIR filter

For large number of stages CIC filter has a frequency response which is does not have a wide, flat pass band. As CFIR filter has a magnitude response response inverse to that CIC filter is applied to overcome the magnitude drop to achive frequency correction[5]. The magnitude response of CFIR filter is:

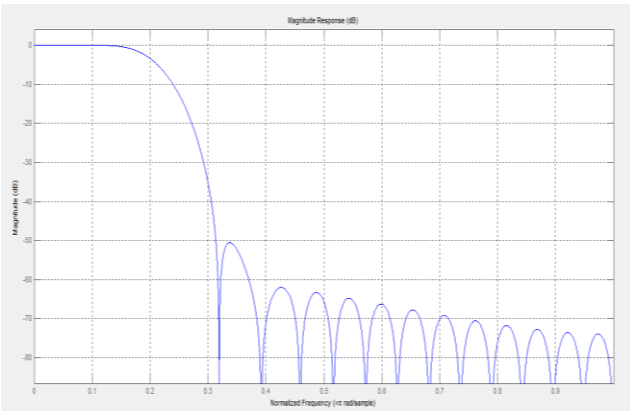

Figure 7 Magnitude response of CFIR filter

CFIR filter reduce the sample rate by 2

D PFIR filter

In DDC PFIR filter is used after CFIR filter as a shaping filter. It is design to reduce sampling rate by 2. The magnitude response of PFIR filter is:

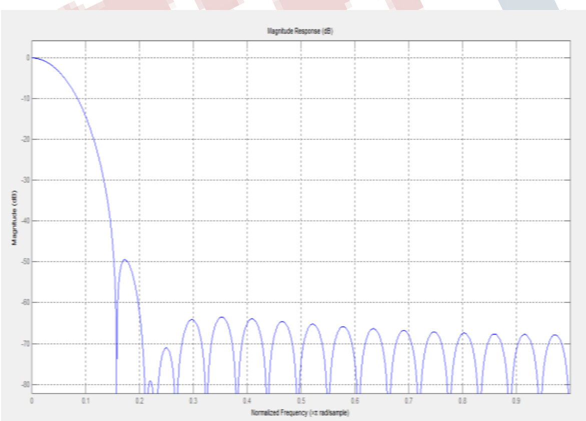

Figure 8 Magnitide response of PFIR filter

Simulation results

The simulink modal of DDC is design to processes bit frequency which is less than 200kHz and will attenuate all the above frequency. The output of DDC when NCO frequency is equal to that of IF frequency is:

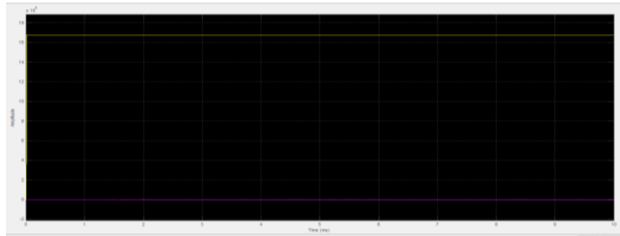

Figure 9 Output of DDC

(NCO and Input signal with same frequency)

Output signal of DDC when bet frequency introduce in a input digital signal is given:

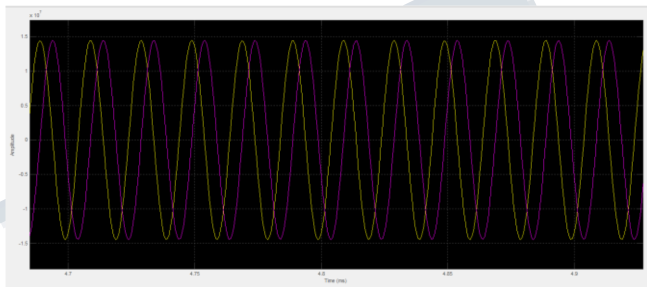

Figure 10 Output of DDC

(Input digital signal with Beat frequency)

Frequency of ouput signal of DDC is:

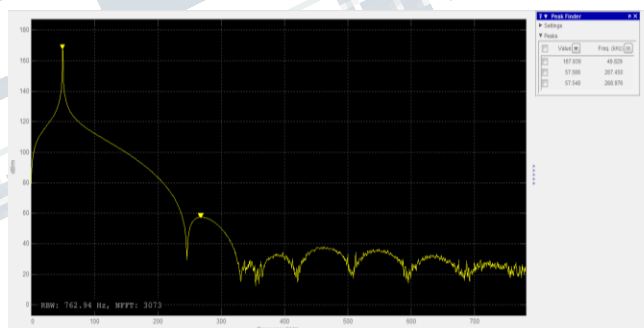

Figure 11 Frequency of output signal og DDC

Output of DDC when input siganl has a beat frequency which is grater than the design LPF filter range

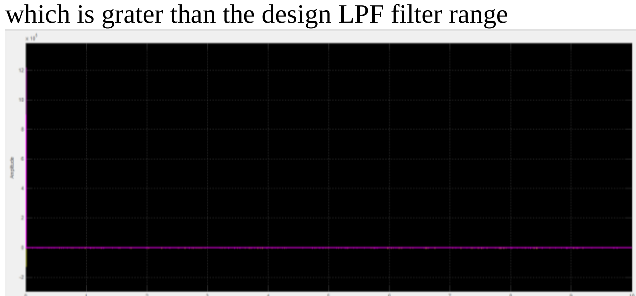

Figure 12 Output of DDC

(beat frequency greater than LPF filter range)

V. CONCLUSION

This paper is presented the simulink design of DDC. The design base is matlab simulink which is help to simplify design and reduce development time. As design is in simulink we can change the LPF filter specification by change parameter of each block. By observing result we can say that design DDC fullfil the system specification.

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