

# Design of High Speed 8 Bit Carry Look Ahead Logic for Arithmetic Operations

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**Abstract:** - This paper attempts to show the survey in 8-bit carry look ahead adder with Gate delay, propagation delay, and the total number of gates are listed. The circuits were built in .asl file and simulated using AUSIM L2.3. The operation of digital logic simulator called the Auburn University Simulator (AUSIM) is described. The AUSIM version L2.3 not only provides the simulation of non-hierarchical circuit descriptions, but also provides an area and performance audits of the cell.

**Keywords** – Carry look ahead adder, gate delay, propagation delay, Ausim 12.3.

## I. INTRODUCTION

The analysis of the total number of gates, gate delay and propagation delay for the 8bit carry look ahead adder circuit. The connection of AND, NAND, OR, NOR in the combinational circuit are described. The 8-bit CLA circuit has the least gate delay and propagation delay of 6 and 20 and maximum of 25 and 127 respectively.

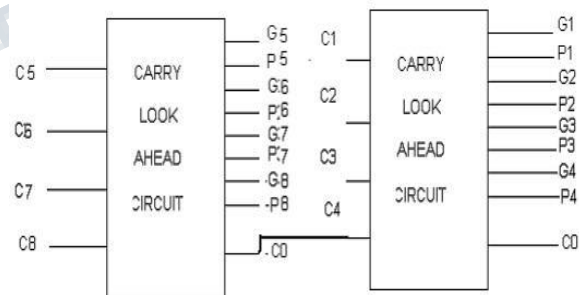
## II. AUSIM OVERVIEW

Logic simulation has become essential in ensuring that a digital design is correct prior to actual implementation of the hardware. The process of ensuring the correctness of a digital logic circuit through simulation is often referred to as design verification. One of the inputs to any logic simulation tool is a description of the digital design in some hardware description language. The hardware description language for Auburn University Simulator. AUSIM is the Auburn Simulation Language (ASL). In addition to providing simulation for debugging and verifying digital designs, AUSIM provides audits which can aid in debugging a circuit or in analyzing a circuit in terms of area and performance metrics. This version of AUSIM (version L2.3) simulates digital circuits described as elementary logic gates (AND, OR, NOT, NAND, and NOR gates).

## III. CARRY LOOK AHEAD ADDER

A carry-lookahead adder (CLA) is otherwise named as fast adder. It is a type of adder used in digital logic circuit. The

major advantage of the CLA is that the speed is increased by reducing the amount of time required to determine carry bits. The calculation of one or more carry bits before the sum in the carry-look ahead adder will reduce the wait time to calculate the result of the larger value bits. The logic of Carry look ahead adder always use the concept of generating and propagating carries.



$$P_i = A_i \oplus B_i$$

$$G_i = A_i B_i$$

The output Sum and carry can be defined as

$$S_i = P_i \oplus C_i$$

$$C_{i+1} = G_i + P_i C_i$$

Where  $G_i$  is known as Carry generate signal and  $P_i$  is known as Carry propagate signal. The major advantage of using CLA is reduced propagation time (delay) and it gives the fastest addition logic.

#### IV. AUSIM SOFTWARE DESCRIPTION

The AUSIM process involves two input files namely: ASL (Auburn Simulation Language) file and a vector file. These input files can be generated by any text editor program but these files should be saved as text files. The ASL description comprises of two statements namely circuit statement and component statement. The circuit statement for a full adder circuit can be given by the syntax as:

**CKT:ADDER IN:A B C OUT:S C;**

In the component statement the name of the comp (NOT, AND, OR, NAND, NOR) is used as the keyword instead of the "CKT" keyword. Every gate is given with unique names. The vector file is an input stimulus file which specifies the input patterns to be applied to the circuit. The vector file can be represented by the syntax as:

#the input vector for the circuit is;

```
000      001      010      110
```

#### V. SIMULATING WITH AUSIM

To access AUSIM L2.2, copy the AUSIM executable (ausim.exe) into the directory containing the ASL and vector files if we want to simulate. From the Windows Explorer or My Computer, double click the ausim.exe icon in the directory file. The AUSIM window should appear. The AUSIM window consists of three main areas:

- 1) The Input/output File Control section at the top left hand side of the window
- 2) The Circuit Statistics list at the top right hand side of the window
- 3) The Process and Simulate buttons and Status dialog area at the bottom of the window.

#### VI. ENTERING FILE NAMES

The first step upon entering AUSIM is to specify the names of the input and the output files. These can be entered individually by moving the cursor to the appropriate file name box, clicking the left mouse button, and entering the full name of the associated file name. The input files include the ASL file and input vector (or VEC) file. The output files include the audit (or AUD) file and simulation results (or OUT) file. Alternatively, default file names can

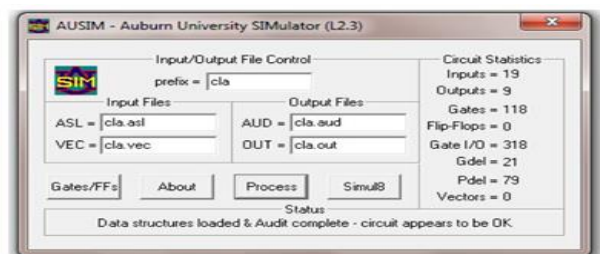
be specified by the user by typing the file prefix into the text box that appears in the top center of the Input/output File Control section. As the file prefix is typed in the "prefix" textbox, the names of the various input and output files appear in their respective text boxes with their default file suffix ("asl" for the ASL file, ".vec" for the VEC file, ".aud" for the AUD file, and ".out" for the OUT file). By using the default naming convention, all files associated with a given circuit have the same prefix and can be easily found in directories containing multiple circuits or versions of a circuit. The default naming convention of the ASL and VEC files must be saved and named with the correct file suffix ("asl" and ".vec", respectively).

#### VII. PROCESS OF .ASL FILE

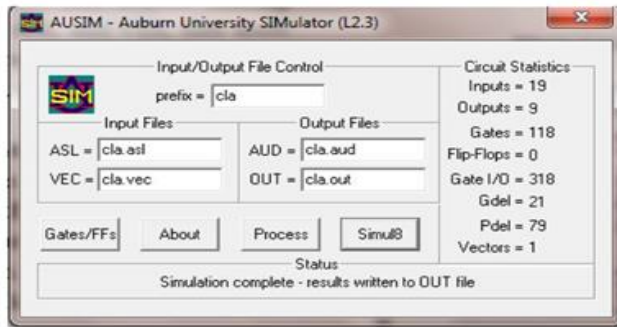
The names of the files have been specified, the ASL file must be processed by AUSIM. This is accomplished by clicking the Process button. The result of the ASL file includes the following steps: Check to see that the ASL file exists. In case of failure to find the file will result as a "can't find ASL file". If there are any syntax errors in the ASL description check the syntax of the ASL file. It will result in a message "Syntax Errors in ASL file - check 'ausim\_errs.txt' for any details". Count the number of gates driven by signal nets the internal data structures for subsequent simulation as shown in the figure 1. Perform an audit of the circuit to look for connectivity problems. Problems found will result in a status box message - "Circuit errors encountered - check 'ausim\_errs.txt' and AUD file. The audit of the circuit looks for problems such as:

- unconnected gate inputs (nets with no driving source).
- unconnected outputs (nets with no
- loads, other than primary outputs).
- multiple gates driving the same signal net.
- duplicate gate names.
- Generate an audit file for the circuit and Post the circuit statistics box with data for the circuit.

#### VIII. PROCESS OF CLA



**Fig 2. Process of 8 bit CLA in AUSIM**



**Fig 3. Simulation of 8 bit CLA in AUSIM**

```

Timing Path Analysis:
path= s0->t0->c0: Gdel=2, Pdel=9
.
.
path= s8->t16->c8->g7->a7: Gdel=4, Pdel=15
.
.
path= s8->t17->f17->c8->h10->c7->h9->c6->h8->c5->h7->c4->h6->c3->h5->c2-
>h3->h2->p0->k1->z->b: Gdel=21, Pdel=79
.
.
path= s8->t17->f17->c8->h10->c7->h9->c6->h8->c5->h7->c4->h6->c3->h5->c2-
>h4->h1->p1->k2->m1->a1: Gdel=21, Pdel=79
.
.
Worst Case: Gdel=21, Pdel=79
    
```

### X. PROGRAM FOR 8 BIT CLA:

```

# comment ;
CKT: cla in: a b c0 a1 b1 a2 b2 a3 b3 a4 b4 a5 b5 a6 b6 a7 b7 a8 b8 out:
s0 s1 s2 s3 s4 s5 s6 s7 s8 ;
and: y in: a b out: g0 ;
not: n1 in: a out: m ;
not: n2 in: b out: z ;
and: u in: m b out: k0 ;
and: v in: a z out: k1 ;
or: r in: k0 k1 out: p0 ;
not: n3 in: p0 out: f0 ;
not: n4 in: c0 out: f1 ;
and: u1 in: f0 c0 out: t0 ;
and: v1 in: f1 p0 out: t1 ;
or: r1 in: t0 t1 out: s0 ;
#comment
    
```

This part of program is used multiple times for executing the 8 bit carry look ahead adder.

- $C1 = G0 + P0C0$
- $C2 = G1 + P1C1$
- $C3 = G2 + P2C2$
- $C4 = G3 + P3C3$
- $C5 = G4 + P4C4$
- $C6 = G5 + P5C5$
- $C7 = G6 + P6C6$
- $C8 = G7 + P7C7$

These formulas are used for the generation of carry(s) C1.....C8.

### XI. SIMULATION RESULTS

```

Area Analysis:
Number of primary inputs: Pi= 19
Number of primary outputs: Po= 9
Number of gates: G= 118
Number of flipflops: FF= 0
Number of gate I/O pins: Gio= 318
Gate type and number of uses:
AND: 55
OR: 27
NOT: 36
    
```

### XII. OUTPUT

```

# AUSIM (L2.3) Simulation Results ;
# cabababababababab ssssssssss ;
# ab01122334455667788 012345678 ;
0101101010101101001 100000000
0111101010101101001 010000000
1100101010111001001 000001111
1110101010111001001 100001111
1101010110011110001 000110111
1111010110011110001 100110111
0100111010100011011 110001110
0110111010100011011 001001110
0001101110010110001 000111011
0011101110010110001 100111011
1010011001001001101 010111000
1000011001001001101 100111000
0000000001111111111 000001111
0010000001111111111 100001111
0000000000000000000 000000000
0010000000000000000 100000000
1111111111111111111 111111111
1101111111111111111 011111111
    
```

**Fig.4. Result of the 8 bit CLA**

### XIII. SUMMARY AND CONCLUSION

In this paper, Gate delay and Propagation delay of the 8 bit carry lookahead adder are found with the help of the AUSIM L2.3. Based on the simulation results the gate delay is found as 21 and propagation delay is calculated as 79 for the 8 bit carry look adder.

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