ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
Vol 4, Issue 12, December 2017

Analysis of 5-Bit Multiplier Using Reversible Logic

[1] Krishnapriya T [2] Lakshmipriya S, [3] Kiruthika T, [4] Swamynathan S.M
[4] Assistant Professor, Department of ECE, SNS College of Technology, Coimbatore, TN, India.
[1,2,3] UG Scholar, Department of ECE, SNS College of Technology¬, Coimbatore, TN, India.

Abstract: **- The Multipliers are the vital component of processors or computers. A Multiplier is one of the key hardware blocks in most digital signal processing systems. It plays an important role in digital filtering, digital communication and spectral analysis. Multiplication is very expensive and slows the overall operation. The performance of many computational problems dominated by the speed where the multiplication operation can be executed. Power dissipation becomes one of the primary design constraints. So we are going to analyse multipliers using reversible logic gates.In current scenario, the reversible logic gate attracting more interest due to low power consumption. The goals of reversible logic is to minimize the garbage, number of an inputs, total number of gates and delay.Under ideal conditions, reversible logic gates produce zero power dissipation.The applications of reversible logic circuits such as low power CMOS, Nanotechnology and optical data processing DNA computing and quantum computing.**

Keywords**: Reversible logic gates, Partial product generation (PPG), Multi-operand addition(MOA), Complementary metal oxide semiconductor(CMOS).**

I. INTRODUCTION

Reversible logic gates has a power to decrease the power dissipation which is sufficient in low power VLSI design. By Landauer's research,for every irreversible bit operation, the amount of energy dissipated is atleast KTln2 joules where K=1.3806505*10-23m2kg-2k-1(joule/kelvin-1)is the Boltzmann's constant is the temperatureat which the operation is performed. The heat generated due to the loss of one bit of information is very small at room temperature. When the number of bits is more as in the case of high speed computational works the heat dissipated will be large in which result is the reduction of lifetime of the components and performance. Reversible computing strongly affects digital logic designs. Reversible logic elements are needed to recover the state of inputs from the outputs. Besides that also, the growing area of quantum computation established a promising application of reversible logic. To realize a reversible logic circuit some restrictions must be considered, fan out and feedback are not allowed. In this paper, the important building blocks in most of the computing systems, multiplier is designed using reversible logic gates in the direction to optimize the quantum parameters which decide the performance of a reversible logic circuit.

REVERSIBLE LOGIC CIRCUITS

A reversible logic gate is an n-input n-output logic device that is one-to-one mapping. It helps to determine the outputs from the inputs and also the inputs can be uniquely recovered from the outputs .There are many parameters in determining complexity and performance of circuits. The number of constant inputs refers to the number of inputs that are to be maintained constant at either 0 or 1 in order to synthesize the given logical function. The number of unused outputs present in a reversible logic circuit is called as the number of garbage output. We can't avoid the garbage outputs as these are very essential to achieve reversibility. The well-known gate whose quantum cost is specified and add up their quantum cost to calculate total quantum cost.

BASIC REVERSIBLE LOGIC CIRCUITS:

Feynman Gate/CNOT Gate:This figure.1 shows a 2*2 Feynman gate. The input vector is (A, B) and the output vector is (P, Q). The outputs are defined as P=A, Q=A B. Quantum cost is 1.

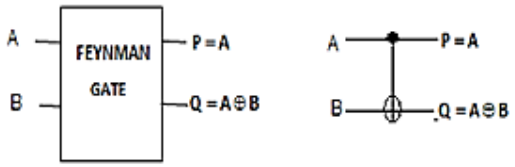

Fig.1.Feynman gate

Toffoli Gate:It shows a 3*3 Toffoli gate. The input vector is X (A, B, C) and the output vector is Y(P, Q, R). The outputs are defined by P=A, Q=B, R=AB C. Quantum cost of a Toffoli gate is 5. It is known as "controlled-controlled-not" gate, which describes its action.it has 3-bit input and output; If the 2-bits are set, it inverts the third bit, otherwise all bits stay the same.

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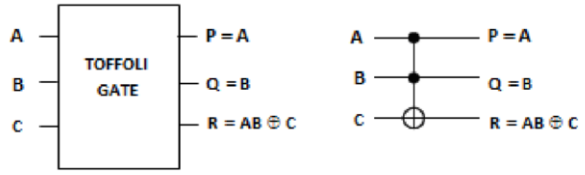


Fig.2. Toffoli gate

Peres gate(PG): It shows 3*3 peres gate. The input vector is X(A,B,C) and the output vector is Y(P,Q,R). The output is defined by P=A, Q=A XOR B and R=AB XOR C. Quantum cost is 4.

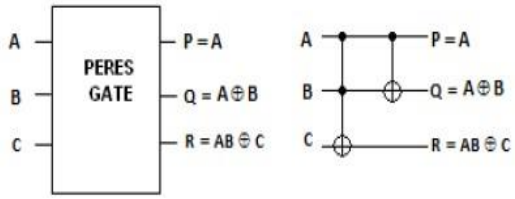


Fig.3. Peres gate

Double Peres gate (DPG):): It shows 3*3 peres gate. The input vector is X(A,B,C) and the output vector is Y(P,Q,R). The output is defined by P=A, Q=A XOR B and R=AB XOR C. Quantum cost is 4.

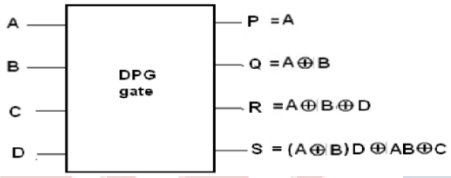


Fig.4.Double peres gate

REVERSIBLE MULTIPLIERS

Multipliers has major role because that they are the integral component of every computer system, cellular phone, micro phone etc. Multiplier circuits play an remarkable role in reversible computation, which ishelpful in various areas such as low power CMOS design ,optical computing bioinformatics. It is important for every processor to have low power and a high speed multiplier.The number of input is equal to the number of output. In addition to the available basic reversible gates, new gates are invented in order to optimize reversible circuits in terms of quantum cost. The new RS gate is proposed to implement reversible multipliers, main advantage is the number of gate will be reduced. This new RS gate is implemented using 2 Controlled NOT gates function as a XOR gate and AND operation is implemented using FRG gate and the quantum cost of RSG gate is 10.The new RS gate reduces the gate count when compared to the earlier RS gate which was implemented using Controlled NOT gates and the two Peres gates. The new RS gate is along with its quantum representation.

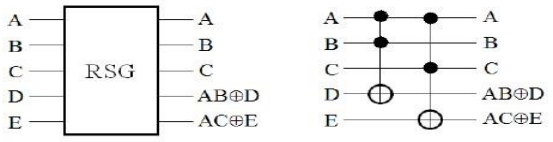


Fig.5.New RS gate and its Quantumrepresentation

REVERSIBLE SIGNED MULTIPLIER: Designing a multiplier using reversible logic gates is achieved by Partial product generation(PPG) and Multi-operand addition(MOA).

PARTIAL PRODUCT GENERATION:Using the partial product generation circuit is same for signed and unsigned multiplier. In the previous multiplier designs partial products are generated using Peres gates, and in order to use these product terms to multi - operand addition circuit, copying the gates are sufficient because of fanout obstruction in reversible logic circuits. The use of proposed RS gate not only reduces the number of gates required to produce partial product terms but also provide the sufficient number of product terms that exclude the necessity of copying gates. The entire partial product are generated and organized in an array. To determine the final product, the multi-operand addition is used.

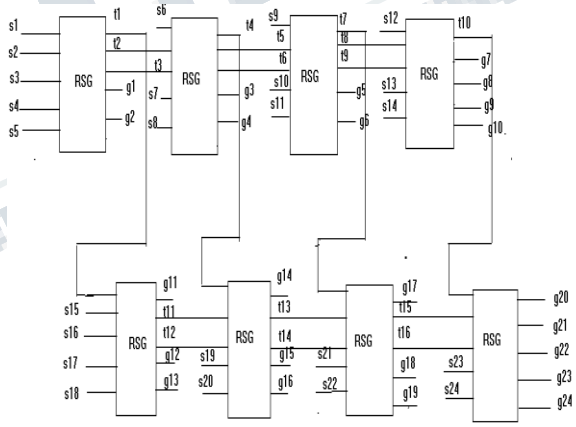
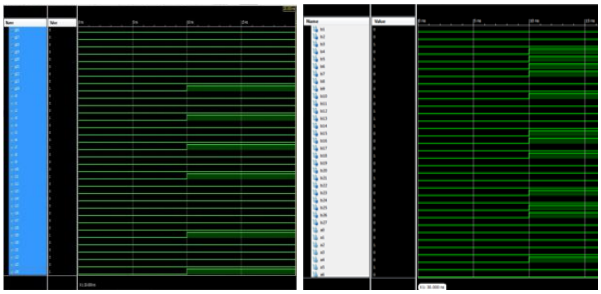


Fig.6. Partial Product Generation

OUTPUT WAVEFORM CONFIGURATION:



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MULTI-OPERAND ADDITION (MOA):MOA is a bit-arrays for unsigned and signed operands. It add up a bunch of numbers S=∑i=1 x(i). It is used in several algorithms like multiplication, recurrences, transforms and filters. The product terms generated from the PPG circuit are to be added to achieve the multiplier operation. For MOA, DPG and peres gate will function as same as full adder and half adder.

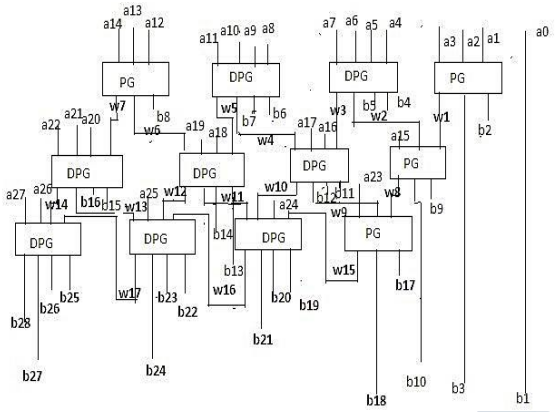

Fig.6. Multi-Operand Addition

II. RESULT AND COMPARISON

The analysis of multipliers using reversible logic gate is logically verified using XILINX 14.5 MODELSIM.
COMPARISON TABLE:

Parameter	Existing method	Proposed method	Altered method
LUTs	32	31	30
Average fan out	3.23	3.04	2.89
Delay	19.118ns	19.076ns	16.74ns

Maximum combinational path delay : 16.74ns
Number of IOs : 55
Number of 4 input LUTs : 30 out of 1536 1%
Number of slices : 17 out of 768 2%
Number of bonded IOBs : 54 out of 124 43%

III. CONCLUSION

By comparing existing and proposed method, the altered method decreases the delay and fan out. The reason to go for VLSI based software is to provide best results in three major criteria are low power dissipation, high speed and area. The efficiency of a multiplier in any processor depend on this three key points. Analysing the multiplier using reversible logic gate decreases delay by 16.74ns.In Future, the choice for creating computational devices is based on Reversible logic gate technology. These circuits can provide solution to propagation delay problems, low power dissipation, increases speed and efficiency of multiplier.

REFERENCES

[1] Mohan D.V.R, Vidyamadhuri K (2017): "Design of low power multiplier using reversible logic", in IJARCCE, Vol.6, Issue 3. pp.96-102.

[2] Karthikeyan A, Pradeep V, Praveen kumar G, Lakshmanan S (2015):"An efficientVLSI implementation for 64 bit error tolerant adders", in IJARSE,Vol.4,Issue 4,pp.596-603.

[3] Sharath B.P, Suhas K.V (2013): "A New approach to the design and implementation of multipliers using reversible logic", in ISSN,Vol.2, Issue 10, pp. 20-23.

[4] Karthikeyan A, Rajeshwarwan N (2012): "Design and implementation of multiple fault diagnosis on VLSI circuits using artificial neural networks", International Journal of Advances in Engineering and Technology,pp.685-695.

[5] Nielsen M and Chuang I (2000): 'Quantum Computation and Quantum Information', Cambridge Univ. Press, 2000.

[6] Thapliyal H and Srinivas M.B (2006): 'Novel Reversible Multiplier Architecture using Reversible TSG gate', in Proc. of IEEE Int. ConE on Computer Systems and Applications, March pp. 100-103.

[7] Zhirnov V. V, Cavin R.K, Hutchby J. A and BourianofI G.l (2003): 'Limits to binary logic switch scaling - a gedanken model', in Proc. of the IEEE, vol. 91, no. 11, pp. 1934-1939.

[8] G. Naveen Balaji, S. Chenthur Pandian, D. Rajesh "Fast Test Pattern Generator using ATALANTA M 2.0" Asian Journal of Research in Social Sciences and Humanities (Annexure I) Vol. 7 No. 2 (Feb 2017) pp. 721-729 ISSN: 2249-7315 DOI: 10.5958/2249-7315.2017.00124.1

[9] G. Naveen Balaji, V. Aathira, K. Ambhikavathi, S. Geethiga, R. Havin "Low Power and High Speed Synchronous Circuits using Transmission Gates" Asian Journal of Research in Social Sciences and Humanities (Annexure I), Vol. 7 No. 2 (Feb 2017) pp. 713-720. ISSN: 2249-7315, DOI: 10.5958/2249-7315.2017.00123.X