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Design and Implementation of a High Speed Multiplier Using Reversible Logic

[1] Vinutha P [2] Praveen Kumar Y G
[1]Student, M. Tech (VLSI and Embedded Systems), SSIT, Tumakuru
[2]Asst.Prof, Dept. of ECE, SSIT, Tumakuru

***Abstract:* -- The core of all the digital signal processor(DSPs) are its multipliers and the speed of the DSPs is mainly determined by the speed of its multipliers. Latency and throughput are the two important parameters associated with multiplication algorithm performed in DSP application. The performance of multiplication in terms of speed and power is crucial for most of the digital signal processor applications. In this paper, a design of 32 bit multiplier using the nikilam sutra to minimize the power delay product of multipliers intended for high performance and low power applications.**

***Keywords*- vedic multiplier, nikilam sutra architecture, reversible logic.**

I. INTRODUCTION

Multiplication is the process of adding a number of partial products. Multiplication algorithms differ in terms of partial product generation and partial product addition to produce the final result. Higher throughput arithmetic operations are important to achieve the desired performance in many real time signal and image processing applications. With time applications, many researchers have tried to design multipliers which offer either of the following- low power consumption, high speed, regularity of layout and hence less area or even grouping of them in multiplier. However, the two design criteria are often in conflict and that improving one particular aspect of the design constrains the other. The need of fast multiplication has gives rise to algorithms such as Baugh-Wooley method, Booth multiplier using recoding bits, Modified Booth algorithm (MBE). Although the MBE is most successful algorithms yet it is also a time consuming process. Nowadays, new methods are required for even faster multiplication strategies. The conventional mathematical algorithms can be simplified and even optimized by the use of Vedic mathematics. By using this technique we can improve the computational speed of processor to perform fast arithmetic operations.

The reversible logic design attracting more interest due to its low power consumption.Reversible logic is very important in low-power circuit design. The important reversible gates used for reversible logic synthesis are Feynman Gate, Fredkin gate, toffoli gate, New Gate sayem gate and peres gate .

Reversible computation in a system can be performed only when the system comprises reversible gates. Reversible circuits do not lose in formation, and can generate unique output vector from each input vector and vice versa (i.e., there is a one-to-one mapping between the input and the output vectors). Landauer has shown that for irreversible logic computations, each bit of information lost generates kTln2 joules of heat energy, where k is Boltzmann's constant and T the absolute temperature at which the computation is performed. Bennett showed that kTln2 energy dissipation would not occur if a computation is carried out in a reversible way.

A time, area, power efficient multiplier architecture using Vedic mathematics.In this a comparative study of the array multiplier, Carry save multiplier, Wallace tree multiplier, Booth multiplier and Vedic multiplier was done in detail. The study clearly showed that though array and booth multipliers are faster among the conventional multipliers, they are so because of some trade-off with complexity and high power consumption respectively. A fast, low power multiplier architecture based on Vedic mathematics and new architecture for multiplication which uses the modified binary tree network (MBT). This architecture focuses on generating all partial products in one step. The generated partial products are added by the MBT network. This also showed evidence of increase in speed. Reduced bit multiplication algorithm for digital arithmetic. It mainly consisted of the in depth explanation of Urdhva tiryakbhyam sutra and the Nikhilam sutra. These sutras are the extracts from the Vedas which are the store house of knowledge. The former was suggested for smaller numbers and the latter was suggested for larger numbers. This paper showed that

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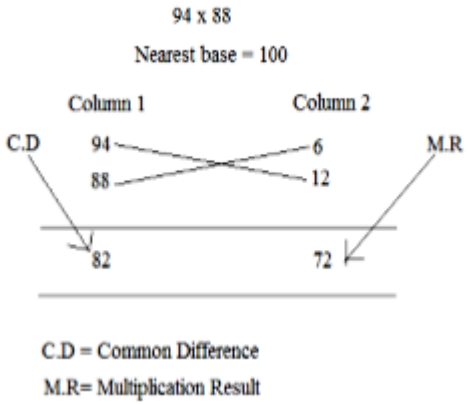
multiplication of two 8 bit numbers can be effected by reducing it further into two 4 bit numbers and likewise. This proposed a way to implement the design of the Urdhva sutra based multiplier as a bottom up design methodology.

It was very clearly evident from the explanations that, the Vedic square and cube architecture were faster than the conventional square and cube calculations. All the Vedic based calculations, sutra explanations and complete discussions were made. This does all explanations right from scratch. This contains the complete essence of the Vedic techniques, calculations and all the associated sutras with the explanations in detail. This forms the base and is the fundamental of any Vedic mathematics based calculations.

II. VEDIC MATHEMATICS- NIKILAM SUTRA



The Sanskrit term Nikhilam means "all from 9 and last from 10". It is also applicable to all cases of multiplication, but it tends to be more efficient when the numbers involved are large. This is because, it just finds out the compliment of the large number from its nearest base to perform the multiplication operation on it. Larger the original number, lesser the complexity of the multiplication. This sutra is illustrated by considering the multiplication of two decimal numbers (94 * 88) where the chosen base is 100 which is nearest to and greater than both these two numbers. The right hand side (RHS) of the product can be obtained by simply multiplying the numbers of the Column 2 (6*12 = 72). The left hand side (LHS) of the product can be found by cross subtracting the second number of Column 2 from the first number of Column 1 or vice versa, i.e., 94 - 12 = 82 or 88 - 6 = 82.

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III. CONCLUSION

I design of a vedic multiplier of nikilam sutra has been implemented that consumes less delay and less power.

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