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# High-Speed, Low Area and Energy Efficient 32bit Carry Skip Adder using verilog HDL

[1] Konduru Lakshmi Bhanu Prakash Reddy, [2] Dr.S.Vijaya Kumar
[1] PG Scholar [2] Associate Professor,
[1][2]Dept.of ECE Sreenivasa Institute of Technology and Management Studies
Chittoor A.P, INDIA

***Abstract:*** **-- Adders are basic essential component used in DSPs Processors and Digital filters and widely used in the Digital Integrated Circuits and also in Analog ICs.In this paper, a carry skip adder structure that has a higher speed, Low area as well as lower energy consumption compared with other adders is presented. The speed and reduction in the design area can be achieved by using "HYBRID MUX" instead of conventional MUX for skip logic in the existing method. In addition, instead of utilizing compound gates (AOI&OAI), the proposed structure makes use of "HYBRID MUX" for the skip logic. The Proposed structure assessed by comparing their speed, delay, area & energy parameters with those of other adders using a 45-nm static CMOS technology. The results that are obtained by Xilinx tool. Simulation reveals, on average 45% and 40% improvements in the delay &energy, respectively compared with conventional one. The power delay product is the lowest among all adders.**

***Keywords*:-- Hybrid Mux, cska, nmos pmos, xor gate, high speed, low area**

## I. INTRODUCTION

The increasing demand for mobile electronic devices requires use of power efficient, low area and high speed in VLSI Circuits. Addition is the most arithmetic operation and addition plays an important role in processors, Filter designs and DSP Applications.

Adders are a main building block in ALUs [1] and hence reducing their power consumption and increasing their speed mainly affect the speed, area and power consumption of DSPs, Filters and processors. There are different methods on the subject of minimizing the power and speed of these units, which have been discussed in [2]-[9].Truly, it is highly desirable to achieve higher speeds at low energy/power consumptions, which is a challenge for the designers of VLSI circuits.

One of the main techniques to lower the energy/power consumption of digital circuits is to reduce the supply voltage due to quadratic dependence of the switching energy on the voltage. A Complex DSP system contains many adders. The Designers are forced with more constraints are high speed , high throughput , small silicon area and low power consumption. Many design styles of adders exist in VLSI. Although, Ripple carry adders are the small in design structure but it's very slower. Recently, carry-skip adders are used popularly due to their performance of high speed and small size. There are many different adder families with different power consumptions, delays and area usages. The examples include RCA, CIA, CSKA, CSLA and PPAs may be found in [1] and [13].

The CSKA, which is an effective adder in terms of area usage, power consumption, was discussed in [17]. The critical path delay of the CSKA is much smaller than the RCA, but the power consumption and its area usage is similar to RCA. The power delay of the CSKA is smaller than that of the PPAs and CSLAs. In addition to this, due to small number of transistors, the CSKA benefits from the wiring lengths. The CSKA structure, on reducing its delay by using static CMOS Logic. The proposed method increases the speed considerably while maintaining the low power consumption and area properties of CSKA. Hence, the contribution of this paper can be summarized as follows.

1) Proposing a modified CSKA structure by using HYBRID MUX instead of conventional multiplexer and compound gates in the existing once. The rest of the paper is ordered as follows. Section II describes about the existing methods and section III describes about the proposed method. Section IV shows the simulation Results. Finally, the Conclusion is drawn in section V.

## II.EXISTING METHODS

***Conventional carry skip adder (existing method 1):***

The block diagram of an M-bit Conv. CSKA,

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contains the blocks of the RCA, is as shown in the Figure 1.In addition to the Chain of FULL ADDERs in each stage, there is a carry skip Logic.

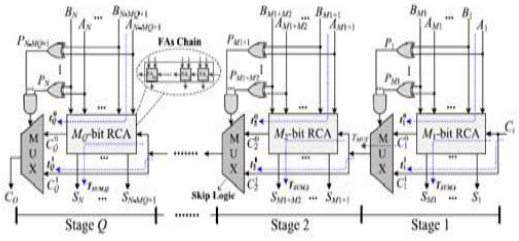


***Figure 1.Conventional Carry Skip Adder***

An RCA Contains M cascaded FULL ADDERS, the worst propagation delay of the addition of two M-bit numbers, A and B, belongs to where all the FULL ADDERS are in propagation mode. The CARRY SKIP operation can be performed by the multiplexers as shown in the above figure.

To design this conv.multiplexer 12 transistors are required. So propagation delay and also area of the design also increases. To reduce the propagation delay one may use the compound gates for the SKIP Logic. The Power consumption of the compound gates (AOI and OAI) smaller than that of multiplexer but the power consumption of the CI-CSKA (EXISTING METHOD 2) is more than that of CONV. CSKA.

***CI-CSKA Existing Method*** **:**

The block diagram is based on combining the concatenation and incrementation methods with the Cons-CSKA block diagram, and hence it is denoted by CI-CSKA.In this the skip logic replaced by compound gates and the sum can be produced from the incrementation blocks. The incrementation blocks contains xor gates and and gates (HALF ADDERS).The CI-CSKA as shown in the below Figure 2.

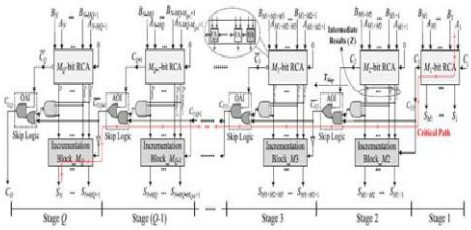

***Figure 2.CI-CSKA***

Due to this incrementation blocks area of the design increases and propagation delay also increases. In this adder the designer may give zero the carry input signal for the each RCA block as shown in above figure. On each consequent stage the is complemented and also one NOT gate is used to compliment the carry. It increases the delay area and power but speed of the operation is highest. But the SKIP LOGIC (AOI or OAI compound gates) is not able to bypass the zero carry input until the zero carry input propagates from the corresponding RCA block. To solve this problem, in the proposed method the SKIP logic can be implemented by using "HYBRID MUX".The details of proposed method is discussed in the following section.

## III.PROPOSED METHOD

***Proposed Hybrid CSKA:***

In the proposed method the Skip logic can be implemented by "HYBRID MUX" instead of conv. Mux and also compound gates. By using this hybrid mux speed of the operation increases, power consumption decreases and also the design area reduces. The proposed method of CSKA as shown in below Figure 3.

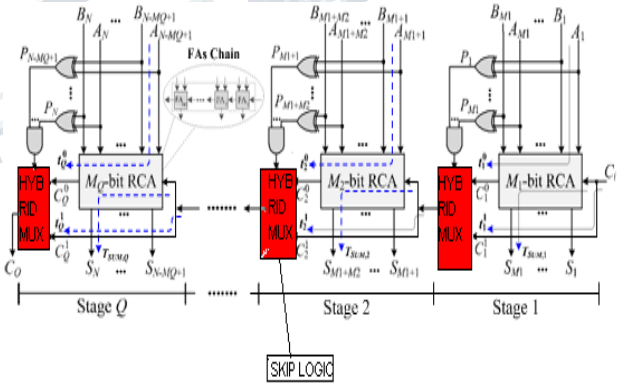


***Figure 3.Proposed Hybrid CSKA***

***HYBRID MUX*****:**

Hybrid mux is similar to the CMOS Inverter. The hybrid mux consists of one NMOS, one PMOS and two NOT gates. The structure of hybrid mux as shown in below Figure 4.It contains two inputs and one output and one conditional signal. The hybrid mux having one NMOS, one PMOS followed by two NOT gates as shown in the Figure

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4.To design the hybrid mux 12 transistors are required. The conditional signal is generated by the partial products of the input bits. All these partial products are applied to an AND gate to generate the conditional signal. If the conditional signal is equal to one NMOS transistor is ON and PMOS transistor is OFF. The NMOS is connected to the Cin and PMOS is connected to the Cout of the RCA block. If NMOS is ON the input carry signal is directly connected to the next stage. If the conditional signal is equal to the "zero" PMOS transistor is ON and NMOS transistor is OFF. The Cout of the RCA block can acts as a carry signal for next stage. It reduces the propagation delay of the carry, and also reduces the design area.

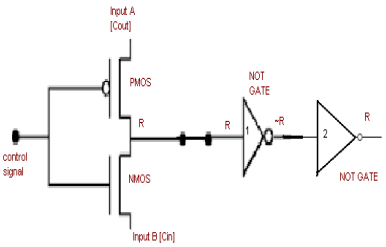


*Figure 4.HYBRID MUX*

## IV. SIMULATION RESULTS

In this the simulation results are obtained by using the Xilinx tool. The coding of the design is written in verilog HDL Language and Simulated. The Simulation is analyzed in Xilinx 12.1.The simulation results as shown in the Figure 5.Here the Table 1 shows the comparison of No. Of LUTs, Power consumption, delay and No. Of IOB's of the CONV CSKA, CI-CSKA, MODIFIDE CSKA and HYBRID CSKA.

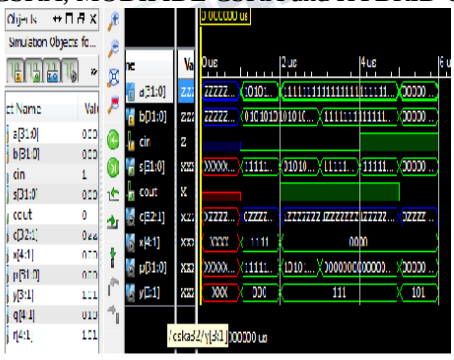

*Figure 5.Simulation Results*

***DESIGN SUMMARY*:**

| cska32 Project Status (02/17/2017 - 14:05:53) | | | |
|---|---|---|---|
| Project File: | lakshmi703.xise | Parser Errors: | 0 Errors |
| Module Name: | cska32 | Implementation State: | Synthesized |
| Target Device: | xc3s500e-4fg320 | •Errors: | 0 Errors (0 new) |
| Product Version: | ISE 12.1 | •Warnings: | No Warnings |
| Design Goal: | Balanced | •Routing Results: | |
| Design Strategy: | Xilinx Default (unlocked) | •Timing Constraints: | |
| Environment: | System Settings | •Final Timing Score: | |

Maximize

| Detailed Reports | | | | | [-] |
|---|---|---|---|---|---|
| Report Name | Status | Generated | Errors | Warnings | Infos |
| Synthesis Report | Current | Fri Feb 17 14:10:20 2017 | 0 Errors (0 new) | 0 | 0 |
| Translation Report | Out of Date | Mon Dec 5 15:28:57 2016 | 0 | 0 | 0 |
| Map Report | Out of Date | Mon Dec 5 15:29:02 2016 | 0 | 0 | 2 Infos (0 new) |
| Place and Route Report | Out of Date | Mon Dec 5 15:29:18 2016 | 0 | 0 | 1 Info (0 new) |
| Power Report | Out of Date | Mon Dec 5 15:08:11 2016 | 0 | 1 Warning (0 new) | 1 Info (0 new) |
| Post-PAR Static Timing Report | Out of Date | Mon Jan 30 15:50:54 2017 | | | |
| Bitgen Report | | | | | |

```
Partition Implementation Status
-------------------------------

  No Partitions were found in this design.

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Generating "PAR" statistics.

Timing Score: 0 (Setup: 0, Hold: 0)


Generating Pad Report.

All signals are completely routed.

Total REAL time to PAR completion: 14 secs
Total CPU time to PAR completion: 13 secs

Peak Memory Usage:  188 MB
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***TABLE 1:-Comparison of different CSKA***

| LOGIC Utilization | CONV CSKA | CI-CSKA | MODIFIDE CSKA | HYBRID CSKA |
|---|---|---|---|---|
| No. of LUTs | 72 Out of 9312 | 75 Out of 9312 | 68 Out of 9312 | 57 Out of 9312 |
| No. of bonded IOBs | 98 Out of 242 (42%) | 98 Out of 242 (42%) | 98 Out of 242 (42%) | 98 Out of 242 (42%) |
| Delay(ns) | 15.386 | 10.731 | 10.112 | 7.714 |
| Power consumption(%mw) | 17 | 16 | 16 | 6 |

## V. CONCLUSION

In this paper, a static CMOS CSKA structure called "HYBRID CSKA" was proposed, which exhibits a lower power consumption and lower design area and high speed compared with the conventional one. The high speed and low area and energy efficient can be achieved by using the hybrid mux for the skip logic in the proposed method. The simulation results suggested that the CSKA structure is a useful adder for the applications where the speed and energy consumption and area are critical.

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