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Low Power Design Techniques in VLSI System design through clock network optimization

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***Abstract*— Power reduction is of significant importance in VLSI designs. As VLSI technology goes further in nanometer technology, as speed increases power becomes an important parameter. There are various design techniques which can be used to reduce power. Optimization in synthesis and physical design stages can give significant power reduction. In this paper, power reduction through optimization of clock network in digital circuits is discussed.**

Index terms— Low power deisgn,low power Synthesis,VLSI design,Clock network optimization.

I. INTRODUCTION

Microelectronic VLSI circuits and designs with low power dissipation is something that the mobiles, laptops and battery operated electronic device markets requires. Power consumption of designed circuit can be calculated as

P = I*V Watts

Where I is the current from the power supply, and V is the supply voltage. One way to reduce power is by maximizing instantaneous power or average power [2]. Though power reduction is an important objective, in VLSI designs, reaching an optimum performance is always a design goal. It is seen that power reduction can be obtained by compromising on performance. In this kind of scenarios, low power techniques are preferred generally in circuits where having power minimization is significant. To balance this tradeoff, many combined metrics are suggested in different literatures. One example is, power-delay product. It is used in several digital designs as a standard metric. Huge compromise on performance to have power reduction is not good. The degradation in performance can be monitored by taking energy-delay product. Energy-delay product is the square of power-delay product. It can be considered in situations where design performance is of higher priority compared to power consumption [3].

In VLSI designs, low power techniques can be applied to designs at architectural, logical and circuit levels. In synthesis and physical design of digital circuits, optimizations at various levels can give power saving.
Major such techniques are explained in [1].

In every digital circuit, there will be power derived from data coming external sources, power generated within the module due to digital components within the module and clock power. For those circuits where clock power is an important factor, optimization of clock network can give significant power saving. Clock optimization techniques for VLSI digital designs are discussed in the following sections.

II. DYNAMIC POWER COMPONENTS

Total dynamic power of a digital circuit is given by the equation

Pdyn=A*C*(V^2)*F

Where Pdyn is the total dynamic power of the circuit, A is the activity factor, C is the total capacitance, V is the supply voltage and F is the frequency of operation. Activity factor A is defined as the fraction of circuit that is switching. At a given point of time activity factor may not be one always. Sometimes toggling of the nets are in such a way that, switching may not be a complete reversal from 1 to 0 or 0 to 1.This happens because of the fact that, interconnect capacitance may not be charged or discharged completely from the previous stage.

When node capacitance C is discharged and charged by input clock signal with frequency F and supply voltage V, then the charge change per cycle is given by C*V and the charge changed or moved per unit time (second) is given by C*V*F. As the charge is given at supply voltage V, energy dissipation per cycle, or the dynamic power, is C*V*V*F. The dynamic power of a synchronous flip-flop, that can change its state once in a cycle, will be 0.5*C*V*V*F. When capacitance nodes are gated by enable signals or when flip-flops do not toggle every cycle, their power consumption will be less. As a result, a parameter known as activity factor (0<A<1) is used to show the switching activity in average in the circuit.

In digital circuits or modules which are part of processors or large circuits, the supply voltage V and

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frequency of operation remains constant throughout the design life time. Then the 2 parameters remaining that can be controlled and optimized are activity factor A and parasitic and load capacitance C. Various methods to reduce the activity factor A of a circuit are discussed here .As VLSI technology goes deeper down in sub-micron technology, the dynamic clock power constitutes major portion of dynamic power. It is found that there are modules where 50% dynamic power is from clock network. In those modules if clock network is optimized, it can give significant power saving. In the following sections, different methods for clock network optimization are explained with diagram.

III. CLOCK NETWORK OPTIMIZATION TECHNIQUES

In deep sub-micron technologies, most of the power burning is coming from clock network. In this module concentration was given on the optimization of clock network. The general structure of a clock network is shown in Figure 3.1.

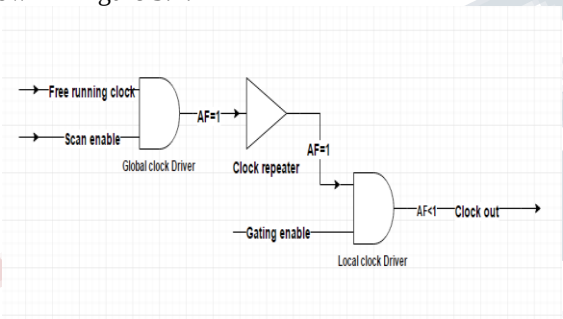

Figure 3.1:General clock network structure

Free running master clock is connected to a global clock driver. Global clock driver will be gated by a scan enable signal which will control mode of operation in DFT mode. The net after the global driver will be having activity factor of one. Total dynamic power is a function of activity factor, dynamic capacitance and supply voltage. Since supply voltage remains constant for a given process technology, controllable parameters are activity factor and capacitance.

One of the major aim is to reduce number of nets with high activity factor. Methods applied to reduce activity factor of nets and thereby total power are described below.

A. Merging of Clock enables

Every module has free running clock supply. A global clock driver will be providing the clock. The specialty of global clock driver is in such a way that, it is having an enable controlling the mode of work. All the modules are scan inserted in order to make Design for Testing easier. Global clock driver is having an enable signal which deactivates clock driver during DFT operation. This enable is always active during normal mode of operation.

Free running clock driver is driving local clock driver which in turn drives other cells in the circuit. Local clock buffers are having enable signals which are generated based on logic inside the module. Power can be reduced by minimizing activity factor and Dynamic Capacitance of a module. Merging of enables of global clock buffer and local clock buffer helps in reducing Activity factor of net which comes from free running clock.

B. Reduce number of clock cells

In deep sub-micron technology which aims at running for GHz frequency range, almost 50% of power is constituted by clock cells. Reduction of clock cells can improve reduction in power. Sometimes manual synthesis leads to structures where local clock cells can be merged together. If the drive strength required to drive two different nets are same, and if they are driven by different drivers, they can be merged together. It effectively will reduce dynamic power.

C. Remove clock cells between global clock driver and local clock driver

In general scenarios, if merging of global clock driver enable and local clock driver enable are not merged, another way is there to reduce power. If there are more number of cells in high activity factor non gated clock, then it will increase power. The number of cells driven by high activity net should be as minimum as possible. If there is a buffer or inverter in between global clock driver and local clock driver, it can be removed and can be added after the output net of local clock buffer where the AF is less. As a result dynamic Capacitance will be less.

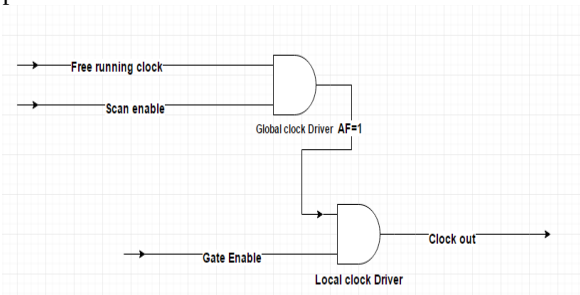

Figure 3.2:Removal of clock cell between global and local clock driver

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If there are any clock cells between global clock driver and local clock driver, they can be removed. If they were inserted for timing or driving purpose they can be added after the local clock driver so that functionality and timing remains same but the number of cells on high activity factor net becomes zero. This will in turn reduces overall capacitance as the cell is not toggling on free running clock.In Figure 3.2, clock cell, clock repeater is removed from the network.This is with respect to the reference figure, Figure 3.1.This helps in reduction of total number of clock cells.Clock cell from high activity factor net is removed.Methods depicted in B and C are depicted in Figure 3.2.

D. Reduce length of High AF net

In order to reduce power, the length of high activity factor net should be made as small as possible. One of the thumb rule for ensuring the same is to have an upper limit on the length of the net between global clock driver and local clock driver. Global clock driver and local clock driver should be placed as close as possible. This should be taken care in physical design. Since the output net of local clock driver is of less activity factor, as it is gated by an enable, it can be routed to larger distances.

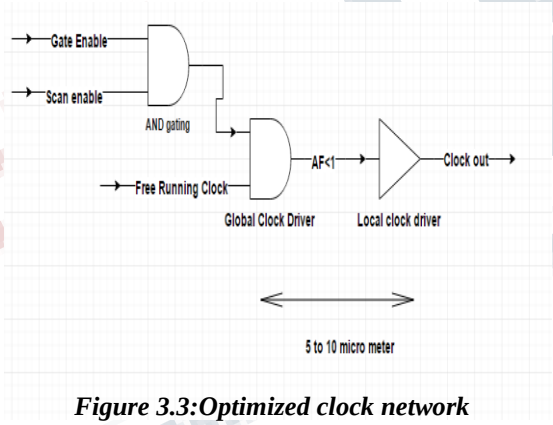

Figure 3.3:Optimized clock network

An optimized clock network is shown in Figure 3.3.. Merging of enables of global clock driver and local clock drivers are done. The distance between global and local clock drivers are restricted to 5 micro meter, so that the high activity factor net contribution will be limited. Merging of enables of global and local driver will reduce the activity factor of net, after global driver to less than one.

E. Splitting of local clock buffers

Global clock drivers typically will be driving many number of local clock drivers as shown in Figure 3.4. The enables of local clock drivers may be different. In that case merging of enables of global clock driver and local clock driver is not possible. This happens where the fan out of global drivers are more than one. In this case the global clock driver can be split and extra drivers can be added in such a way that, enables of local and global clock drivers can be merged. One factor which needs to be taken care is, power overhead from addition of new global clock driver should not be more than advantage obtained from splitting.

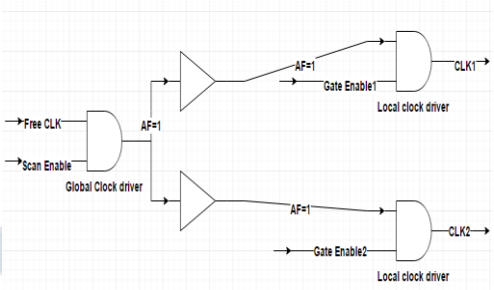

Figure 3.4:Global driver driving more than one local clock driver

In Figure 3.4, a global clock driver is driving 2 local clock drivers through 2 buffers. The nets before and after the buffer are having activity factor=1 which leads to more power. Direct merging of enables for global and local clock drivers are not possible here, as gating enable of local clock drivers are different.

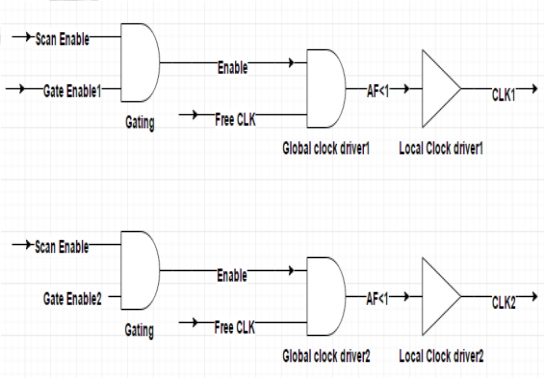

Figure 3.5:Splitting of local clock buffers from global driver

One possible solution in this case is splitting of global clock driver into 2.Each global driver will be driving different local clock drivers. After splitting merging of enables can be made possible. One other aspect of power saving from here is AND driver can be replaced by

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buffer. If power of standard buffer cell is less than that of standard AND clock cell, it can give further saving. Splitting and merging of clock drivers are shown in Figure 3.5.

IV RESULTS

Broadcast module which is part of microprocessor is analyzed here. All the above mentioned clock optimization techniques are applied on the module for power saving. The power distribution within the module is as given in Figure 4.1.

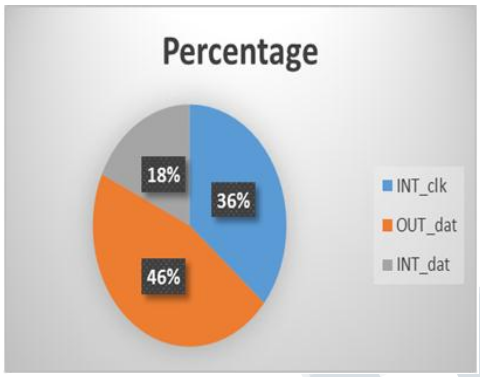

Figure 4.1:Power distribution before optimization

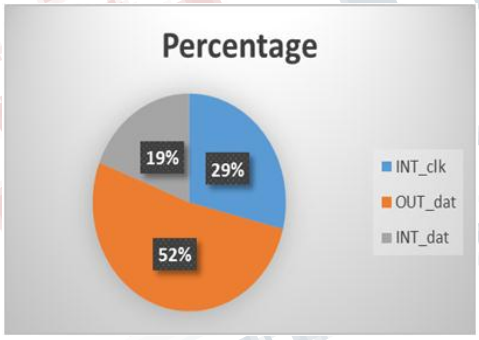

Figure 4.2:Power distribution after optimization

From the pie chart in Figure 4.1 it is clear that 36 percentage of total power is burned in clock network. Internal data is taking 18% of power and external data is taking 46% of power. Our aim is to apply clock network optimization techniques and reduce the percentage of clock power. As the percentage of clock power decreases, clock network will be optimized and power burned in clock network will be less After applying mentioned clock optimization techniques in the module, it is found that the percentage of clock power has reduced from 36% to 29%.Along with this, some logic optimization techniques are also applied as given in reference[1]. These techniques gave 8.553 % power saving. In TABLE 4.1 comparison of power before and after optimization is given. Total power saving obtained is 8.553 %. and is 5.4936 mw. Out of that 4.4515 mw power is saved by clock network optimization. Hence it is shown that significant power reduction is possible through clock network optimization as given in the above sections.

TABLE 4.1:Comparison of dynamic power

	Total Dynamic Power	Clock Power
Before Optimization	40.8437 mw	14.703 mw
After Optimization	35.3501 mw	10.2515 mw
Power saving	5.4936 mw	4.4515 mw
% Power saving	8.553	7

V. CONCLUSION

Low power designs are very important, especially in deep sub micron technology design processes.Dynamic power is the major contributor of power.In general clock network will be a major contributor towards power burning because high number of toggling of nets.
Certain methods are identifies to optimize clock network, that can save power.All these methods are applied in a module inside microprocessor and significant saving is observed.These techniques can be applied to digital VLSI designs in order to save power.These methods will be extremely useful, if clock network is a major contributor of power inside the considered module.

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