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Design and Implementaion of Booth Multiplier using optical reversible carry select adder with AOI logic

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***Abstract* - An important requirement of digital system design is to reduce Area, Propogation delay and Power dissipation. Reversible logic is one of the emerging technology for reducing Area, Delay and Power. The aim of this paper is to realize Booth multiplier using optical reversible carry select adder (ORCSA) with And-or-invert (AOI) logic. Optical reversible full adder (ORFA) and optical reversible mux (ORM) has been used for designing optical reversible carry select adder. Here two reversible gates i.e. Feyman gate (FG) and Toffolli gate (TG) are been used. Optical switches such as Beam combiner (BC) Beam splitter (BS) and Mach-zehender Interferometer (MZI) are also been used. The circuit has been implemented and simulated in Xilinx. The synthesis results shows that the proposed booth multiplier improves both interms of Area and Propagation delay over the conventional booth multiplier.**

Index Terms: Optical reversible gate (ORG), Optical reversible carry select adder (ORCSA), Optical reversible full adder (ORFA), Optical reversible mux (ORM), Feyman gate (FG), Toffolli gate (TG), Beam combiner (BC), Beam splitter (BS) Mach-zehender Interferometer (MZI).

I.INTRODUCTION

Area, Propagation delay and Power dissipation in electronic system is extremely crucial limiting issue which will be reduced or decreased with the assistance of optical reversible logic circuits. Based on G. Moore's law [1], amount of transistor counts to be incorporated per device region in products can almost dual in one and half year. To attain high speed computation, high appearance density with in the logic circuits is needed that effects in additional temperature reduction.The traditional process is found unable to cope with reduced power, high compaction and heat dissipation issues of the existing processing environment.In 1961, R. Laundaur [2] expressed that temperature reduction happens because of energy loss in irreversible logics. Every little bit of data dissipates an quantity of energy adequate to KTln2 joules where K is Boltzmann's Constant and T is the absolute temperature. In 1973, C. H. Bannett [3] explicit that reversible logic will over come the heat dissipation drawback of VLSI circuits as a result of bits of data don't seem to be erased in reversible computing.

New technologies are rising to manage these problems. Reversible Computing is one of the way to beat the matter of heat dissipation in computing chips that succesively facilitate in increasing the packaging density. Reversible Logic appears to be hopeful because of its wide application in rising technologies like quantum computing, optical computing and power efficient nanotechnologies etc. Reversible circuits don't lose data. A reversible gate has one to at least one mapping between input and output vectors i.e. range of input lines are adequate to range of output lines with in the reversible gate[12], [14]. Fan-out isn't allowed in the reversible logic. Constant inputs and garbage output line are often added to the circuit to make it reversible[12],[13], [14].

Optical Computing is computation with photon as opposed to typical electron based computation. Unequaled high speed and zero mass of photon have attracted the specialists towards the optical realization logic gates using Semiconductor Optical Amplifier(SOA) based Mach Zehnder Interferometer (MZI) switches.MZI switches are chosen because of its high speed, quickly dynamic, least energy and convenience in manufacture [4], [5], [6]. The authors have conferred the optical realization of standard reversible logic gates like Feynman and Toffoli Gates [4].

In this paper, we have proposed Booth multiplier using optical reversible full adder and 2x1 optical reversible mux. First, optical reversible MNOT gate using MZI switch is been realized, then optical realization of 4x4 Toffoli gate has been presented.

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Rest of the paper is organised as follows Section II describes basic building blocks of optical reversible logic design and exsisting methodologies.Section III describes optical reversible carry select adder with AOI logic, which will be implemented in Booth multiplier.Section IV describes the proposed Booth multiplier with optical reversible gates.Section V descibes the implementation results and finally Section VI is the conclusion part.

II. BASICS OF ALL OPTICAL REVERSIBLE LOGIC

Reversible logic are executed with optical innovation by utilizing some building blocks like MZI based optical switch, Beam splitter and Beam combiner.

2.1 SOA Based MZI Switch

An SOA based MZI switch can be outlined using two Semiconductor Optical Amplifiers (SOA-1, SOA-2) what's more, two couplers (C-1, C-2) [8], [9]. In a MZI switch, there are two wellsprings of information ports A and B, and two yield ports called bar port and cross port, independently, as showed up in Figure 1 and 2.

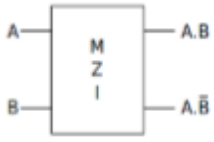

Fig.1. Block diagram of Mach-Zehnder Interferometer switch [8]

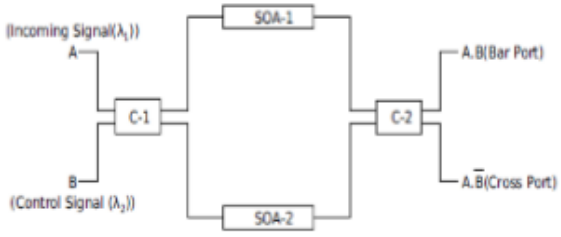

Fig.2. SOA based Mach-Zehnder Interferometer switch [8]

The optical sign at port B is named as the control signal what's more, signal at port A is named as incoming signal. At the moment that there are signal display at port A and port B at that point there is a presence of light signal at the bar port and nonattendance of light signal at the cross port. Without control signal at port B and proximity of incoming signal at port A, the yields of MZI are exchanged and comes about inside seeing light at the cross port and no light at the bar port. Here, nonappearance of light is considered as the justification regard 0 and presence of light is considered as justification quality 1.

This conduct of SOA based MZI switch can be composed as Boolean capacities having contributions to yields mapping as (A, B) → (P=A.B, Q = A.B), where A, B are the sources of data and P, Q are the yields of MZI, individually. The optical expense and the delay of MZI based all optical switch is considered as solidarity. The creators have considered the accompanying enhancement parameters for the all optical reversible rationales: optical expense i.e. number of MZI switches, number of BC and BS utilized as a part of the rationale circuit, and optical postponement i.e. number of phases of MZI switches utilized as a part of the outline of rationale circuit.

2.2 Optical Feynman Gate

The Feynman gate (FG) has mapping (A, B) → (P=A, Q=A⊕B) where A, B are the sources of data and P=A, Q=A⊕B are the yields, individually. The Feynman entryway can be acknowledged utilizing 2 MZI switches, 2 beam combiners (BC) and 3 beam splitters (BS) in all optical domain as appeared in figure 3 [4].

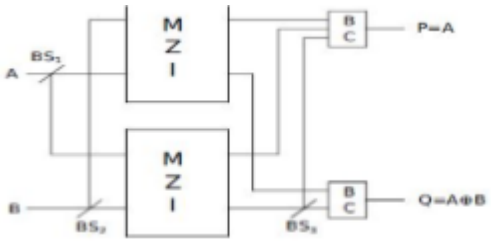

Fig.3. Feynman gate and its optical implementation [4]

2.3 Optical Reversible MNOT Gate

Another 2×2 optical reversible MNOT gate (1, A) → (P, Q) has been illustrated, where P=A and Q=A. Figure 4 demonstrates the Block chart of MNOT

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gate. This gate produces sensible NOT of the incoming logic A.

Fig.4. Block diagram of 2×2 MNOT gate

The optical reversible MNOT gate has been illustrated in figure 5. This gate is planned with single MZI switch. The approaching sign of MZI switch is set to 1 then yield produced at cross port is backwards of the contribution at control signal. The optical expense of MNOT gate is one. NO Beam Splitter (BS) or Beam Combiner (BC) is utilized as a part of this entryway. As stand out MZI switch is utilized, so the delay is 1Δ.

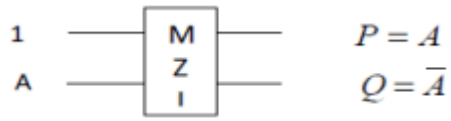

Fig.5. 2×2 Optical Reversible MNOT gate

2.4 Optical Realization of 4×4 Toffoli Gate

The 4×4 Toffoli Gate (4×4 TG) is mapped from incoming vector (A, B, C, D) to outgoing vector (P, Q, R, S), where P=A, Q=B, R=C, and S=D ⊕ABC, separately. Fundamentally, 4×4 Toffoli gate is Multiple Controlled Toffoli door (MCT) with 3.

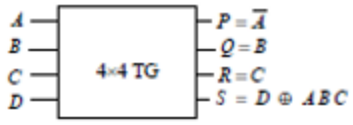

Fig. 6. Block diagram of 4×4 Toffoli gate

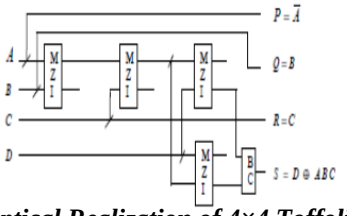

Fig. 7. Optical Realization of 4×4 Toffoli gate control lines.

Figure 6 demonstrates the Block diagram and Figure 7 Shows the optical acknowledgment of 4×4 Toffoli gate. This gate has been acknowledged with 4 MZI Switches, Five Beam splitters (BS) and one Beam Combiners (BC). The optical delay of this gate is considered as 3Δ.

II.B) EXSISTING METHODOLOGIES

2.5 Optical Reversible 2×1 Multiplexer

Here it is been explained how a 2x1 mux has been designed by utilizing MNOT gate and optical Toffoli Gate (TG) [4].Here we have two incoming ports(D0 and D1),a single outgoing port O and a select line S0 to choose one of the two incoming lines. The outgoing capacity of 2×1 Multiplexer is given by O=S0D0+S0D1. The optical realization of 2×1 Reversible Multiplexer is been illustrated in figure 8. It is formed with one MNOT and two TG gates. Here, MNOT gate acts as NOT gate. At the point when the third info line of TG is set to Zero, the TG carries on as AND gate.

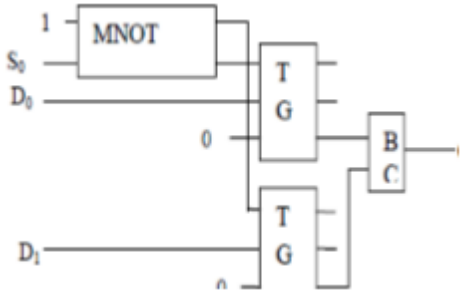

Fig.8. Optical Realization of 2×1 Reversible Multiplexer

2.6 Optical Reversible Full Adder

Here it explains about optical reversible full adder by using two optical reversible logic gates, they are optical feynman gate and ORG-I. The ORG-I is been illustrated in figure 9.

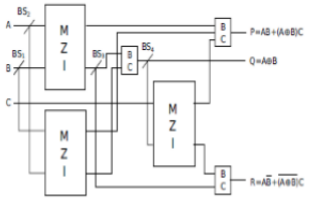

Fig. 9.Optical Reversible Gate (ORG)-I [8]

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ORG-I is mapped as (A, B, C) = (P, Q, R) where functions of P, Q and R are as illustrated in the block diagram. Optical reversible full adder circuit is been illustrated in figure 10.

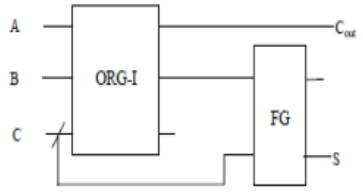

Fig.10 Optical Reversible Full Adder (ORFA)

Incoming bits A, B and C are passed to ORG-I gate. The output P of ORG-I gives the carry function of optical reversible full adder, output Q of ORG-I and input C are given to the incoming lines of feynman gate which gives the output sum function of optical reversible full adder circuit.The output of optical reversible full adder circuit is given by

S = A(+)B(+)C and Cout = AB+(A(+)B)C

III. PROPOSED OPTICAL REVERSIBLE CARRY SELECT ADDER WITH AOI LOGIC

Here optical reversible carry select adder is been designed using optical reversible full adder and optical reversible mux and AOI logic, the proposed optical reversible carry select adder will be less interms of device utilization summary and delay as compared to conventional carry select adder.

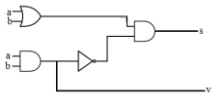

Fig.11 AND OR INVERT Gate(AOI)

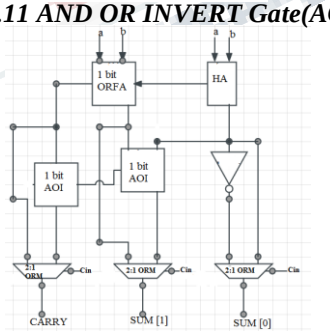

Fig.12 2 Bit Optical Reversible Carry Select Adder With AOI Logic

Fig.11 illustrates AOI gate in which a,b are inputs and S,V are outputs. Here we are using three wires K1, K2 and K3, Hence K1=a|b, K2=a&b, K3=~(a&b), therefore the outputs will be S=K1&K3, V=K2. By using AOI logic, no. of gates will be reduced & hence Area will be reduced.

Fig.12 illustrates 2-bit optical reversible carry select adder with AOI logic, Here we are using 1-bit optical reversible full adder, 1-bit half-adder, 2-bit AOI and three 2:1 optical reversible mux. a,b,Cin are taken as inputs. Sum[0], Sum[1] and Carry are taken as outputs. Using 2-bit optical reversible carry select adder, we can construct 16-bit optical reversible carry select adder and when we compare it to conventional carry select adder Area and propogation delay will be reduced, Also proposed carry select adder will be more faster.

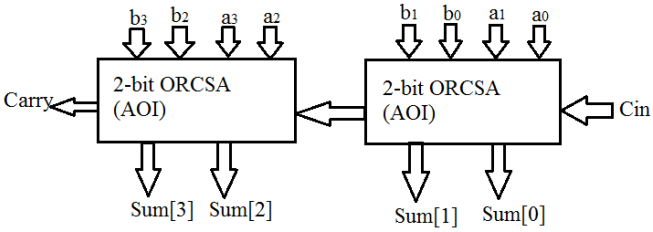

Fig.13 4-bit Optical Reversible Carry Select Adder with AOI Logic

Fig.13 shows 4-bit optical reversible carry select adder with AOI logic, which is designed by cascading two 2-bit optical reversible carry select adder. Inputs will be a[3:0], b[3:0], Cin and outputs will be Sum[3:0], Carry.

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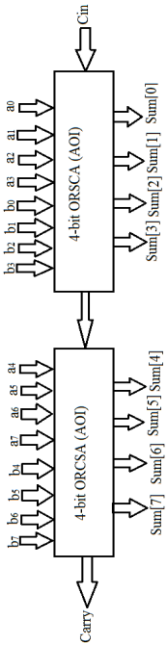

Fig.14 8-bit Optical Reversible Carry Select Adder with AOI Logic

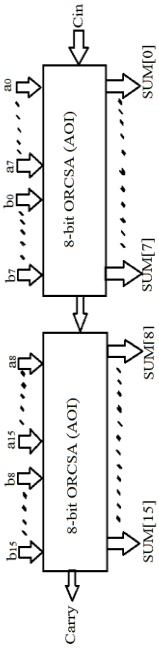

Fig.15 16-bit Optical Reversible Carry Select Adder with AOI Logic

Fig.14 shows 8-bit optical reversible carry select adder which is designed by cascading two 4-bit optical reversible carry select adder.

Fig.15 illustrates 16-bit optical reversible carry select adder which is designed by cascading two 8-bit optical reversible carry select adder.This 16-bit optical reversible carry select adder will be implemented in 8-bit Booth multiplier.

IV PROPOSED BOOTH MULTIPLIER

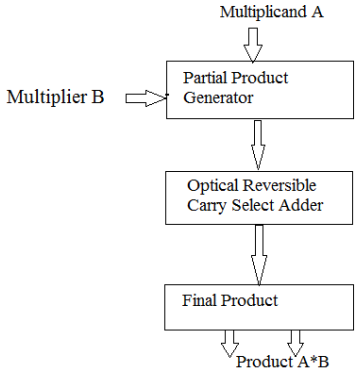

Fig.16 Proposed 8-bit Booth Multiplier

Fig.16 illustrates Proposed 8-bit Booth multiplier in which Multiplicand A and Multiplier B are given to a partial product generator through which 4 partial products are generated. Here instead of Normal adder we are using 16-bit optical reversible carry select adder, because of which delay taken by the adder will be less.Here the name,optical reversible carry select adder is given because we are using optical reversible full adder and optical reversible mux with the help of optical switches like beam combiner,beam splitter and MZI. Also reversible gates like Feynman and Tofolli gates are used.

By using this 16-bit optical reversible carry select adder with AOI logic Area and propogation delay in Booth multiplier will be reduced and hence booth multiplier will be more faster as compared to conventional booth multiplier.

V IMPLEMENTATION RESULTS

The Proposed 8-bit Booth Multiplier was designed and implemented in Verilog. Simulation was carried out using Modelsim 6.5 in Xilinx Spartan 3.

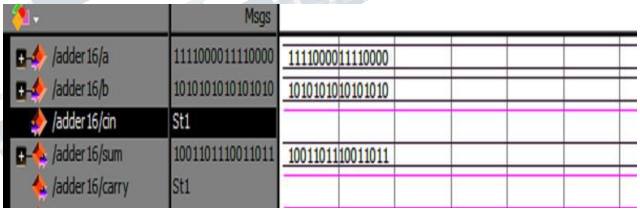

Fig.17 Simulation Results of 16-bit Optical Reversible Carry Select Adder

Here a,b, cin are inputs and sum,carry are outputs. So we are taking a as 1111000011110000,b=1010101010101010 and cin as 1, so we will get sum as 1001101110011011 and carry as 1.

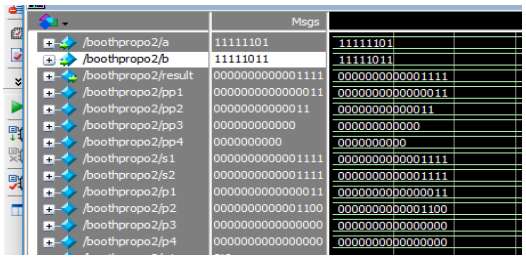

Fig.18 Simulation Results of 8-bit Booth Multiplier

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Simulation results of 8-bit Booth multiplier are shown, where multiplicand a is 11111101 and multiplier B is 11111011, Hence the result will be 0000000000001111.

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of 4 input LUTs	148	1,536	9%
Number of occupied Slices	80	768	10%
Number of Slices containing only related logic	80	80	100%
Number of Slices containing unrelated logic	0	80	0%
Total Number of 4 input LUTs	148	1,536	9%
Number of bonded IOBs	32	124	25%
Average Fanout of Non-Clock Nets	3.99		

Table.1 Device Utilization Summary of Proposed Booth Multiplier

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of 4 input LUTs	159	1,536	10%
Number of occupied Slices	84	768	10%
Number of Slices containing only related logic	84	84	100%
Number of Slices containing unrelated logic	0	84	0%
Total Number of 4 input LUTs	159	1,536	10%
Number of bonded IOBs	32	124	25%
Average Fanout of Non-Clock Nets	4.63		

Table.2 Device Utilization Summary of Conventional Booth Multiplier

By comparing Table.1 and Table.2 we can say that no. of gates used in table.1 are less. Hence Area is reduced in Proposed Booth multiplier.

IBUF:I->O	33	0.715	1.750	b_1_IBUF (b_1_IBUF)
LUT4:I1->O	1	0.479	0.000	adr11/a1/g1/g1/g3/carry_and000084_SW1
MUXF5:I1->O	1	0.314	0.704	adr11/a1/g1/g1/g3/carry_and000084_SW1
LUT4:I3->O	2	0.479	0.804	adr11/a1/g1/g1/g3/carry_and000084 (ad
LUT3:I2->O	4	0.479	0.838	adr11/a1/g1/g1/g4/carry1 (adr11/a1/g1
LUT3:I2->O	2	0.479	0.804	adr11/a1/g1/g2/g4/out7 (adr11/a1/g1/g
LUT3:I2->O	2	0.479	0.804	adr11/a1/g1/g2/g5/out1 (N8)
LUT3:I2->O	2	0.479	1.040	adr11/a1/g1/g2/g5/out2 (sum1<6>)
LUT4:I0->O	1	0.479	0.976	csa1/s7/Mxor_sum_xo<0>_SW1 (N228)
LUT4:I0->O	4	0.479	1.074	csa1/s7/Mxor_sum_xo<0> (sum<6>)
LUT4:I0->O	1	0.479	0.000	cla1/a1/g1/g2/g1/g3/carry_F (N282)
MUXF5:I0->O	3	0.314	0.794	cla1/a1/g1/g2/g1/g3/carry (cla1/a1/g1
LUT4:I3->O	2	0.479	0.915	cla1/a1/g1/g2/g2/g3/carry (cla1/a1/g1
LUT4:I1->O	1	0.479	0.000	cla1/a1/g1/g2/g7/out401 (cla1/a1/g1/g
MUXF5:I1->O	3	0.314	0.941	cla1/a1/g1/g2/g7/out40_f5 (cla1/a1/c1
LUT4:I1->O	2	0.479	0.804	cla1/a1/g2/g5/out11 (N21)
LUT3:I2->O	2	0.479	0.768	cla1/a1/g2/g6/out1 (N24)
LUT4:I3->O	6	0.479	1.023	cla1/a1/g2/g7/out1 (cla1/a1/c2)
LUT4:I1->O	1	0.479	0.704	cla1/a1/g3/g6/out138 (cla1/a1/g3/g6/o
LUT4:I3->O	1	0.479	0.976	cla1/a1/g3/g6/out162_SW0 (N216)
LUT4:I0->O	1	0.479	0.740	cla1/a1/g3/g6/out162 (N23)
LUT4:I2->O	1	0.479	0.681	cla1/a1/g3/g6/out2 (product_15_OBUF)
OBUF:I->O		4.909		product_15_OBUF (product<15>)
Total		32.331ns (15.188ns logic, 17.143ns route)		

Table.3 Timing Report Of Conventional Booth Multiplier

Cell:in->out	fanout	Gate Delay	Net Delay	Logical Name (Net Name)
IBUF:I->O	23	0.715	1.741	b_3_IBUF (b_3_IBUF)
LUT3:I0->O	7	0.479	1.201	m12/Mrom_ain_rom000011 (m12/Mrom_ain_
LUT3:I0->O	1	0.479	0.000	be22/pji12 (be22/pji11)
MUXF5:I0->O	4	0.314	0.949	be22/pji1_f5 (p2<2>)
LUT4:I1->O	1	0.479	0.000	adr11/p1/k5/k1/g7/m4/c11 (adr11/p1/k5
MUXF5:I1->O	5	0.314	0.842	adr11/p1/k5/k1/g7/m4/c1_f5 (adr11/p1/
LUT4:I2->O	1	0.479	0.000	adr11/p1/k5/k2/g7/m4/c11 (adr11/p1/k5
MUXF5:I1->O	4	0.314	1.074	adr11/p1/k5/k2/g7/m4/c1_f5 (adr11/c1)
LUT4:I0->O	3	0.479	1.066	adr11/p2/k1/g7/m4/c1 (adr11/p2/c1)
LUT3:I0->O	4	0.479	0.838	adr11/p2/k2/g3/m4/c1 (sum1<10>)
LUT4:I2->O	2	0.479	1.040	cla1/p2/k2/p1/carry1 (cla1/p2/k2/c1)
LUT4:I0->O	1	0.479	0.851	cla1/p2/k2/p2/r1/w91 (cla1/p2/k2/cv)
LUT4:I1->O	5	0.479	1.078	cla1/p2/k2/g7/m4/c1 (cla1/c2)
LUT4:I0->O	1	0.479	0.000	cla1/p3/k1/g7/m4/c1_G (N97)
MUXF5:I1->O	2	0.314	0.804	cla1/p3/k1/g7/m4/c1 (cla1/p3/c1)
LUT4:I2->O	1	0.479	0.740	cla1/p3/k2/g4/m4/c1_SW0 (N70)
LUT4:I2->O	1	0.479	0.681	cla1/p3/k2/g4/m4/c1 (product_15_OBUF)
OBUF:I->O		4.909		product_15_OBUF (product<15>)
Total		25.534ns (12.628ns logic, 12.906ns route) (49.5% logic, 50.5% route)		

Table.4 Timing Report Of Proposed Booth Multiplier

In comparision of Table.3 with Table.4 we can say that the propagation delay is reduced by 8ns in Proposed Booth multiplier, Hence it will be more faster than the conventional Booth multiplier.

VI CONCLUSION

Optical Computing is an rising technology to implement reversible logic. We have Proposed a new overall design approach to achieve optical reversible logic circuits using SOA based MZI switches. Optical reversible carry select adder with AOI logic has been proposed which is implemented in 8-bit booth multiplier. Implementation results shows that the proposed Booth multiplier will be more faster because Area and propogation delay are reduced.

REFERENCES

[1] Moore, Gordon. "The Future of Integrated Electronics." Fairchild Semiconductor internal publication, 1964.

[2] R. Landauer, ―Irreversibility and heat generation in the computing process‖, IBM Journal of Research and Development, pp. 183–191, July 1961.

[3] C. H. Bennet, ―Logical Reversibility of Computation‖, IBM Journal of Research and Development, vol. 17, no. 6, pp. 525-532, 1973.

[4]C. Taraphdara, T. Chattopadhyay, and J. Roy, ―Mach-zehnder interferometer-based all-optical

reversible logic gate‖, Optics and Laser Technology, vol. 42, no. 2, pp. 249–259, 2010.

[5] G. K. Maity, S. P. Maity, T. Chattopadhyay and J. N. Roy, "MachZehnder Interferometer Based AllOptical Fredkin Gate", International Conference on Trends in Optics and Photonics March 1 – 4, 2009 Kolkata, India Department of Applied Optics and Photonics University of Calcutta, Kolkata, India. Page 314

[6] G. K. Maity, J. N. Roy, and S. P. Maity, ―Machzehnder interferometer based all-optical peres gate‖, in Advances in Computing and Communications, ser. Communications in Computer and Information Science, A. Abraham, J. L. Mauri, J. F. Buford, J. Suzuki, and S. M. Thampi, Eds. Springer Berlin Heidelberg, 2011, vol. 192, pp. 249–258.

[7] G. K. Maity, T. Chattopadhyay, J. N. Roy, and S.P. Maity, "All-optical reversible multiplexer", Computers and Devices for Communication, 2009. CODEC 2009. 4th International Conference on , vol., no., pp.1,3, 14- 16 Dec. 2009.

[8] S. Kotiyal, H. Thapliyal, and N. Ranganathan, ―Mach-zehnder interferometer based design of all optical reversible binary adder‖, in Design, Automation Test in Europe Conference Exhibition (DATE),2012, pp. 721 –726, March 2012.

[9] S. Kotiyal, H. Thapliyal, and N. Ranganathan, "Mach-Zehnder Interferometer Based All Optical Reversible NOR Gates", VLSI (ISVLSI), 2012 IEEE Computer Society Annual Symposium on , vol.,no., pp.207,212, 19-21 Aug. 2012.

[10] G. K. Maity, J. N. Roy, and S.P. Maity, "Design of all-optical new gate using Mach-Zehnder interferometer", Devices, Circuits and Systems (ICDCS), 2012 International Conference on , vol., no., pp.474,478, 15- 16 March 2012.

[11] G. K. Maity and S.P. Maity, "Implementation of HNG using MZI", Computing Communication & Networking Technologies (ICCCNT), 2012 Third International Conference on , vol., no., pp.1,6, 26-28 July2012.

[12] Mehdi Saeedi and Igor L. Markov, ―Synthesis and Optimization of Reversible Circuits – A Survey‖, arXiv: 1110.2574v2 [cs.ET], 20 Mar 2013, pp. 1-34.

[13] R. Feynman, ―Quantum mechanical computers‖, Optical News, vol. 11, pp. 11-20 1985.

[14] T. Toffoli, ―Reversible computing‖, In Automata, Languages and Programming, Springer Verlag, pp. 632-644, 1980.