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Improved Design of D Flip Flop for Low Power Applications

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***Abstract* - An Implicit Pulse Triggered D flip flop is designed, which incorporates gated clocking. Clock gating using XOR gate inhibits redundant internal node switching. The pull-up network (PUN) control technique is used to conditionally strengthen the discharge path. This work aims at further reduction in power consumption using substrate bias technique to reduce leakage power which is referred to as Back Gate Forward/Reverse Bias method. Cadence Virtuoso 180nm technology is used to implement various pre & post layout simulations. From the results, it can be inferred that the proposed design reduces the power consumption by 41.82% at 10% data switching activity as compared with the existing counterparts. A comparison of three bit counter designed using conventional transmission gate (TG) based master-slave flip-flop and the proposed implicit pulse triggered flip flop shows a reduction of 23.90% in average power consumption.**

I.INTRODUCTION

TECHNOLOGY is moving from low scale integration (Intel 4004 a 4-bit CPU with 2300 transistors) to VLSI and ultra large scale integration (Intel i7 processor with 774 million transistors). Operating frequency has changed from megahertz (MHz) to gigahertz (GHz) [5] in order to meet the processing speed requirements. Pipelining technique is used to achieve high speed in modern synchronous digital systems. Flip flop rich modules like register files and shift registers are incorporated. Advent of SoCs and SIPs lead to development of different portable devices like mobile phones, tablet PC and wearable information or healthcare equipment. These devices which are battery operated directly maps to the need for low power consumption. This need has changed the VLSI digital design methodologies from speed oriented perspective to low power design approach [12].

The design of the clocking subsystem is vital in digital CMOS VLSI circuits, as it strongly affects not only the chip performance, but also its overall energy consumption. It accounts for 30%-60% of the total power dissipation in a system. Any clocking subsystem can be subdivided into three main parts: the clock generation unit, the circuits associated with clock distribution and the clocked storage elements (latches or flip-flops). Flip-flops introduce a timing overhead that is a significant fraction of the clock cycle. In a digital system flip-flops consume 30% to 50% of the total energy requirement [11]. It is crucial to keep this energy within reasonable bounds, since it reduces the energy available for computation under a given energy budget, and hence it limits the overall performance in power-limited systems. The above performance and energy issues, together with the need for adequate robustness and ability to deal with clock uncertainties like clock skew, clock jitter, make the flip-flops design quite tricky [11].

Different flip-flop architectures are used based on the application demand. Pulse triggered flip-flop is one such design which consists of a pulse generating stage and a data latching stage. Pulse triggered flip flop designs have zero or negative setup time in contrast to hard edge properties of TG based designs[10]. Master-slave designs have two data latching stages whereas pulse triggered flip-flops have single data latching stage [7]. Hence they are preferred over TG based designs in applications with power consumption as major constraint. Based on the method of pulse generation implicit and explicit pulse triggered flip flops are the two categories. In implicit configuration pulse generator controls only discharging path whereas in explicit designs pulse generator has to generate pulse externally and also control the discharging path [10]. The rest of paper is organized as follows. Section 2 includes survey on existing pulse triggered and advanced master-slave flip-flop designs. Working of the proposed implicit_FFs with clocking gating, pull up control and Back gate biasing technique in Section 3. Section 4 involves comparison of simulation results of proposed designs and counterparts. Section 5 provides the conclusion.

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II. REVIEW OF EXISTING DESIGNS

In this section existing pulse triggered FFs and advanced master-slave FFs designs are reviewed.

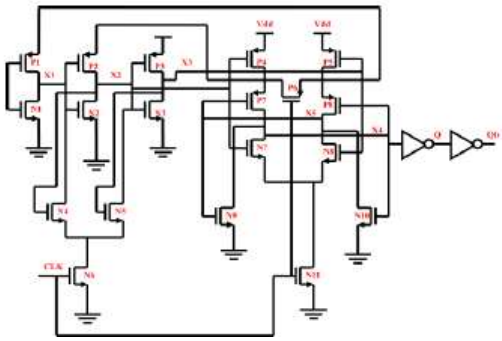

Figure 1 Topologically Compressed Flip-Flop (TCFF)

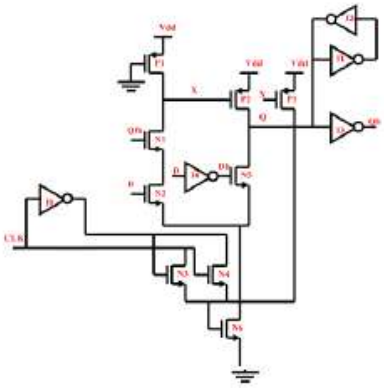

Figure 2 Conditional Pulse Enhancement Flip-Flop (CPEFF)

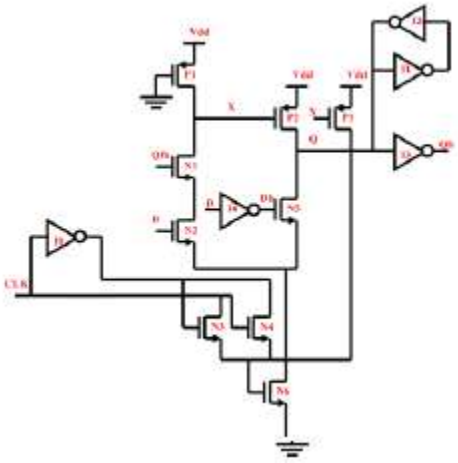

Figure 3 Contention Reduced Conditional Pulse Enhancement Flip-Flop (CRCPEFF)

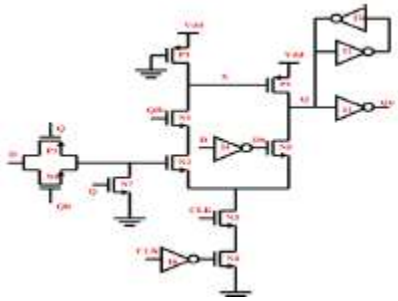

Figure 4 Clock Pair Shared Flip-Flop with Conditional Data Mapper (CPSFF)

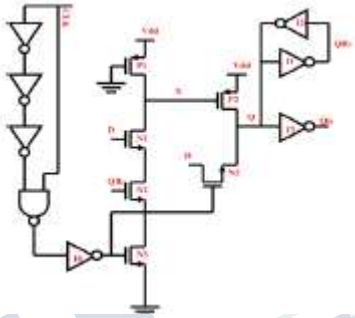

Figure 5 Explicit Pulse Triggered Flip-Flop with Signal Feed through Scheme

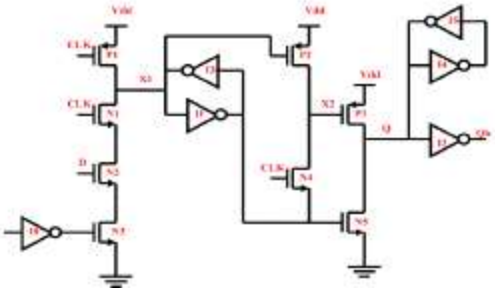

Figure 6 Dual Dynamic Node Flip-Flop

Fig 1 shows topologically compressed flip flop (TCFF) [7]. In this design clocked transmission gates are replaced by AND-OR gates with same inputs, at the transistor level pMOS and nMOS with same inputs are merged. This reduces the number of transistors clocked from 12 (in TGFF) to 3 thereby reduce dynamic power consumption. But major drawback of this design is that when clock signal is low any switching occurring at input node D will trigger unnecessary transition of intermediate nodes X2, X3.
Fig 2 is an implicit conditional pulse enhancement flip flop [4]. 2 nMOS transistors are used to realize 2 input AND gate which forms pulse generator stage. A weak pMOS transistor is used as keeper to conditionally

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strengthen discharge path for 0 to 1 transition of D input. 0 to 1 transition and 1 to 0 transitions are sampled and picked up by left branch and right branches of the data latching circuit respectively. Major drawback of this design is that, initially if Q=0, Qfb=1, 0_1 transition on D results in short circuit path from Vdd to Gnd. Also if the data gets sampled before transparency window it results in glitch at output node Q.

Fig 3 shows contention reduced conditional pulse triggered flip flop [6]. In this the Pseudo nMOS transistor of pull up network is replaced by a pair of parallel pMOS transistors with Q and Qfb as control signals. This isolates pull up and pull down network during evaluation phase (i.e. Clk=1). An additional nMOS transistor is added in the feedback loop with voltage at node X as control signal so as to overcome crossbar current flow while charging the output node Q.

Fig 4 shows clock pair shared flip flop design [9]. It uses a conditional data mapper which is combination of transmission gate and nMOS with Q and Qfb as control signals. This avoids unnecessary discharge of intermediate node X. However the problem of short circuit path from Vdd to Gnd when Q=0, Qfb=1, D=0_1 during transparency window persists in this configuration as well.

Fig 5 shows an explicit pulse triggered flip flop with signal feed through technique [8]. In this the right branch (path sampling 1_0 transition of D input) is replaced by an nMOS pass transistor which in turn serves as discharging path. Also as input D is connected to output node Q, controlled by clock. Any change in D is reflected at Q when clock is high, hence the name signal feed through technique.

Fig 6 shows dual dynamic node flip flop design [5]. Redundant data transitions and large pre-charge capacitance are the major sources of power dissipation in semi-dynamic flip flop designs. Single intermediate node drives both pull-up and pull-down transistors of output stage (larger capacitance) in conventional flip flops. D flip flop structure is modified to possess two pre-charge nodes of which one is pseudo dynamic and the other one is dynamic. Thereby reducing the load capacitance and hence the dynamic power.

III. PROPOSED IMPLICIT PULSE TRIGGERED FLIP-FLOP

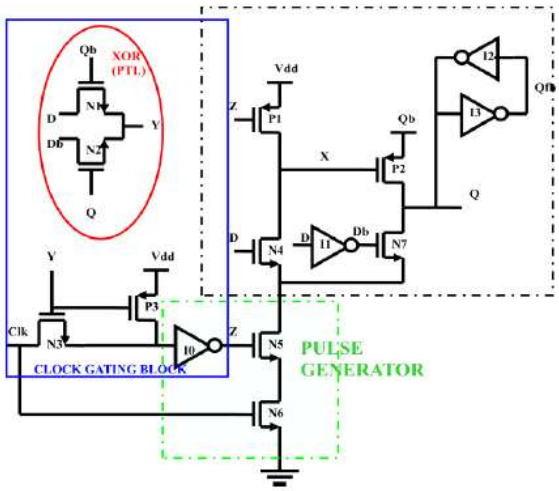

Figure 7 Implicit Pulse Triggered Flip Flop with Clock Gating, Conditional Pull-Up Control techniques

It consists of pass transistor based XOR gate which acts like a comparator. Input D and its compliment Db are fed as inputs with Qfb and Q as control signals as shown in Fig 7.XOR gate along with N3, P3 transistors forms clock gating logic. If the input D stays stable for successive clock cycle (say D=0; Db=1; hence Q=0; Qfb=1) Y will be logic 0.Logic 0 on Y turns off N3 transistor thereby blocking Clock signal. At the same time P3 is enabled which results in logic 0 at node Z turning off N1 (i.e. discharging path is shutoff).Whereas if D input makes transition then Y will be logic high and clock signal is allowed to propagate. For a short duration equal to the delay generated by inverter at node Z both N1, N2 will be on. The transition on input will be captured by discharge of X node if (0-1) else it will be captured by discharging of node Q (i.e. 1-0).Pre-charge pMOS will be turned off when Z node goes logic high (which happens only during the transparency period) this prevents contention between pull-up and pulldown networks. However this design has a drawback of threshold voltage drop because of PTL. This design is operated with variable data activities at 50MHz clock frequency, 1.8V as power supply voltage. Further the power supply voltage is scaled down from 1.8V to 1.3V, aspect ratios of transistors are modified. As the power supply voltage is scaled down in order to avoid degradation in D-Q delay the threshold voltage should also be scaled down.

$VT = VT0 \pm \gamma(\sqrt{|-2\varphi F + Vb|} - \sqrt{2|\varphi F|})$

Threshold voltage is governed by the above equation.$VT0$ is the threshold voltage when there is no

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body biasing. Down scaling of threshold voltage leads to increase in leakage currents. Substrate biasing technique is used in which the substrate of both pMOS and nMOS are either forward biased or reverse biased with respect to the source terminal ($VBS \neq 0$). As shown in Fig 8 Nb and Pb are bias voltages (0.1V to 0.4V) applied to MOS transistors. This reduces leakage current which in turn reduces power consumption.

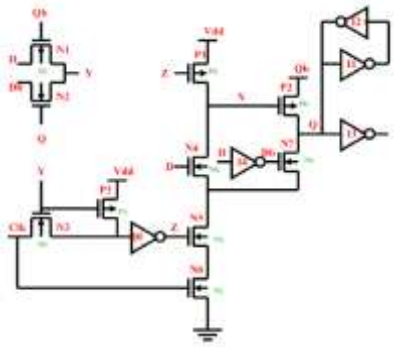

Figure 8 Implicit Pulse Triggered Flip Flop with Clock Gating, Conditional

Pull-Up Control and Back Gate reverse bias techniques

IV. SIMULATION RESULTS

All the designs are realized using Cadence Virtuoso tool with 180nm CMOS technology as implementation platform, Spectre simulator is used for simulation of the same. Design Rule Check (DRC), Layout versus Schematic (LVS) for the layouts drawn are performed by using Assura.

Power Supply Voltage (volts)	Clock signal (vpulse source)	Input (D) signal (vbit source)
V_{dd}=1.8V	tr=tf=1ns; period=20ns	tr=tf=100ps;
V_{ss}=0V	pulse width=10ns;	pulse width=10ns;
no substrate bias	V_1=1.8V; V_2=0V;	V_1=1.8V; V_2=0V;

Table 1 Simulation setup for flip-flop designs

Above table shows the simulation setup for various flip-flop designs

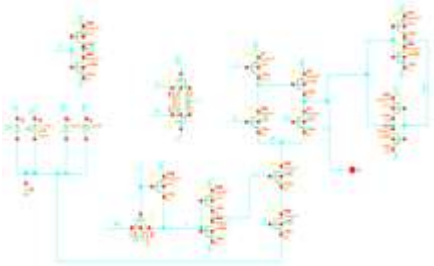

Figure 9 Implicit Pulse Triggered Flip Flop with Clock Gating and Pull-Up Control

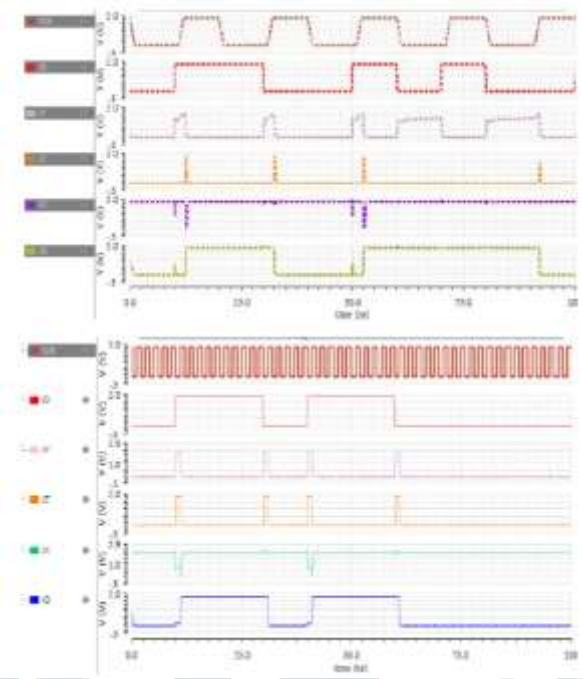

Figure 10 Simulation waveforms of IPFF_CGPC at 50MHz and 1GHz

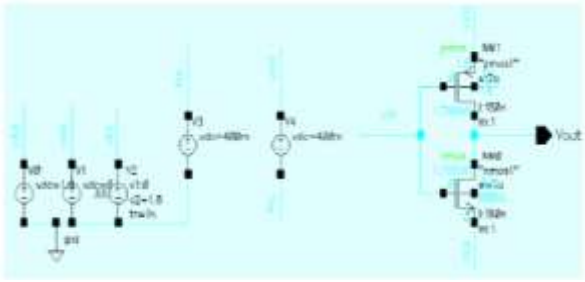

Figure 11 Back Gate substrate bias technique applied to CMOS inverter

Back Gate/body bias technique is applied to CMOS inverter. Variation of threshold of both pMOS and nMOS with respect to bias voltage are tabulated in the table below.

Vbs (V)	nMOS-Vth(mV)	pMOS-Vth(mV)
0	542.632	-516.801
.1	514.97	-483.643
.2	491.435	-453.799
.3	470.947	-430.154
.4	452.109	-410.768

Table 2 Variation of threshold voltages of pMOS and nMOS

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Flip Flop	D=0	D=1	D=10%	D=20%	D=50%	D=100%
TCFF	15.15µw	12.2 µw	15.66 µw 11.53 µw	20.02 µw 23.03 µw	31.52 µw 27.3 µw	43.1 µw 47.21 µw
CPEFF	7.859 µw	12.29 µw	18.09 µw 19.08 µw	29.39 µw 25.29 µw	35.27 µw 36.89 µw	54.66 µw 53.67 µw
CR_CPEFF	21.3 µw	22.66 µw	29.97 µw 27.25 µw	36.19 µw 35.57 µw	44.5 µw 41.76 µw	56.27 µw 59.02 µw
CPSFF	9.224 µw	11.35 µw	15.64 µw 16.48 µw	22.8 µw 20.69 µw	27.03 µw 27.87 µw	39.32 µw 38.44 µw
Ex-SFT_PFF	52.13 µw	48.38 µw	49.01 µw 51.99 µw	56.63 µw 52.41 µw	57.08 µw 59.89 µw	67.7 µw 65.3 µw
DDFF	28.49 µw	116.9 µw	124.5 µw 29.94 µw	105.2 µw 50.58 µw	103.2 µw 43.12 µw	67.2 µw 83.21 µw
IPFF_CGPC	2.49 µw	1.05 µw	5.999 µw 4.848 µw	8.329 µw 9.867 µw	13.37 µw 12.21 µw	19.58 µw 20.73 µw
IPFF_ECGPC	1.238 µw	1.057 µw	11.39 µw 4.85 µw	15.01 µw 15.17 µw	25.31 µw 18.77 µw	32.32 µw 39.17 µw
IPFF_CGPC_BB	1.748µw	807.6µw	5.461 µw 4.227 µw	7.949 µw 8.951 µw	12.7 µw 11.46 µw	18.37 µw 19.93 µw

Table 3 Average Power Consumption of various flip-flops

Flip Flop	#of transistors	Delay (ns)
TCFF	23	1.677
CPEFF	19	1.53
CR_CPEFF	19	1.51
CPSFF	21	1.58
Ex-SFT_PFF	24	1.63
DDFF	20	1.603
IPFF-CGPC	20	1.489
IPFF-ECGPC	22	1.494
IPFF-CGPC-BB	20	1.55

Table 4 D_Q delay of various flip-flops

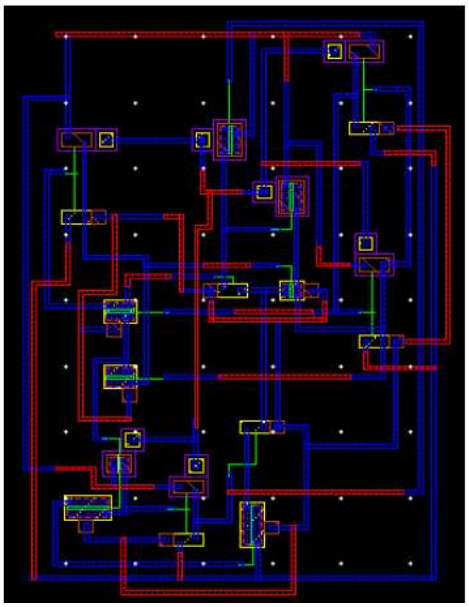

Figure 12 Layout view of the IPFF_CGPC with substrate bias technique

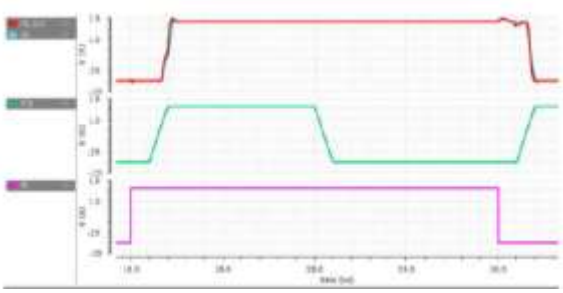

Figure 13 Simulation waveforms of both schematic and layout after RC extraction of the IPFF_CGPC with substrate bias technique

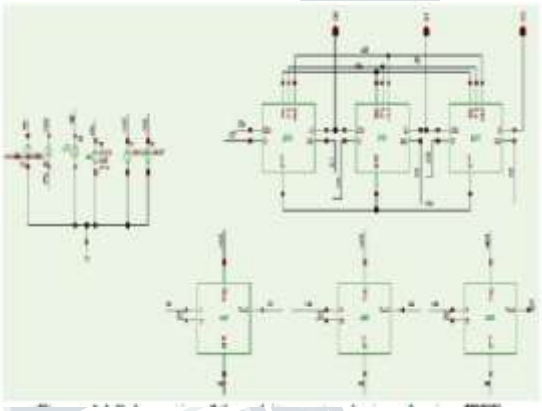

Figure 14 Schematic of three bit counter designed using IPFF

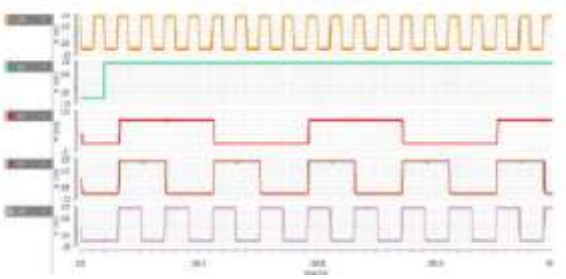

Figure 15 Simulation waveforms of three bit counter

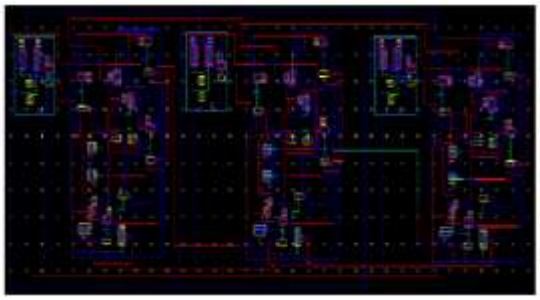

Figure 16 Layout view of three bit counter using IPFF

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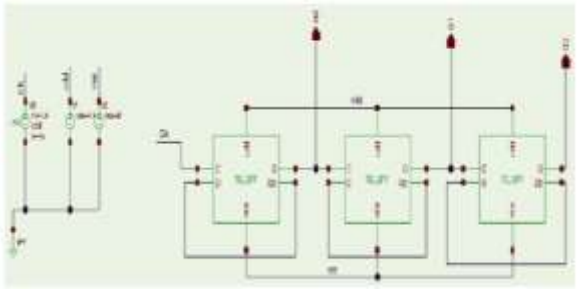

Figure 17 Schematic of three bit counter designed using TGFF

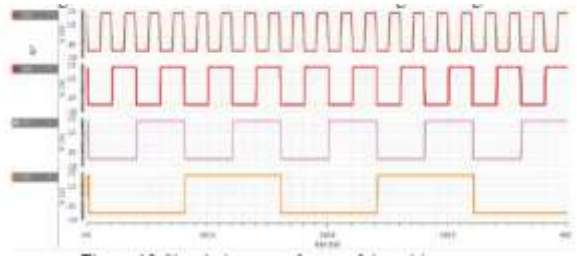

Figure 18 Simulation waveforms of three bit counter

Counter	Vdd(V)	Power (µw)
IPFF with body bias	1.4	18.75
IPFF with no body bias	1.4	32.43
TGFF	1.4	24.64

Table 5 Tabulation of average power consumed by counter design

V. CONCLUSION AND FUTURE SCOPE

The objective to design and implement a D flip flop with low power as desirable characteristics achieved by using pulse triggering approach in contrast to the conventional master slave approach. Incorporating low power techniques like conditional pre-charge, and clock gating forms a better alternative to the existing master-slave D flip flops. It is seen from the simulation results that at 10% data activity a power reduction of up to 41.82%is achieved. Even though the proposed design consumes lesser power compared to the master-slave type D flip flop, circuit operating conditions are still in the super-threshold (i.e. the gate input voltage VGS is greater than threshold-voltageVTH). In order to further reduce power consumption sub-threshold design (in which VGS is lesser thanVTH) can be an optimal method. As conduction in sub threshold is because of leakage current care should be taken which otherwise will lead to degradation of speed.

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