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Implementation of SVPWM estimation technique for three phase VSI

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***Abstract* - In most of the applications to get the variable voltage and frequency for AC drives is obtained from Voltage Source Inverter. This paper exhibits the estimation of a space vector PWM (SVPWM) utilizing MATLAB/Simulink and ModelSim tools. Both the programs work in co-simulation mode provided by the Link- for-ModelSim toolbox in the Simulink. The choice of a particular PWM depends on the permissible harmonic content in the output voltage waveform. The simulation results showed that the technique preserves the advantage of the SVPWM especially with regard to the reduction of THD.**

Index Terms— SVPWM; three phase VSI; MATLAB/simulink; Modelsim

I.INTRODUCTION

As a result of advancement in solid state power electronic devices, switching power converters are used to a greater extent in modern motor drives to convert and distribute the required energy to the motor. Voltage source inverters are used in a lot of industrial applications such as UPS, frequency converters, motor drive. The crucial function of VSI is to synthesize AC output voltage and frequency from a constant DC voltage as a means of PWM technique. The main complications faced by the power electronic design engineers are about the reduction of harmonic content in inverter circuits. The choice of a particular PWM relies on the permissible harmonic content in the output voltage waveform, dc bus utilization and minimum switching losses. In recent years, there is an increase trend of utilizing SVPWM because of easy digital implementation and efficient utilization of DC bus voltage. [1] The SVPWM algorithm is the most complex, advanced PWM generation technique for three phase VSI in order to generate PWM gating signals for control of various AC motors, Because of its ability to generate inverter's wave output with variable amplitude for the same DC bus and its ability to reduce the harmonics and switching losses. This makes SVPWM the most widely accepted modulation technique. The comparative analysis between DSP's and FPGA based control capabilities in PWM converters in [10] concludes FPGA as a rival technology.With FPGA based implementation field programmable capability, flexible adjustment of dead time and switching frequency makes it suitable to drive various switching devices in practical application. In [5]author proposed a Universal SVM with dead time compensation and over modulation is not a flexible design and its switching frequency cannot be set arbitrarily. In [2] the authors implemented SVPWM and ANN-SVPWM. The mathematical complexity involved with SVPWM is reduced extremely but the design of an ANN is an iterative process, and based on the application and nonlinearity suspected it is selected the ANN structure. The author in [3] proposed a comparison between the implementation of SPWM and SVPWM modulation techniques for controlling a three-phase inverter to find the simplicity of the algorithm and compare the overall performance of both the techniques. Related to the area of control and power electronics [6][8][13] demonstrate how the researchers are working on reconstructing PWM techniques. In this article, a new SVPWM estimation technique is proposed which shows the approximate reduction in total harmonic distortion. The SVPWM generated gating signal waveforms is given to the three phase VSI. This work focuses on design of this block using HDL (VHDL/verilog) so, that the software control can be transferred to FPGA kit. The HDL block models are estimated using co-simulation with Modelsim and simulink/MATLAB. The inverter is modeled using Simulink. The rest of the paper is organized as follows: section 2 discusses the theory of generation of SVPWM, section 3 shows the simulation results of SVPWM pulses generated and output voltages of inverter, section 4 ends with conclusion.

II . GENERATION OF SVPWM

A. Voltage source inverter :

The three phase output voltage can be acquired from combination of six transistors i.e, VSI. The circuit model of a typical three phase VSI is as shown in the

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Figure 1. There are six power switches (S1-S6) that shape the output. There is assumption that the switching of these switches are in a complementary way. Since there are three leg, total 8 switching vectors are possible (V0-V7). Six out of these 8 vectors produce Non-zero switching voltage i.e, Non-zero switching states. The remaining 2 vectors produce zero output voltage i.e, zero switching states. Hence, the inverter output is composed of these eight switching states. Now, the Non-zero output voltage divide the space vector plane into 6 sized sectors of $60^0$with equal magnitude thus forming a origin centered hexagon, and the 2 zero vectors are at origin and the various possible switching vectors are as shown in Figure 2. The maximum boundary of space vector is hexagon. A Voltage reference (Vref) is provided in terms of a revolving space vector.

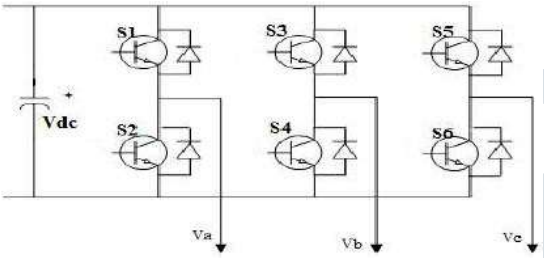

Figure 1 voltage source inverter

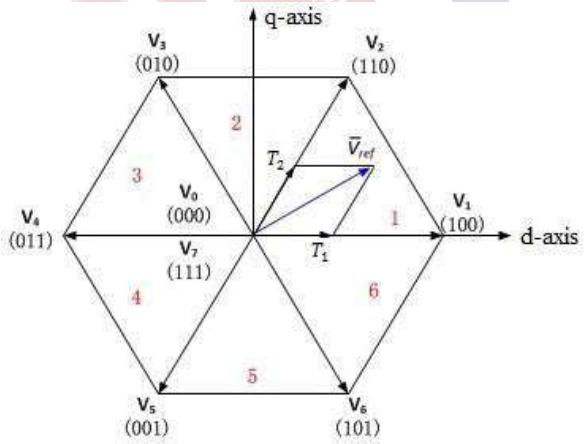

Figure 2 Switching sectors

B. Principle of SVPWM :

The space vector pulse width modulation is inherently a voltage control scheme, calculates the optimum switching pattern for the three phase inverter. The calculations are performed in a d-q /space vector plane.

Realization of SVPWM involves the following steps:

i. Co-ordinate transformation :

The three phase voltage equations in reference frame are transferred into the stationary d-q frame as shown in Figure 3. The relation between switching variable vector and phase voltage vector [Va Vb Vc] can be expressed as follows

$$V_d = V_{an} - V_{bn} \cdot \cos 60 - V_{cn} \cdot \cos 60 = V_{an} - \frac{1}{2}V_{bn} - \frac{1}{2}V_{cn}$$

$$V_q = 0 + V_{bn} \cdot \cos 30 - V_{cn} \cdot \cos 30 = V_{an} + \frac{\sqrt{3}}{2}V_{bn} - \frac{\sqrt{3}}{2}V_{cn}$$

$$\therefore \begin{bmatrix} V_d \\ V_q \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix}$$

$$\left|\overline{V}_{ref}\right| = \sqrt{V_d^{\,2} + V_q^{\,2}}$$

$$\alpha = \tan^{-1}\left(\frac{V_q}{V_d}\right) = \omega_s t = 2\pi\pi_s t$$

(where, f_s = fundamental frequency)

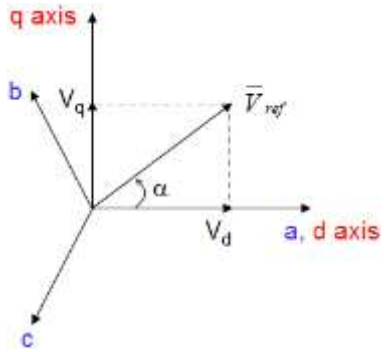

Figure 3 vectors in d-q reference

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ii. Determine time duration T1, T2, T0 :

Consider sector 1. The vector states V0, V1, and V2 are to be switched ON for time durations T0, T1 and T2, respectively. Hence, for the switching time durations at Sector 1,

$$\int_0^{T_z}\bar{V}_{ref}=\int_0^{T_1}\bar{V}_1 dt+\int_{T1}^{T_1+T_2}\bar{V}_2 dt+\int_{T_1+T_2}^{T_z}\bar{V}_0$$

$$\therefore T_z\cdot\bar{V}_{ref}=(T_1\cdot\bar{V}_1+T_2\cdot\bar{V}_2)$$

$$\Rightarrow T_z\cdot|\bar{V}_{ref}|\cdot\begin{bmatrix}\cos(\alpha)\\ \sin(\alpha)\end{bmatrix}=T_1\cdot\frac{2}{3}\cdot V_{dc}\cdot\begin{bmatrix}1\\ 0\end{bmatrix}+T_2\cdot\frac{2}{3}\cdot V_{dc}\cdot\begin{bmatrix}\cos(\pi/3)\\ \sin(\pi/3)\end{bmatrix}$$

(where, $0\le\alpha\le 60^{\circ}$)

$$\therefore T_1=T_z\cdot a\cdot\frac{\sin(\pi/3-\alpha)}{\sin(\pi/3)}$$

$$\therefore T_2=T_z\cdot a\cdot\frac{\sin(\alpha)}{\sin(\pi/3)}$$

$$\therefore T_0=T_z-(T_1+T_2),\quad\left(\text{where, } T_z=\frac{1}{f_s}\text{ and } a=\frac{|\bar{V}_{ref}|}{\frac{2}{3}V_{dc}}\right)$$

Similar calculations can be performed at any of the sectors to determine the suitable time combinations of vectors in any of the sectors

iii. Determine the switching time of each transistor (S1 to S6):

Depending upon the sector, the time duration for which each switch is ON is determined, as shown in table 1. This time corresponds to the gating pulses given to each of the six IGBT switches. The sequence maintained is such, that only one switch changes state (from OFF to ON or vice versa) at a time, therefore minimizing the switching losses.

Sector	Upper Switches (S_1, S_3, S_5)	Lower Switches (S_4, S_6, S_2)
1	$S_1=T_1+T_2+T_0/2$ $S_3=T_2+T_0/2$ $S_5=T_0/2$	$S_4=T_0/2$ $S_6=T_1+T_0/2$ $S_2=T_1+T_2+T_0/2$
2	$S_1=T_1+T_0/2$ $S_3=T_1+T_2+T_0/2$ $S_5=T_0/2$	$S_4=T_2+T_0/2$ $S_6=T_0/2$ $S_2=T_1+T_2+T_0/2$
3	$S_1=T_0/2$ $S_3=T_1+T_2+T_0/2$ $S_5=T_2+T_0/2$	$S_4=T_1+T_2+T_0/2$ $S_6=T_0/2$ $S_2=T_1+T_0/2$
4	$S_1=T_0/2$ $S_3=T_1+T_0/2$ $S_5=T_1+T_2+T_0/2$	$S_4=T_1+T_2+T_0/2$ $S_6=T_2+T_0/2$ $S_2=T_0/2$
5	$S_1=T_2+T_0/2$ $S_3=T_0/2$ $S_5=T_1+T_2+T_0/2$	$S_4=T_1+T_0/2$ $S_6=T_1+T_2+T_0/2$ $S_2=T_0/2$
6	$S_1=T_1+T_2+T_0/2$ $S_3=T_0/2$ $S_5=T_1+T_0/2$	$S_4=T_0/2$ $S_6=T_1+T_2+T_0/2$ $S_2=T_2+T_0/2$

Table 1 SWITCHING TIME CALCULATION FOR EACH SECTOR

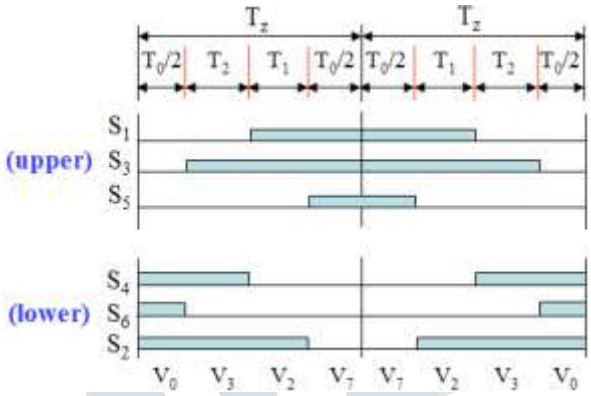

Figure 4 switching pattern for sector 2

Table 2 Output voltages of three phase inverter

Voltage Vectors	Switching Vectors			Line to neutral voltage			Line to line voltage		
	a	b	c	V_{an}	V_{bn}	V_{cn}	V_{ab}	V_{bc}	V_{ca}
V_0	0	0	0	0	0	0	0	0	0
V_1	1	0	0	2/3	-1/3	-1/3	1	0	-1
V_2	1	1	0	1/3	1/3	-2/3	0	1	-1
V_3	0	1	0	-1/3	2/3	-1/3	-1	1	0
V_4	0	1	1	-2/3	1/3	1/3	-1	0	1
V_5	0	0	1	-1/3	-1/3	2/3	0	-1	1
V_6	1	0	1	1/3	-2/3	1/3	1	-1	0
V_7	1	1	1	0	0	0	0	0	0

III SVPWM ESTIMATION

In this section the estimation of the SVPWM algorithm is presented. In this work direct polynomial relations have been developed between each reference voltage and conduction time period within the converter's arms.

The conduction time duration can be obtained by the three first order polynomials (Va, Vb, Vc) and the one third order polynomials (Vdc).

$$Ton_{a,b,c}=A(V_{dc})V_{a,b,c}+k$$

Here, polynomial A is a function of DC bus voltage. A is constant if Vdc is constant and k is a constant. A is acquired to minimize the harmonic distortion by varying the dc bus voltage A(Vdc) interpolation graph

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is as shown in the figure 5. A(Vdc) is a polynomial of order 3 given by the following equation.

$$A = a * V_{dc}^3 + b * V_{dc}^2 + c * V_{dc} + d$$

This equation can further optimally implemented by factorization.

$$A = \left((a * V_{dc} + b) * V_{dc} + c\right) * V_{dc} \cdot + \mathrm{d}$$

Hence, this estimation can consume six multipliers and six adders to calculate six switching times of switches.

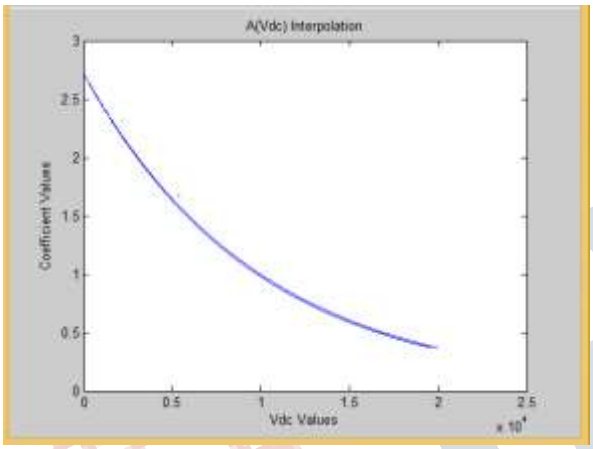

Figure 5 A(vdc) interpolation

IV SIMULATION RESULTS

In this work, the effectiveness of the proposed technique is proven by various simulation results. SVPWM algorithm is described in HDL performing all the SVPWM calculation: coordinate transformation, sector determination, switching time calculations, and switching signal generation. The three phase VSI has been described using Simulink. Implementation is done with a word length equal to 8 bits. The MATLAB allows performing the dynamics of system while the ModelSim runs a program written in HDL Figure 5 shows the SVPWM generated signals using ModelSim for sector 2 which is as expected with respect to theoretical result as shown in Figure 4. Figure 6 shows the line and phase voltages of three phase inverter. Figure 7 shows the harmonic's spectrum of the inverter output voltages. Table 3 and 4 shows the tabulation of THD for line and phase voltages. In practice, filters are added to filter the harmonics.

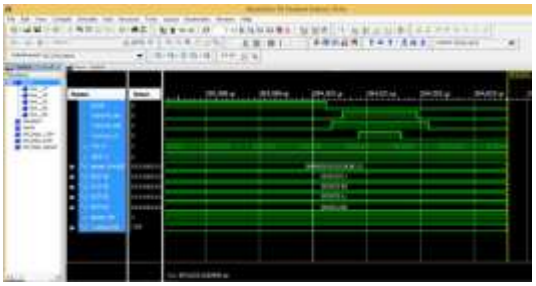

Figure 6 SVPWM for sector 1

Figure 7 line voltage of inverter

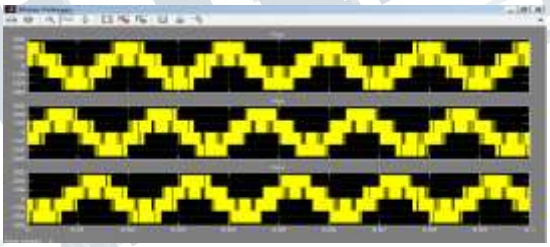

Figure 8 phase voltage of inverter

Table 3 THD for phase voltages

Phase voltages	Fundamental(50hz)	THD(%)
Van	229.9	52.75
Vbn	229.8	52.68
Vcn	230	52.67

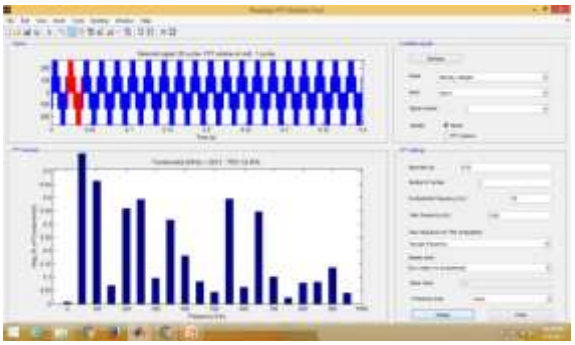

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Figure 9 Harmonic spectrum of phase voltage (Phase A)

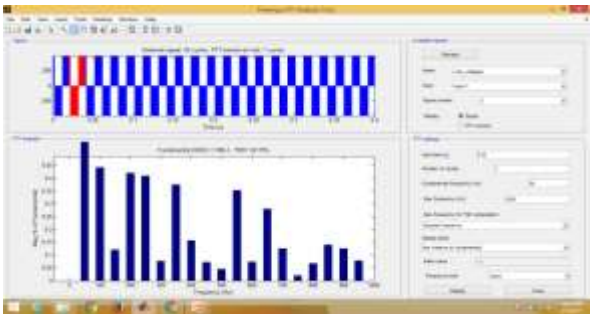

Figure 10 Harmonic spectrum of line voltage (Phase A)

Table 4 TDH for line voltages

line voltages	Fundamental(50hz)	THD(%)
Vab	398.1	52.75
Vbc	398.4	51.60
Vca	398.0	50.33

V CONCLUSION

This paper presents the realization of a SVPWM using HDL. The verification of algorithm is performed using co-simulation between ModelSim and Simulink. Simulation is a mandatory step in the design process of a power converter. This work presents the simulation of a DC-AC converter. The simulation result preserves the advantage of SVPWM especially with regard to the reduction of THD. The synthesis results would show that this new technique consumes few resources during implementation leaving enough resources for control loops implementation.
Future work includes extending the estimation technique to multilevel inverter as, the number of voltage level reaches infinity, the output total harmonic distortion approaches to 0.

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