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Design and Implementation of 12-T SRAM Cell in 32nm FinFET Technology

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Abstract:- **The primary downside of utilizing CMOS transistors is high power utilization and high leakage current. FinFET has turned into the most encouraging substitute for CMOS which has less short channel effects compared to CMOS technology. In low power applications, as the technology is scaling down leakage current and leakage power are the most noticeable problems for SRAM cell. The interest for static random access memory (SRAM) is expanding with extensive utilization of SRAM in System On-Chip and VLSI circuits. In order to design low power devices leakage current and power dissipation must be kept low. To reduce this dissipation conventional 12T SRAM is implemented using FinFET technology. In this paper power consumption during hold, read and write operations of CMOS 12T SRAM cell with FinFET based 12T SRAM cell are compared with the help of HSPICE simulator.**

Keywords**: FinFET, SRAM, HSPICE, BSIM-CMG Model, Power Dissipation.**

I. INTRODUCTION

The demand for battery operated high speed portable devices like notebook, laptop computers, personal digital assistants; cellular phones, etc. are increasing day by day. High speed portable devices require primary memory that responds faster. For that purpose, static random access memory (SRAM) is used, which is faster and refreshing is not needed. Static random access memory (SRAM) cell is preferred over dynamic random access memory (DRAM) due to its better performance property. But unlike DRAM, SRAM cell requires continuous supply voltage to retain the stored data and consumes more power. Further scaling for a transistor causes an unreasonable increase in the power consumption due to the enhanced gate leakage.

Dynamic power dissipation and leakage current are the main issues of high speed SRAM cells where leakage currents contribute to a large part of total power consumption. This unwanted power dissipation reduces the battery backup life of portable devices. So it is required to have a SRAM cell design, having both low static and dynamic power dissipations. Many techniques have been employed to fulfil these requirements such as supply voltage scaling, mutlithreshold CMOS etc. In this paper FinFET based 12T SRAM is implemented and compared with CMOS based 12T SRAM cell.

A. FINFET INTRODUCTION

FinFET devices show better suppression of the short channel effect, lower energy consumption, higher supply voltage scaling capability, and higher ON/OFF current ratio compared with the bulk CMOS. Even though current conduction is in the plane of the wafer, it is not strictly a planar device. Rather, it is referred to as a quasi-planar device, because its geometry in the vertical direction also affects device behaviour. The thickness of the fin (measured in the direction from source to drain) determines the effective channel length of the device. Amongst the DGFET (Double Gate FET) types, the FinFET is the easiest one to fabricate. Amongst multigate FETs, FinFETs have emerged as the best candidate structures from a fabrication perspective.

Most important Features of FinFET are:

(1) Ultra thin Si fin for suppression of short channel effects.

(2) Raised source/drain to reduce parasitic resistance.

(3) Improve current drive.

(4) Symmetric gates yield great performance, but can built asymmetric gates that target VT.

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(5) FinFETs are designed to use multiple fins to achieve larger channel widths.

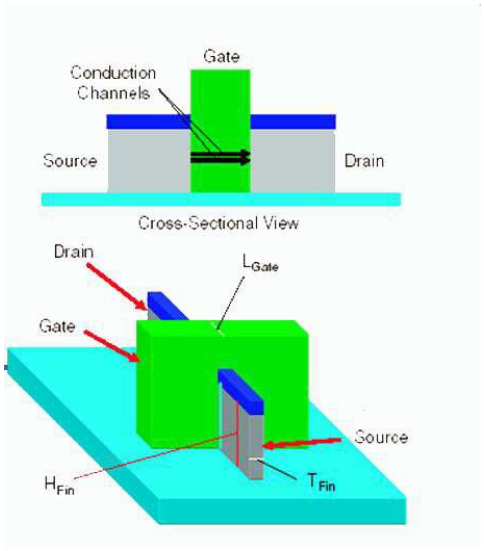

Fig.1: Structure of FinFET

II. EXISTING CMOS BASED 12-T SRAM CELL

This section introduces the existing 12T SRAM design and its operation. Fig.2 shows the schematic of the existing CMOS based 12T SRAM cell [1], [3], [4].

To control SRAM cell mainly three signals are used i.e. word line (WL), bit line (BT), bit line bar (BB) and read write bar (RD WRB). The nodes XT and XB are monitored in read, write and hold operations. In read operation bit lines (BT) and (BB) are pre-charged to logic '1' and word line (WL) and RD WRB signal is activated.

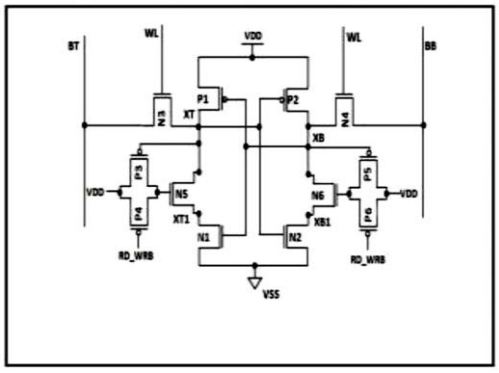

Fig.2: Schematic of CMOS based 12-T SRAM cell

In Read '1' operation BT remains at logic '1' as the corresponding storage node XT is storing logic '1' and transistors P3, P4 are off, hence transistor N5 is also in the 'off' state. When XT='1' then XB is at logic '0' so transistor N6 will be on as transistor P5 is in the 'on' state. The bit line BB discharges through N4, N6 and N2 and the potential difference developed between BT and BB is sensed through the sense amplifier. In read '0' operation, XT= '0' and XB='1' so transistor N5 will be in the 'on' state as P3 is on; so bit line BT discharges through N3 , N5 and N I . Thus, the developed potential difference between BT and BB is sensed through the sense amplifier. In write operation word line (WL) is activated and the RD WRB signal is deactivated. The write '0' operation is performed by pulling down bit line (BT) to logic ' 0 ' and pulling up the bit line bar (BB) to logic ' 1 ' . N5 and N6 transistors are ON, as the RD WRB signal is low and it acts as 6T SRAM cell. The node XT starts discharging and P2 turns on, the voltage at node XB will raise and logic ' 0 ' is written. In write ' 1 ' operation, the bit line (BB) is pulled down to logic ' 0 ' and the bit line (BT) is kept at logic '1'. Node XB is discharged and P1 transistor turns ON and the voltage at node XT starts to rise, hence logic ' 1 ' is written into the cell. In hold mode both the word lines WL as well as read write signal (RD WRB) are deactivated.

III. FINFET BASED 12-T SRAM CELL

This section introduces the proposed 12T SRAM design and its operation is as mentioned in above section. Fig.3 shows the schematic of the proposed 12T SRAM cell.

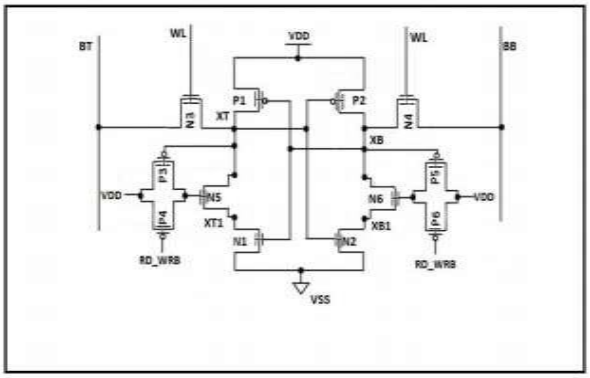

Fig.3: Schematic of FinFET based 12-T SRAM cell

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TABLE I
VOLTAGES FOR DIFFERENT STATES

States	Word Line(V)	Bit Line(V)	Bit Line Bar(V)
Hold	0	0	0
Write'1	1	1	0
Write'0'	1	0	1
Read'0'	1	0.6	0.6
Read'1'	1	0.6	0.6

IV. SIMULATION RESULTS

To Simulation has been done by Synopsys HSPICE using 32nm BSIM-CMG FinFET model. The model files are available as open source from Predictive technology model (PTM and BSIMCMG) for CMOS and FinFET. The simulation is conducted at room temperature. The power consumption is measured by multiplying the supply voltage to the average current flowing out from the VDD terminal when there is no input and output signal transition.

The power dissipation is given as

$P_{LEAK} = V_{DD} \times AVERAGE\ (I(V_{DD}))$

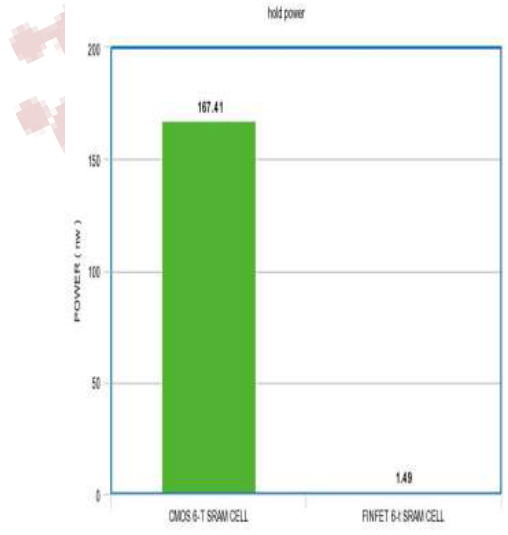

Fig.4: Comparison of Hold Power 6-T SRAM cell

Figure 4, 5 and 6 illustrates the comparison of hold power, read power and Write power respectively of CMOS based 6T SRAM cell and FinFET based 6T SRAM cell. Figure 7, 8 and 9 illustrates the comparison of hold power, read power and Write power respectively of CMOS based 12T SRAM cell and FinFET based 12T SRAM cell.

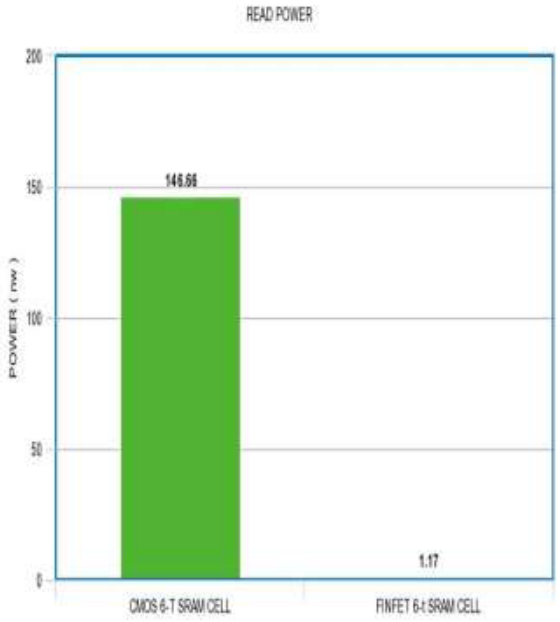

Fig.5: Comparison of Read Power 6-T SRAM cell

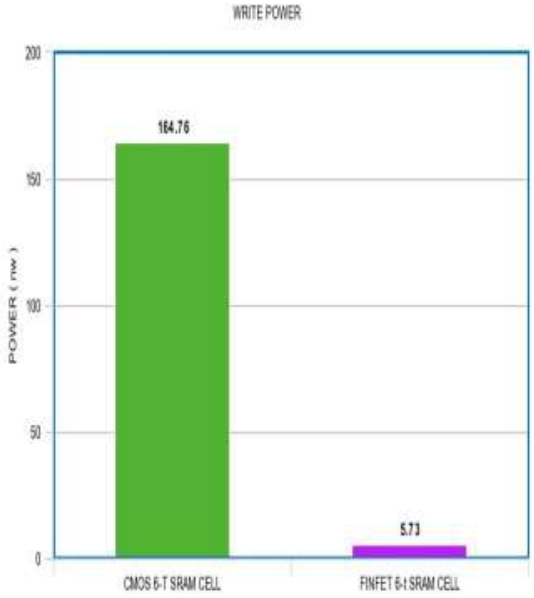

Fig.6: Comparison of Write Power 6-T SRAM cell

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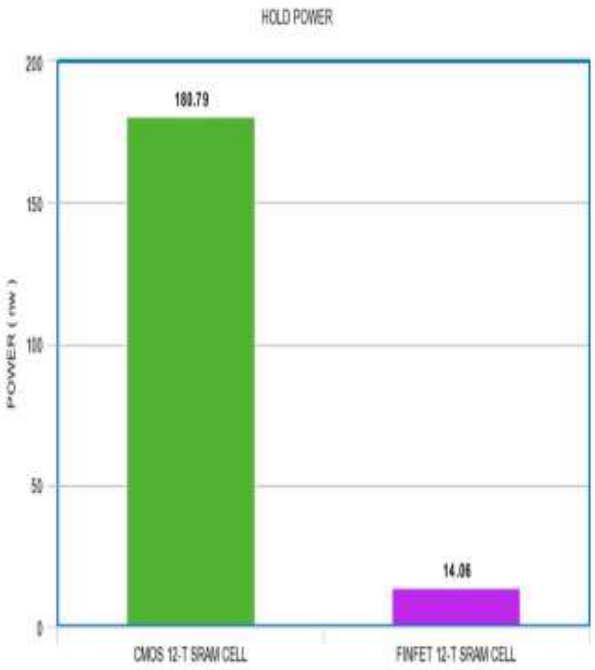

Fig.7: Comparison of Hold Power 12-T SRAM cell

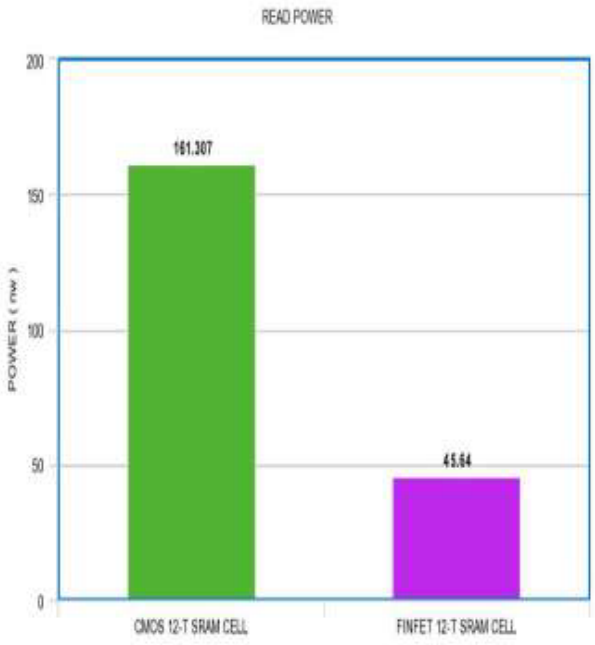

Fig.8: Comparison of Read Power 12-T SRAM cell

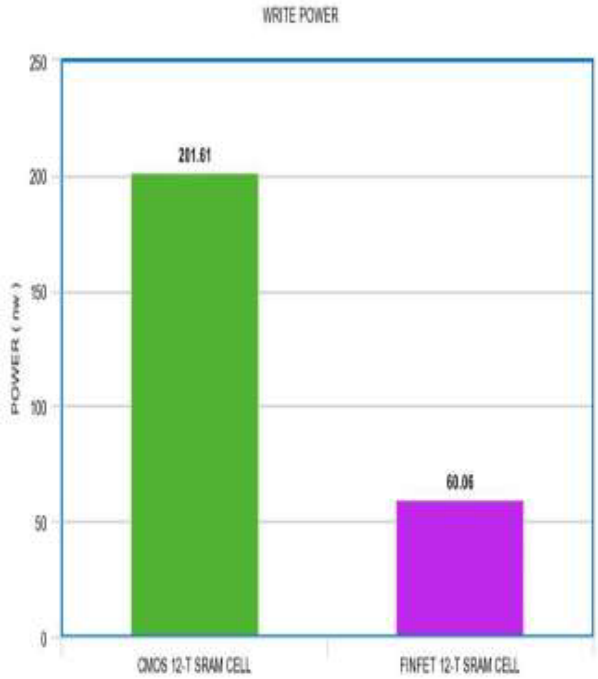

Fig.9: Comparison of Write Power 12-T SRAM cell

TABLE III
AVERAGE POWER

TECHNOLOGY (32nm)	HOLD POWER (nw)	READ POWER (nw)	WRITE POWER (nw)
6-T CMOS SRAM CELL	167.41	164.66	164.76
6-T FINFET SRAM CELL	1.49	1.17	5.73
12-T CMOS SRAM CELL	180.79	161.30	201.61
12-T FINFET SRAM CELL	14.06	45.64	60.06

V. CONCLUSION

A FinFET based 6T and 12T SRAM cell has been developed in Synopsys HSPICE simulator using BSIM-CMG models. The cell performance has been compared with existing CMOS based 6T and 12T SRAM cell. The simulation results show that there is reduction in power dissipation in FinFET based SRAM cell compared with CMOS based SRAM cell.

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