ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
Vol 5, Issue 1, January 2018

Digital Design and Implementation of 8-Bit Carry Bypass & Carry Increment Adder using Xilinx & Cadance Tool

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Abstract: **- In Digital Integrated Circuits, Adders are the most widely used digital components for computing applications. In this paper 8-bit Carry Bypass Adder and Carry Increment Adder are implemented using Xilinx and CADANCE tool. The performance parameters such as area, delay and power distribution are discussed.**

Key words **Digital Signal Processor, Carry Bypass Adder, Carry Increment Adder, and Carry look ahead adder, Carry-select adder, Ripple-Carry Adder.**

I. INTRODUCTION

Arithmetic units are the essential blocks of digital systems such as Digital Signal Processor (DSP), micro processors, micro controllers, and other data processing units. Adders become a critical hardware unit for the efficient implementation of arithmetic unit. In many arithmetic applications and other kinds of applications, adders are not only in the arithmetic logic unit, but also in other parts of processor [1]. Adders are one of the most widely used digital components in the digital integrated circuit design and are the necessary part of Digital Signal Processing (DSP) applications. With the advances in technology, researchers have tried and are trying to design adders which offer either high speed, low power consumption, less area or the combination of them [1]. The adder is the fundamental block in any arithmetic unit, and is often the speed-limiting circuit in a digital system. Hence, many parallel adder architectures have been proposed to increase speed, with reasonable area and power dissipation features. One of the fastest and efficient architectures in terms of area and power dissipation is the Carry Bypass Adder (CBA) [2]. The standard Carry Increment Adder (CIA) consists of CLA's/CSA's and Incremental circuitry. The incremental circuit is designed using HA's in CLA / CSA chain with a sequential order. The addition operation is done by separating the total number of bits in to group of 4bits and addition operation is performed by several 4-bit CLA's / CSA's. Instead of computing two partial sums for each group and selecting the correct one, only one partial sum is calculated and incremented if necessary, according to the input carry. Thus the second adder and the multiplexers in the carry-select scheme can be replaced by a much smaller incremental circuit and the modified architecture is the Carry Increment Adder (CIA) [3].

II. RELATED WORK

Adders are one of the most widely used digital components in the digital integrated circuit design and are the necessary part of Digital Signal Processing (DSP) applications. With the advances in technology, researchers have tried and are trying to design adders which offer either high speed, low power consumption, less area or the combination of them. In this paper, the design of various adders such as Ripple Carry Adder, Carry Skip Adder, Carry Increment Adder, Carry Look Ahead Adder, Carry Save Adder, Carry Select Adder, Carry Bypass Adder are discussed and are compared on the basis of their performance parameters such as area, delay and power distribution [1].

In this paper, a simple and systematic procedure to design Carry Bypass Adders (CBA) is proposed. It allows choosing the block sizes of a CBA to minimize the adder delay, and can be used for pencil and- paper design. Since it derives from rigorous analysis of CBAs, it is general and provides intuitive understanding of the optimum block size. Compared to optimum results reported in the literature, the optimization procedure proposed leads to a delay which is minimum in actual cases, or very close to optimum (within 7%) even in unrealistic cases [2]. The fundamental operation

ISSN (Online) 2394-6849

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in most digital circuits is binary addition. It is very important in VLSI designs to minimize the area, delay and power. In carry skip adder, data to be added is divided into blocks and the carry is skipped though these blocks thereby reducing the time to propagate carry. In this paper a carry skip adder design is implemented on virtuoso, cadence in stages of 2, 8 and 32 bit [4]. In this paper carry bypass and carry increment adder architectures are implemented in XILINX FPGA and compared for their performance. Here we will be finding a suitable adder architecture which will speed up the adder operation. Based on the various speed-up schemes for binary addition, a comprehensive overview of the different adder architectures are given in this report. In addition, it is found that the ripple carry and the carry look ahead adders consumes less area, carry select and carry bypass adders shows the faster performance compare to other adders [5].

The four new reversible gates are also proposed in this paper. Carry-select addition techniques imply the computation of double sum and carry bits with subsequent selection of the correct values, resulting in significant area overheads. This overhead increases massively when the selection scheme is applied to multiple levels in order to further reduce computation time. A recently proposed reduced-area scheme for carry-select adders lowers this overhead by computing the carry and sum bits for a block-carry-in value of 0 only and by incrementing them afterwards depending on the final block-carry-in. The resulting carry-increment adder cuts circuit size down by 23% with no change in performance [7].

Due to the rapidly growing mobile industry, not only faster arithmetic units but also smaller and lower power arithmetic units are demanded. However, it has been difficult to do well both in speed and in area. In general, ripple-carry adder (RCA) provides a compact design but suffers from a long delay time. Carry look ahead adder (CLA) gives a fast design but has a large area. Carry-select adder (CSA) is intermediate in regard to speed and area. Therefore, CSA is suitable in many applications that consider both speed and area. CSA is also used with CLA to improve the speed [9].

III. METHODOLOGY

A. Block Diagram of carry bypass adder using carry look ahead adder.

In Carry Bypass Adder (CBA), CLA is used to add 4-bits at a time and the carry generated will be propagated to next stage with help of multiplexer using select input as Bypass logic. By pass logic is formed from the product values as it is calculated in the CLA. Depending on the carry value and by pass logic, the carry is propagated to the next stage. As shown in below figure 1

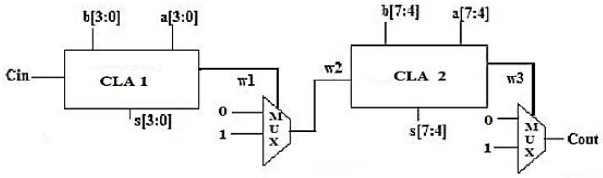

FIGURE 1: Carry Bypass Adder-Carry Look Ahead Adder (CBA-CLA)

B. Block Diagram of carry bypass adder using carry select adder.

In Carry Bypass Adder (CBA), CSA is used to add 4-bits at a time and the carry generated will be propagated to next stage with help of multiplexer using select input as Bypass logic. By pass logic is formed from the product values as it is calculated in the CLA. Depending on the carry value and by pass logic, the carry is propagated to the next stage. As shown in below figure 2.

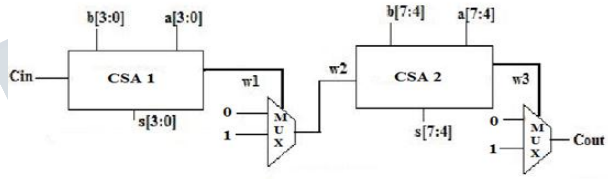

FIGURE 2: CARRY BYPASS ADDER-CARRY SELECT ADDER (CBA-CSA)

C. Block Diagram of carry increment adder using carry look ahead adder.

The standard Carry Increment Adder (CIA) consists of CLA's and incremental circuitry. The incremental circuit is designed using HA's in carry look ahead chain with a sequential order. The addition operation is done by separating the total number of bits in to group of 4bits and addition operation is performed by several 4-bit CLA's. Instead of computing two partial sums for each group and selecting the correct one, only one partial sum is calculated and incremented if necessary, according to the input carry. Thus the second adder and the multiplexers in the carry-select scheme can be replaced by a much smaller incremental circuit and the modified architecture is the Carry Increment Adder (CIA). As shown in below figure 3.

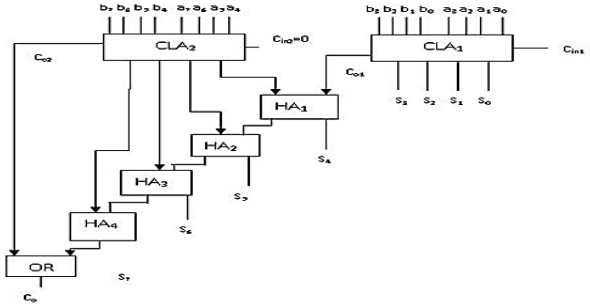

FIGURE 3: Carry Increment Adder-Carry Look Ahead Adder (CIA_CLA)

ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
Vol 5, Issue 1, January 2018

D. Block Diagram of carry increment adder using carry select adder.

In this subsection we present the modified carry increment adder i.e. CIA_CSA. We know that CLA is the circuit and is quite popular because of its simple design. However it suffers from the worst propagation delay affecting the overall performance of the system. It is proved that CSA performs better than CLA in terms of delay at the expense of increased design complexity. We have modified CIA_CLA by replacing the CLA with CSA block. It is quite obvious because of the property of CSA; the overall delay performance will be improved. As similar to CIA_CLA incremental circuit can be designed using HA's in Carry select chain with a sequential order. As shown in below figure 4.

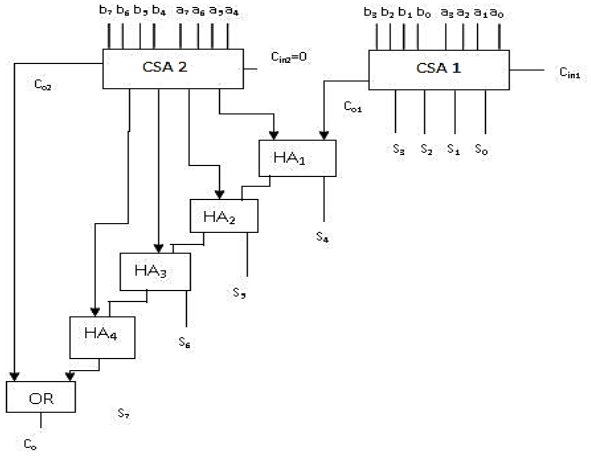

FIGURE 4: Carry Increment Adder-Carry Select Adder (CIA-CSA)

IV. RESULTS AND DISCUSSION

A. RTL Schematic

Figure (5) shows the simulation study of the proposed CBA_CSA & CIA_CSA are presented in this section. The RTL code is written using Verilog HDL and the simulation and design synthesis is carried under Xilinx ISE 12.1 environment. The behavioral simulation result for verifying the design is done under behavioral simulation by writing a test bench. The RTL schematic and technology view are also generated using the synthesis tool. We have performed the experiment for addition of 8 bit binary numbers.

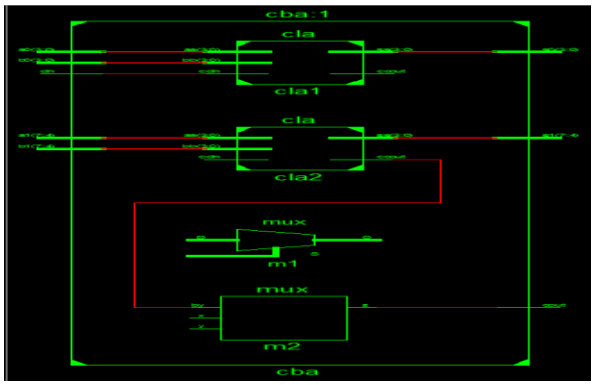

FIGURE 5 . Rtl Schematic Of Carry Bypass Adder-Carry Look Ahead Adder (Cba-Cla)

B. Simulation & power reports

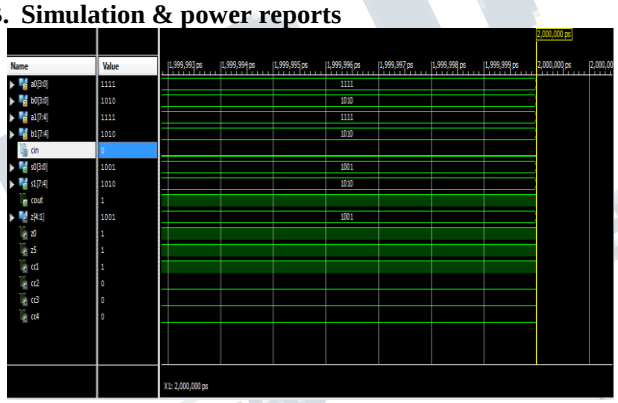

FIGURE 6: Simulation Of Carry Bypass Adder-Carry Look Ahead Adder (CBA-CLA)

Carry Bypass Adder & Carry Increment Adder:-

Below figure (7) shows the Power reports of CBA & CIA. It is observed that the maximum power dissipation .The least power dissipation occurs for ripple carry adder.

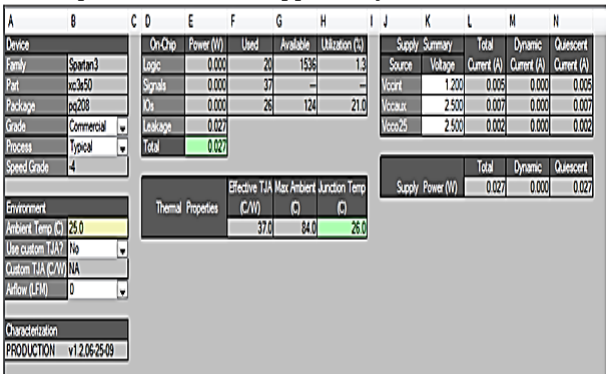

FIGURE 7: Carry Bypass Adder & Carry Increment Adder

C. Comparison Table

Below table (1) shows the comparison of CBA_CLA & CIA_CLA and CBA_CSA & CIA_CSA in terms delay, area

ISSN (Online) 2394-6849

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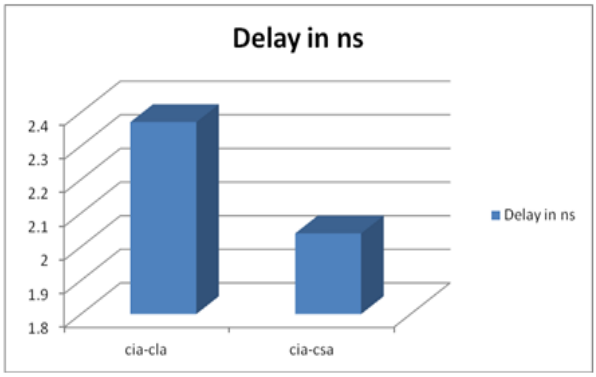
and Memory are given in Table 6. The performance parameters like delay and area are obtained from the Synthesis report and the power dissipation or consumption is calculated using x-power analyzer which is available with the Xilinx ISE design suite.

TABLE I. SYNTHESIS REPORT

DESIGN	AREA (LUTs)	NO OF I/O	AREA (SLICES)	DELAYS (ns)	TOTAL MEMORY USAGE (kb)
CBA-CLA	16	26	9	20.394	205340
CBA-CSA	20	26	11	15.584	205660
CIA-CLA	20	26	11	16.912	205724
CIA-CSA	22	26	12	15.85	204892

TABLE 1: Comparison of CBA & CIA

GRAPH OF CBA USING CLA & CSA



V. CONCLUSION

A modified carry bypass and carry increment adders proposed in this paper using the faster carry look ahead modules instead of the much slower ripple carry adder. By replacing the 4-bit RCA with a 4-bit CLA the delay performance of the circuit is improved in the design without affecting the poer dissipation of the circuit. The design is tested and verified by Verilog HDL coding and simulation is carried out in Xilinx ISE 13.1 environment. In this paper we have carried out the design only for two 8-bit binary addition but the design may be extended to higher order adder circuit. It may pointed out that although CLA has better delay performance than RCA the circuit complexity of CLA increases as the number of bit increases. The choice of a particular adder depends on the intended application. Future work may be dedicated to study the complexity of CIA_CLA when the number of bits are increased.

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