ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
Vol 5, Issue 2, February 2018

On-chip Pentagonal Fractal Inductor for THz Frequency Applications

[1] Nagesh Deevi
[1] PG Scholar, [2] Professor
Dept. of ECE, B V Raju Institute of Technology-Narsapur

Abstract: **- On-chip pentagonal fractal inductor with high inductance for terahertz (THz) frequency applications is presented in this paper. The frequency range of operation of proposed fractal inductor is in the sub-terahertz (sub-THz) band with self-resonant frequency of 335 GHz. The pentagonal fractal inductor is developed on silicon and SiO2, with copper as metal layer. Performance of fractal inductor is compared with planar inductor, fractal inductor shows better performance in terms of quality factor and moderate performance in terms of inductance(pH). On-chip area of the proposed inductor is 100µm×100µm. The simulation results using an electromagnetic simulator showed good agreement with the analysis.**

Keywords: **- GNSS, GPS, GLONASS, IRNSS.**

I. INTRODUCTION

In RF circuits like Phased Locked Loop (PLL), Voltage Controlled Oscillator (VCO) and RF filters, on-chip inductors and capacitors play a vital role in the performance enhancement. Due to the advancement in RF-VLSI fabrication mechanism, the demand for on-chip inductors with miniature area and with high performance has been increased at GHz and sub-THz frequency operating circuits. Using the concept of ferromagnetic materials for CMOS processing technology and also using MEMS system, on-chip inductor performance in terms of Quality factor (Q-factor), inductance and resonant frequency has been enhanced. The maximum Q-factor achieved is 14 at 5.85 GHz. High performance planar inductors with Q-factor of 19.7 operating at 5.1 GHz is presented in literature[1][2]. High performance MEMS planar inductor is fabricated with different inner diameters providing maximum Q-factor of 15.8 and 19.7 at 1.4 GHz and 4.1 GHz respectively [3]. Limitation of MEMS technology is cost effective, development of microsystems and its miniaturization is major challenge [4]. Conventional planar inductors provide very poor Q- factor of 12. This low Q-factor is due to ohmic loss and eddy current loss in standard silicon process. High substrate thickness and high conductivity material is considered to reduce losses. At high frequencies, due to skin effect and high thickness of substrate layer current entering to the conductor decreases, which in turn decrease the substrate losses in device. In addition to this, when outer diameter of device is decreased, the area occupied by the device is minimized, which decreases the substrate losses [5] [6]. To achieve cost-effective silicon devices, area-efficient devices with better performance at desired frequency is required [7]. The performance of these components mentioned in the literature is limited to tens of GHz frequency range only. Later by using the concept of fractal geometry and miniaturized area, the frequency of operation of these components is increased to Sub-THz range. In addition to this, the process of substrate shielding also leads to the improvement in the Q-factor [8] [9]. Proposed on-chip pentagonal fractal inductor is designed and simulated in High Frequency Structure Simulator (HFSS). Silicon and copper are considered as substrate and conducting materials respectively for the design. Substrate thickness is very high to decrease substrate losses and conductivity of copper is very high to decrease ohmic losses. Multi-layer inductor occupies on-chip area of 100µm×100µm, suitable for Sub-THz frequency operating circuits.

II. ON-CHIP PENTAGONAL FRACTAL INDUCTOR DESIGN

Fractal concept is a resultant of space filling curves developed based on mathematical concept. Hilbert, Siepinki, Moore and Osgood are some of the defined iterative space filling curves. Basic fractal phenomenon is explained with the help of Hilbert space filling curve. Figure 1(a) shows the basic Hilbert curve having four sides. The fractal space filling curve generated by replacing each part of an initiator with a curve called generator as shown in Figure 1(b). The

ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
Vol 5, Issue 2, February 2018

size of each segment of the generator considers being one fourth of initiator; the process is dissipated in Figure 1(c). By considering the fractal idea, proposed inductor is developed with the help of pentagonal shape in a single layer. The iteration considered is single iteration and this may be extended till it reaches the best performance. After reaching certain value of iteration, there may be some degradation in behavior of components in terms of inductance and Q-factor.

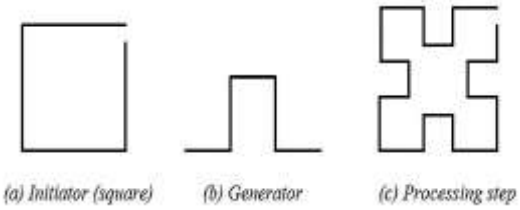

Fig 1 Fractal Inductor Geometry

Proposed pentagonal inductor is shown in Figure 2. The blue color indicates the silicon substrate layer with a thickness of 300µm and green color indicates the Silicon-oxide layer with a thickness of 9.8 µm. The top layer indicates the fractal geometry of pentagonal shape on four sides. The top view of the proposed inductor is shown in Figure 3. The black lines around the inductor structure indicates the PEC material which acts like a ground in analysis. The dimensions of the proposed pentagonal shaped fractal inductor are

1) Width of the conductor is 8 µm.
2) Outer diameter of the conductor is 100 µm.
3) Thickness of the conductor is 2 µm.
4) Induction depth of the fractal inductor is 5 µm.

The concept of fractal increases the length of the overall conductor. This leads to the enhancement of the inductance value. Due to high substrate thickness the losses will decrease and improves the quality factor value which indirectly improves the self-resonant frequency. Lumped ports are connected at the ends of the inductor structure for two-port analysis. Proposed pentagonal fractal inductor performance is compared with planar inductor of similar dimensions with rectangular cross-section.

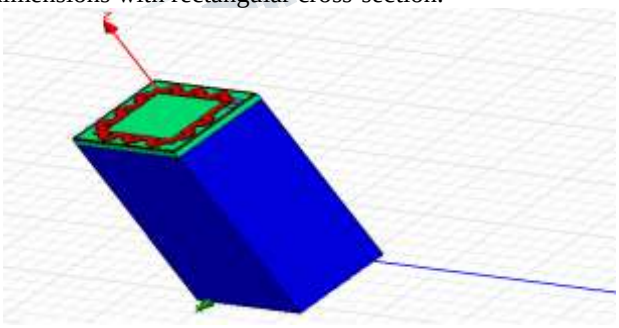

Figure 2 Proposed pentagonal fractal Inductor with different layers

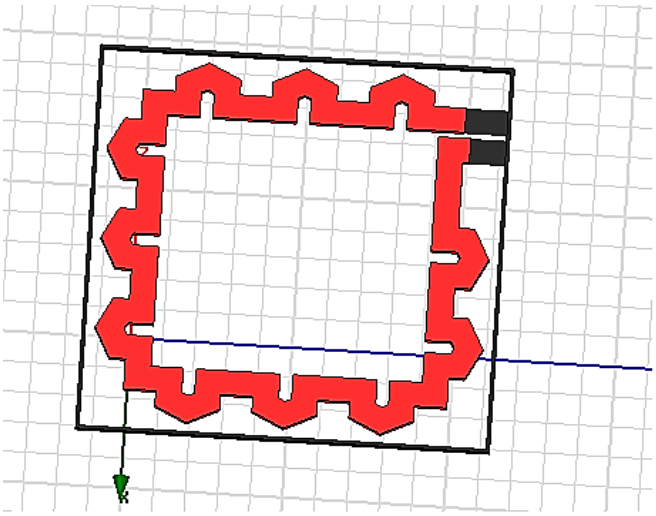

Figure 3 Top view of the proposed pentagonal fractal inductor.

III. RESULTS AND DISCUSSION

Proposed multi-layer inductor is simulated in HFSS. Q-factor and Inductance of the on-chip inductor are obtained from Y-parameters. The expressions for obtaining Q-factor and inductance are given as,

$$Q = \frac{\mathrm{Im}\{Y_{11}\}}{\mathrm{Re}\{Y_{11}\}}$$

$$L = \frac{-1}{(2 * \mathrm{pi} * \mathrm{freq} * \mathrm{Im}\{Y_{11}\}}$$

The performance of pentagonal fractal inductor is compared to planar inductor in terms of inductance (pH) and Q-factor. From the results as shown in Figure 4, the proposed inductor shows moderate performance in terms of inductance when compared to planar inductor. From the result shown in Figure 5, the proposed inductor shows maximum of 98% improvement in terms of Q-factor when compared to planar inductor. The self-resonant frequency of the proposed inductor is 335GHz which is a sub-THz operation. The on-chip area occupied by the proposed inductor and the planar inductor is 100µm×100µm.

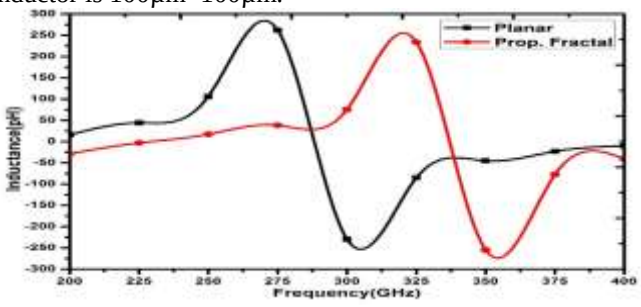

Figure 4 Comparison of Proposed and planar inductor in terms of inductance (pH).

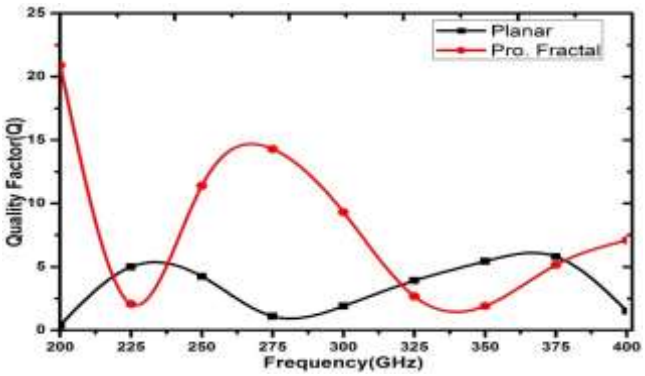

Figure 5 Comparison of Proposed and planar inductor in terms of Q-factor.

IV. CONCLUSION

In this paper, single layer pentagonal fractal inductor is proposed for Sub-THz frequency applications. The performance of proposed fractal inductor is compared with planar inductor. Proposed fractal inductor shows moderate performance in terms of inductance (pH) and 98% improvement in terms of Quality factor when compared to planar inductor. The self-resonant frequency is observed as 325 GHz, maximum inductance value as 324 pH and maximum quality factor as 15 which are suitable for Sub-THz frequency applications. On-chip area occupied by the proposed pentagonal fractal inductor is 100µm×100µm.

REFERENCES

1. Fang, D.-M., Q. Yuan, X.-H. Li, H.-X. Zhang, Y. Zhou, and X.-L. Zhao, "High performance MEMS spiral inductors," The 5th IEEE International Conference on Nano/Micro Engineered and Molecular Systems, 1033-1035, Jan. 2010.

2. Zhao, P. and H. G. Wang, "Resistance and inductance extraction using surface integral equation with the acceleration of multilevel green function interpolation method," Progress In Electromagnetics Research, Vol. 83, 43–54, 2008.

3. Wang, C. and N.-Y. Kim, "Analytical optimization of high-performance and high-yield spiral inductor in integrated passive device technology," Elsevier Microelectronics Journal, Vol. 43, 176-181, Jan. 2012.

4. H.M.Greenhouse , "Design of Planar Rectangular Microelectronic Inductors" , IEEE Transactions On Parts, Hybrids, And Packaging, Vol. Php-10, No. 2,June-74 Pg 101-109

5. Sia, C. B., W. M. Lim, B. H. Ong, A. F. Tong, and K. S. Yeo, "Modeling and layout optimization techniques for silicon-based symmetrical spiral inductors," Progress In Electromagnetics Research, Vol. 143, 1–18, 2013.

6. Pan, S. J., L. W. Li, and W. Y. Yin, "Performance trends of on-chip spiral inductors for RFICs," Progress In Electromagnetics Research, Vol. 45, 123–151, 2004.

7. Tseng, S.-H., Y.-J. Hung, Y.-Z. Juang, and M. S.-C. Lu, "A 5.8-GHz VCO with CMOS-compatible MEMS inductors," Elsevier Sensors and Actuators A, Vol. 139, 187–193, 2007.

8. Shi, J., Yin, W.-Y., Kang, K., Mao, J.-F., and Li, L.-W.: 'Frequency-thermal characterisation of on-chip transformers with patterned ground shields', IEEE Trans. Microw. Theory Tech., 2007, 55, (1), pp. 1 –12.

9. Cheung, T.S.D., and Long, J.R.: 'Shielded passive devices for silicon based monolithic microwave and millimetre-wave integrated circuits', IEEE J. Solid-State Circuits, 2006, 41, (5), pp. 1183 –1200.