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DSP Accelerator Architecture Using Carry-Save Arithmetic

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Abstract: **- A high performance data path to implement DSP kernels are introduced in this paper .Hardware acceleration has been proved an extremely promising implementation DSP domain. We present a novel accelerator architecture comprising flexible computational units for the execution of a large set of operation templates in DSP kernels. Carry Save method has been implemented to improve the performance of the accelerator while computing more bits. Advanced arithmetic design concepts, i.e., recoding techniques, are utilized enabling CS optimizations to be performed in a larger scope than in previous approaches. Accelerator architecture delivers average gain compared with the state-of-art flexible datapaths.**

KEYWORDS**- Arithmetic optimizations, carry-save (CS) form, datapath synthesis, flexible accelerator, flexible datapath operation chaining, recoding techniques.**

I. INTRODUCTION

Latest embedded systems aim at high speed performance and solving the complexity of digital signal processing (DSP) functions through specialized hardware accelerators [1]. Though application-specific integrated circuits (ASICs) are ideal acceleration solution for performance and power, they also leads to increased silicon complexity, as complex ASICs are needed to accelerate various kernels. Many researchers had found to increase ASICs' flexibility without significantly compromising their performance. Flexible datapaths [2], [4], [6], [7], [10] are used to flow graph (DFG) of a kernel. Design decisions have high impact its efficiency. Existing works mainly exploit architecture-level optimizations, e.g., increased instruction-level parallelism (ILP) [2]–[5], [7] and operation chaining. The domain-specific architecture of [5] and [9] efficiently map primitive or chained operations in the initial data-vary the type and number of computation units for a customized design structure. Recently, aggressive operation chaining have been implemented for the computation of entire subexpressions using multiple ALUs with various arithmetic features. Manuscript received July 25, 2014; revised October 16, 2014 and December 12, 2014; accepted January 8, 2015.

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The above described architectures exclude arithmetic optimizations during the architectural synthesis and consider them only at the internal circuit structure of primitive components, e.g., adders, during the logic synthesis [11].The [12]–[14] arithmetic optimizations at higher abstraction levels than the structural circuit have significant impact on the datapath performance. In [12], timing-driven optimizations based on carry-save (CS) arithmetic were performed at the post-Register Transfer Level (RTL) design stage.Verma et al. [14] developed modifications on DFG to maximize the use of CS arithmetic. The aforementioned CS optimization approaches target inflexible datapath, i.e., ASIC, implementations. Recently, Xydis et al. [6], [7] proposed a flexible architecture combining the ILP and pipelining techniques with the CS-aware operation chaining. However, all the above solutions feature a strong drawback, i.e., CS optimization is bounded to merge only additions/subtractions. A CS to binary conversion is inserted before each operation which differ from addition/subtraction, e.g., allocating multiple CS to binary conversions heavily degrades performance due to time-consumptions in carry propagations. In this paper, we propose a high-performance architectural scheme for the generation of flexible DSP accelerators by grouping optimization techniques from both the architecture and arithmetic levels of abstraction. We propose a flexible datapath architecture that exploits CS optimized templates of chained operations that comprises of flexible computational units (FCUs). It delivers average gain up to 61.91% in area-delay product and 54.43% in energy

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consumption compared to state-of-art flexible datapaths [4], [7], managing efficiency toward scaled technologies.

II. CARRY-SAV E AR I TH M ETI C : MOT IVAT IONAL OBSE RVAT I ONS AND DRAWBACKS

CS concepts [15] has been widely used to construct arithmetic circuits having high performance and to eliminate carry-propagation chains. They have multiple input additive operations (i.e., chained additions in the initial DFG), mapping onto CS compressors. The goal is to widen the CS computation within the DFG. A multiplication node is inserted in the DFG, either from CS to binary conversion [12] or the DFG is transformed using the distributive property [14]. CS optimization have limited impact on DFGs e.g., filtering DSP applications. In this brief, we solve the limitation by making use of the CS to modified Booth (MB) [15] and recoding each time a multiplication within a CS-optimized datapath. Thus, the

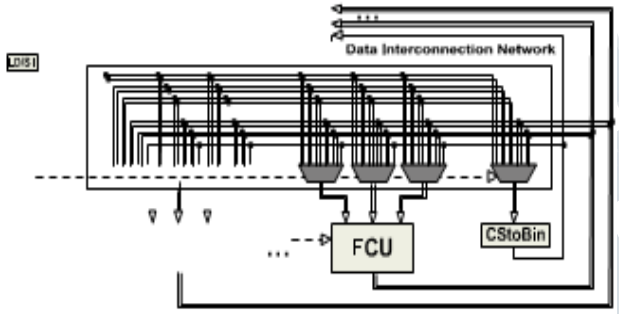

Fig. 1. Abstract form of the flexible datapath.

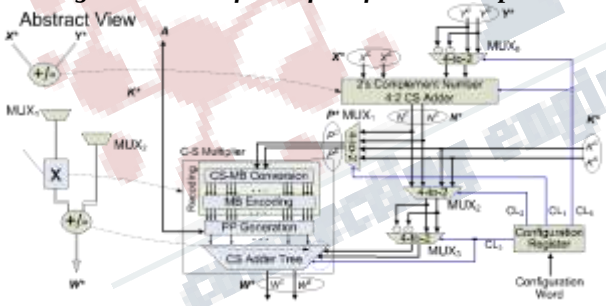

Fig. 2. FCU.

computations are processed using CS arithmetic. Without using any intermediate carry-propagate adder the operation in the targeted datapath are carried in CS to binary conversion,for enhancing the performance.

III. PRO POSE D FLEX I B LE ACC ELER ATO R

The flexible accelerator architecture is shown in Fig. 1. Each FCU operates 16 bit operand directly on CS operands and produces output in the same form1 for reuse of results obtained. Such a bit-length is adequate for the most DSP datapaths [16]. But the architectural concept of the FCU are also adapted for smaller or larger bit-lengths. The number of FCUs arebased on the ILP and area constraints. The CStoBin module is a ripple-carry adder and converts the CS form to the two's complement one. The register bank consists of scratch registers, used for storing intermediate results and sharing operands among the FCUs. Different DSP kernels (i.e., different register allocation and data communication patterns per kernel) can be mapped onto the proposed architecture using post-RTL datapath interconnection sharing techniques [9], [17], [18]. The control unit drives the overall architecture (i.e., communication between the data port and the register bank, configuration words of the FCUs and selection signals for the multiplexers) in each clock cycle.

A. Structure of the Proposed Flexible Computational Unit

The structure of the FCU (Fig. 2) designed are used for high-performance flexible operation chaining based [4], [7]. Each FCU can be configured to any of the T1–T5 operation templates shown in Fig. 3. The FCU also enables intratemplate operation chaining by fusing the additions

1 The FCU operates on either CS or two's complement formatted operands

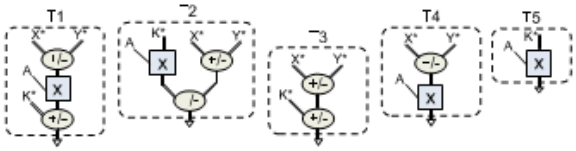

Fig. 3. FCU template library.

performed before/after the multiplication and performs any partial operation template of the following complex operations:

$$W^* = A \times (X^* + Y^*) + K^* \quad (1)$$

$$W^* = A \times K^* + (X^* + Y^*). \quad (2)$$

The following relation holds good for all CS data:

$$X^* = \{X^C, X^S\} = X^C + X^S.$$

The operand A is a two's complement number. The control signals of the multiplexers MUX_1 and MUX_2 (Fig. 2) are set for the alternative execution paths in each FCU. The output of MUX_0 Y^* when $CL_0 = 0$ (i.e., $X^* + Y^*$ is carried out) or Y^* when $X^* - Y^*$ is required and $CL_0 = 1$. The

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Vol 5, Issue 4, April 2018

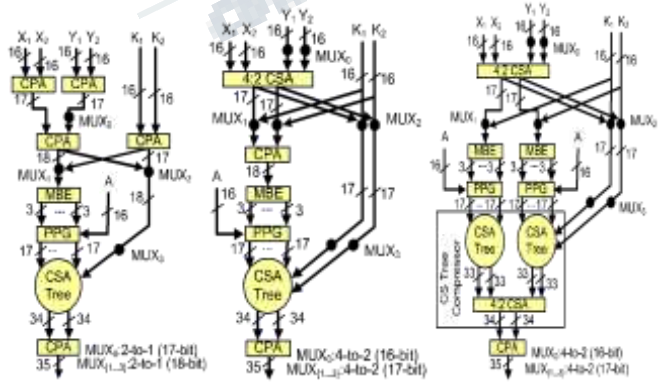
two's complement 4:2 CS adder produces the output $N^* = X^* + Y^*$ when the input carry equals 0 or the $N^* = X^* - Y^*$ when the input carry equals 1. The MUX_1 specifies if N^* (1) or K^* (2) is multiplied with A. The MUX_2 specifies if K^* (1) or N^* (2) is added with the product. The multiplexer MUX_3 consists of the output from MUX_2 and its 1's complement and outputs the former one when an addition with the multiplication product is required (i.e., $CL_3 = 0$) or the later one when a subtraction is carried out (i.e., $CL_3 = 1$). The 1-bit ace for the subtraction is added in the CS adder tree. The multiplier consists of CS-to-MB module, [19] to recode the 17-bit P^* in its MB digits with minimal carry propagation. The product consists of 17 bits. The compensation method is included to eliminate the error during truncation [20].

B. DFG Mapping Onto the Proposed FCU-Based Architecture

In order to map DSP kernels onto the proposed FCU-based accelerator, the semiautomatic synthesis methodology [7] has been adapted. Firstly, a CS operation is performed onto the original DFG, merging nodes of multiple chained additions/subtractions to 4:2 compressors to form FCU template operations (Fig. 3). The designeropt for the FCU operations having the DFG with minimized delay.

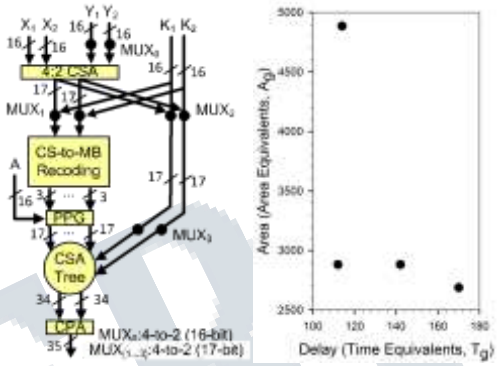
Number of FCUs is fixed, a resource-constrained scheduling is considered with the available FCUs and CStoBin modules determine the resource constraint set. The clustered DFG is assigned to a specific control step. A list-based scheduler [21] has been adopted considering the mobility2 of FCU operations according to descending mobility. These operations are bound onto FCU instances and proper bits are generated. After completing register allocation, a FSM is generated to implement the control unit of the overall architecture.

2 Mobility: The ALAP-ASAP difference of the FCU operations.



(a) *(b)* *(c)*

Fig. 4. Typical chaining of addition–multiplication–addition operations reflecting T1 template of Fig. 3. Its design is based on (a) two's complement arithmetic, (b) CS optimizations of [12], (c) CS optimizations with multiplication distribution [14], and (d) incorporating the CS-to-MB recoding concept. (e) Positioning of the proposed approach with respect to the two's complement one and the CS optimizations based on [12] and [14].



(d)(b)

IV. THEORE T I CAL ANA LY S I S

Based on the unit gate model, we provide the theoretical analysis of the proposed approach. Fig. 4(a) shows the AMADFG when all operands are in two's complement form. Fig. 4(b) shows CS optimizations of [12] . Fig. 4(c) illustrates how [14] distributes the multiplication operation over the CS formatted data. The Fig. 4(d) incorporates the CS-to-MB recoding unit. We assume 16-bit input operands for all the designs and, without loss of generality, we do not consider any truncation concept during the multiplications. Fig. 4(e) shows the positioning of the proposed approach based on [12] and [14].The proposed design solution is the most effective among all the design alternatives.

V. EX P ER I M EN TA L EVA L UAT I O N

A .Proposed FCUs circuit level exploration

A circuit-level comparative study was conducted among the proposed FCU, the flexible computational component (FCC) of [4] and the reconfigurable arithmetic unit (RAU)4 of [7] in scaled technology nodes.bits of the respective two's complement form in scaled .The scaling impact on the performance does not eliminate the benefits of using CS arithmetic. The three units considered were described in RTL using Verilog code .The CSA tree and the adders and multipliers of the FCC were imported from the Synopsys Design Ware library [11]. We used Synopsys Design Compiler [11] to synthesize the examined units and the TSMC 130, 90, and 65nm

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Vol 5, Issue 4, April 2018

standard cell libraries.5 Each unit is synthesized with the highest optimization degree at its critical clock period and 20 higher ones with a step interval of 0.10 ns. Fig. 5 reports the area complexity of the evaluated units

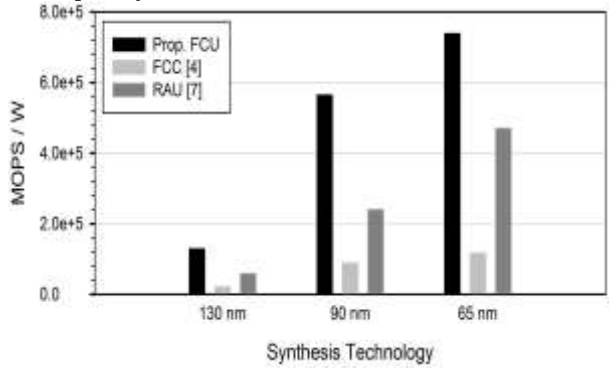

Fig. 6. MOPS/W values of FCUs at the lowest achievable clock periods with respect to the synthesis technology.

FCC, and the RAU operate without timing violations starting at 2.98, 4.83, and 1.99 ns, respectively. At 90 nm, the proposed FCU, the FCC, and the RAU are timing functional starting at 1.66, 2.46, and 1.01 ns, respectively .At 65 nm, the proposed FCU, the FCC, and the RAU start operating without timing violations at 1.13, 1.68, and 0.67 ns, respectively .Fig. 5 shows that the proposed FCU outperforms the FCC in terms of critical delay and area complexity, but presents larger values for these metrics than the RAU in all the technology nodes. However, RAU's flexible pipeline stage (FPS) [7] features limited ability in carrying out heavy arithmetic operations as shown from the mega operations per second/watt (MOPS/W)6 evaluation in Fig. 6. Fig.6 shows the MOPS/W values for the proposed FCU, the FCC, and the RAU at their critical clock periods with respect to the synthesis technology. For each unit, we consider the templates

VI. CONCL U SION

In this detailed description, we have proposed a flexible accelerator architecture that the incorporates CS arithmetic operations for fast switching of addition and multiplication operations. Thus the flexible accelerator is able to operate on both conventional two's complement and CS-formatted data, enabling high degree of computation. Theoretical and practical analyses have shown that the above solution provides an effective design tradeoff point with optimized latency/area and energy implementations. This accelerator enhances the performance than anyother,providing better reliability.

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