ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
Vol 5, Issue 4, April 2018

A Low Power and Area Efficient Symmetric Stacking Counter

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Abstract: **- A very high speed, power and area efficient counter is required in many applications viz. digital memories, ADCs, DACs, microcontroller circuits, frequency dividers, frequency synthesizer etc. Less area, high speed and low power consumption may be met by reducing the size of hardware. Hence, as the applications are increasing, demand for smaller size and longer life batteries increases. This project derives area, power and speed efficient structure counter based on a VLSI design. It uses multiplexer based full adder circuit, which group all of the "1" bits together. In the proposed structure, one XOR block in the conventional full adder is replaced by a multiplexer block so that the critical path delay is minimized. Proposed system is coded in Verilog and simulated using Xilinx 12.1.**

Keywords: **- xor Block; Critical path;Multiplxer.**

I. INTRODUCTION

Very-Large-Scale Integration (VLSI) is the process of creating an Integrated Circuit (IC) by combining thousands of transistors into a single chip. VLSI began in the 1970s when complex semiconductor and communication technologies were being developed. The microprocessor is a VLSI device. Before the introduction of VLSI technology, most ICs had a limited set of functions they could perform. An electronic circuit might consist of a CPU, ROM, RAM and other glue logic. VLSI lets IC designers add all of these into one chip.The electronics industry has achieved a phenomenal growth over the last few decades, mainly due to the rapid advances in large scale integration technologies and system design applications. With the advent of very large scale integration (VLSI) designs, the number of applications of integrated circuits (ICs) in high-performance computing, controls, telecommunications, image and video processing, and consumer electronics has been rising at a very fast pace.

II. LITERATURE SURVEY

Design Of 8-4 And 9-4 Compressors Forhigh Speed Multiplication Marimuthu, R., Dhruv Bansal, S. Balamurugan and P.S. Mallick presents higher order compressors which can be effectively used for high speed multiplications. The proposed compressors offer less delay and area. But the Energy Delay Product (EDP) is slightly higher than lower order compressors. The performance of 8×8, 16×16 and 24×24 multipliers using the proposed higher order compressors has been compared with the same multipliers using lower order compressors and found that the new structures can be used for high speed multiplications.

Low-Voltage Low-Power Cmos Full Adder

D.Radhakrishnan presents a Low-voltage low-power CMOS full adder. Low power design of VLSI circuits has been identified as a critical technological need in recent years due to the high demand for portable consumer electronics products. In this regard many innovative designs for basic logic functions using pass transistors and transmission gates have appeared in the literature recently. These designs relied on the intuition and cleverness of the designers, without involving formal design procedures. Hence, a formal design procedure for realizing a minimal transistor CMOS pass network XOR-XNOR cell. That is fully compensated for threshold voltage drop in MOS transistors, is presented. This new cell can reliably operate within certain bounds when the power supply voltage is scaled down, as long as due consideration is given to the sizing of the MOS transistors during the initial design step. A low transistor count full adder cell using the new XOR-XNOR cell is also presented.

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III. EXISTING SYSTEM

FAST BINARY COUNTERS BASED ON SYMMETRIC STACKING

Christopher Fritz and Adly T. Fam presents a binary counter design is proposed. It uses 3-bit stacking circuits, which group all of the "1" bits together, followed by a novel symmetric method to combine pairs of 3-bit stacks into 6-bit stacks. The bit stacks are then converted to binary counts, producing 6:3 counter circuits with no xor gates on the critical path. This avoidance of xor gates results in faster designs with efficient power and area utilization. In VLSI simulations, the proposed counters are faster than existing parallel counters and also consume less power than other higher order counters. Additionally, using the proposed counters in existing counter-based Wallace tree multiplier architectures reduces latency and power consumption

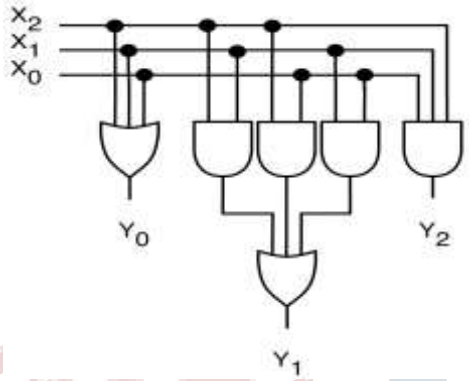


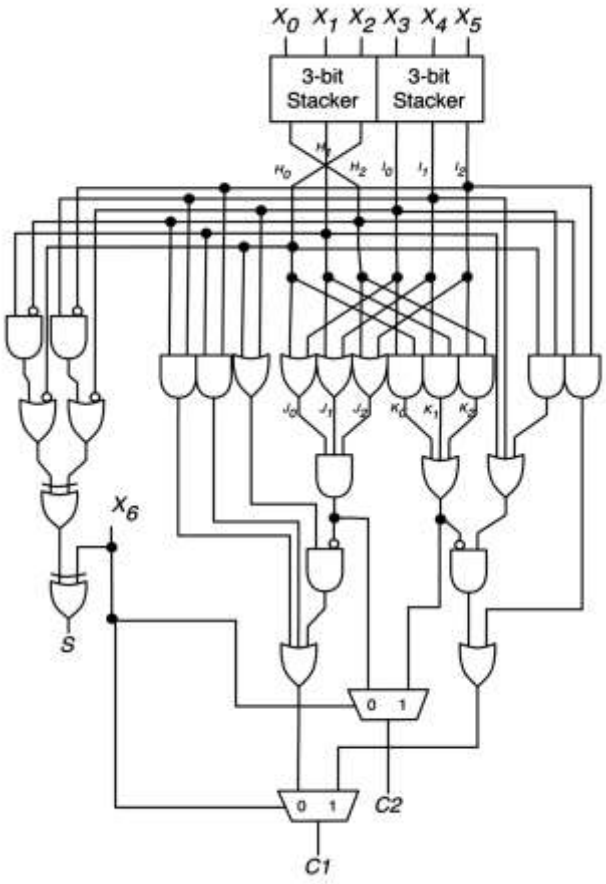
Figure: Three-Bit Stacker Circuits

Given inputs X0, X1, and X2, a 3-bit stacker circuit will have three outputs Y0, Y1, and Y2 such that the number of "1" bits in the outputs is the same as the number of "1" bits in the inputs, but the "1" bits are grouped together to the left followed by the "0" bits. It is clear that the outputs are then formed by

Y0 = X0 + X1 + X2
Y1 = X0X1 + X0X2 + X1X2
Y2 = X0X1X2.

Namely, the first output will be "1" if any of the inputs is one, the second output will be "1" if any two of the inputs are one, and the last output will be one if all three of the inputs are "1." The Y1 output is a majority function and can be implemented using one complex CMOS gate. The 3-bit stacking circuit is shown in Figure.

Figure Counter Based On Symmetric Stacking



The symmetric stacking method can be used to create a 7:3 counter as well. The 7:3 counters are desirable as they provide a higher compression ratio. The design of the 7:3 counter involves computing outputs for C1 and C2 assuming both X6 = 0 (which matches the 6:3 counter) and assuming X6 = 1. We compute the S output by adding one additional XOR gate.

If X6 = 1, then C1 = 1 if the count of X0, . . . , X5 is at least 1 but less than 3 or 5, which can be computed as

C1 = (H0 + I0)J0 J¯1 J2 + H2 I1 + H1 I2.

Also, C2 = 1 if the count of X0, . . . , X5 is at least 3

C2 = J0 J1 J2.

Both versions of C1 and C2 are computed and a mux is used to select the correct version based on X6. Note that this design therefore has muxes on the critical path. The 7:3 counter design is shown in Figure.

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IV PROPSED SYSTEM

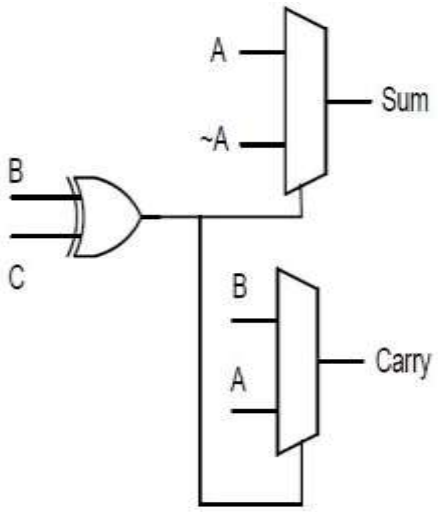
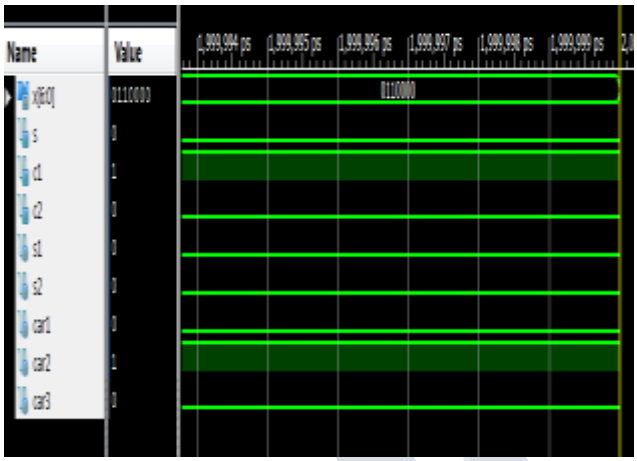


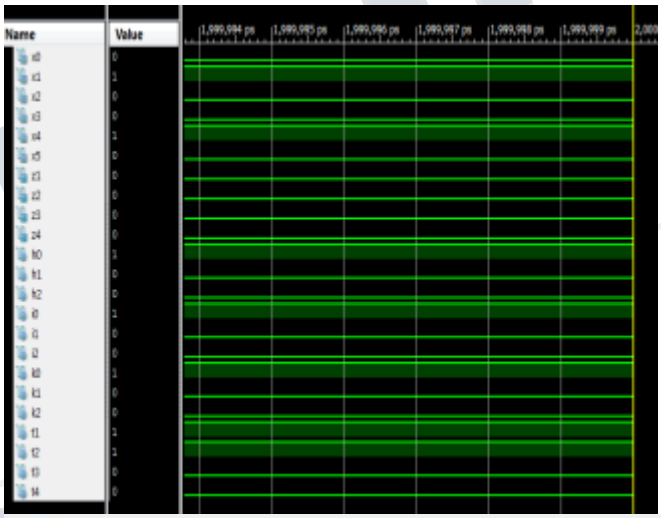
Figure: Proposed Full Adder

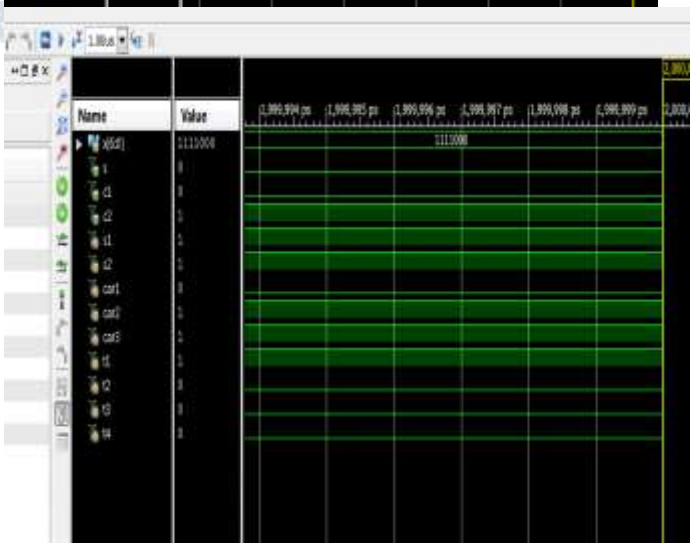
This can be implemented by using second MUX with XOR output as selection line. Since XOR employs most of the power consumption in the adder circuit, by reducing number of XOR gates, power consumption of the full adder can be reduced. The proposed full adder is applied into array multiplier reduction stage to validate the effectiveness. In array structure the partial products is divided into certain levels. In each level, whenever there are three bits, full adder has to be used. Out of the three inputs, one input and its complement is provided as inputs to the first multiplexer. The other two inputs are given to XOR gate, the output of which will act as a select line to both the multiplexers. The inputs of the second multiplexer are, the bits other than the carry bit. This unique way of designing leads to the reduction of the switching activity, which in turn reduces the power. In addition to this, the critical path delay is also reduced compared to the existing designs discussed in literature, which leads to reduction in delay and thus increasing the speed. Operation of the proposed full adder can be explained as follows:

a) When both B and C are zero or one, sum = A;
b) When either of B or C is one and another is zero, sum=A;
c) When both B and C are zero or one, carry= B;

When either of B or C is one and another is zero, carry=A;l





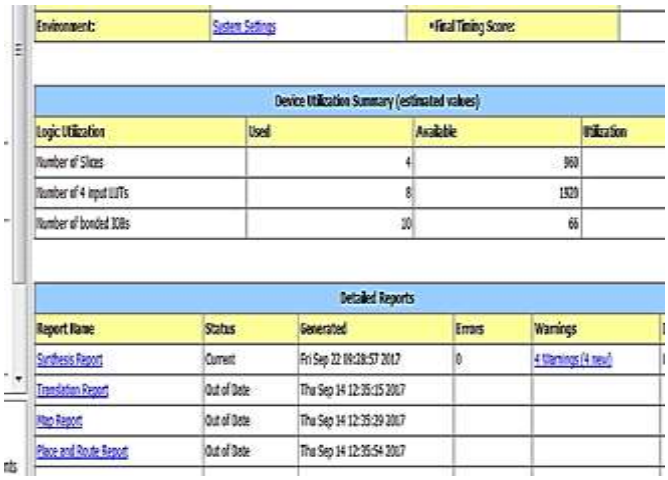


V SIMULATION RESULTS

1. Conventional Counter Output

ISSN (Online) 2394-6849

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)
Vol 5, Issue 4, April 2018



Environment:	System Settings	•Final Timing Score:

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	4	960	
Number of 4 input LUTs	8	1920	
Number of bonded IOBs	10	66	

Detailed Reports				
Report Name	Status	Generated	Errors	Warnings
Synthesis Report	Current	Fri Sep 22 09:28:57 2017	0	4 Warnings (4 new)
Translation Report	Out of Date	Thu Sep 14 12:35:15 2017		
Map Report	Out of Date	Thu Sep 14 12:35:29 2017		
Place and Route Report	Out of Date	Thu Sep 14 12:35:54 2017		

VI CONCLUSION

In this brief, a design method for area effective and speed efficient counter is designed and simulated. A binary counter based on a novel symmetric bit Sum and carry calculation approach is proposed. We showed that this counting method can be used to implement 6:3 and 7:3 counters, which can be used in any binary multiplier circuit to add the partial products. We demonstrated that 6:3 counters implemented with this NFA technique achieve higher speed than other higher order counter designs while reducing power consumption. Lower area, high speed and low power consumption may met by reducing size of hardware. Hence as the applications are increasing, demand for smaller size and longer life batteries increases. This project derives area, power and speed efficient structure counter for VLSI designing as the size of chip is reducing day by day. It uses mux based full adder circuit, which group all of the "1" bits together In the proposed structure, one XOR block in the conventional full adder is replaced by a multiplexer block so that the critical path delay is minimized. Proposed system coded in Verilog and simulated using Xilinx 12.1

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