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Library Characterization of D Flip-Flop

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Abstract- **Cell library characterization is a model of standard cell library possessing a very high quality. Characterization is done because the functionality/delay simulation takes too long. In addition, the power extraction from the whole chip takes more time and automatic detection of timing constraints is also very hard. Hence to overcome this problem, cell characterization is employed. Cell library characterization accurately and efficiently models cell behavior. For accurate modeling of voltage variation or temperature gradient, it is necessary to characterize each library at multiple voltages and multiple temperatures, increasing the total number of library corners. The D flip-flop used here overcomes the drawback of intermediate output and non-allowed logic states by the SR flip-flop.**

***Index Terms*— Cell library characterization, D flip-flop.**

I. INTRODUCTION

As the complexity of circuit design grows, it is becoming increasingly impractical to design logic circuit by hand. Therefore, the use of automatic synthesis EDA tools has become mandatory to speed up the design process. Designing at nanometre process technologies and especially at advanced nodes (28nm and below) requires many additional library views in order to achieve high quality silicon and avoid silicon re-spins due to inaccurate sign off analysis. For accurate modelling of instance specific voltage variation or temperature gradients, it is vital to characterize each library at multiple voltages and multiple temperatures, increasing the total number of library corners. Cell library characterization creates a set of high quality models of standard cell library that accurately and efficiently models cell behaviour. These set of models are used by several different design tools for different purposes. For the most advanced processors, it is becoming common to offer alternative cell libraries that improve yield at the expense of area and performance.

II. SPECIFICATIONS

The major drawback of the SR flip-flop i.e. its indeterminate output and non-allowed logic states are overcome by the D type flip-flop. D flip-flop has the ability to 'latch' and remember data, or a Delay flip-flop because latching and remembering data can be used to create a delay in the progress of that data through a circuit. The important details to be taken into consideration are: Propagation Delay: It is the time taken by the cell for a signal at the input pin to effect the output signal at the output pin. Setup Time: Setup time is the minimum amount of time the data signal should be held steady before the clock events so that the data are reliably sampled by the clock.

Hold Time: Hold time is the minimum amount of time the data signal should be held steady after the clock event so that the data are reliably sampled.

Recovery Time: Recovery time is the minimum amount of time required between the release of an asynchronous signal from the active state to the next active clock edge. It is the time between the reset and clock transition for flip-flop.

Removal Time: Removal time specifies the minimum amount of time between an active clock edge and the release of an asynchronous control signal.

Static Power: Static power is power consumed while there is no circuit activity. For example, the power consumed by a D flip-flop when neither the clock nor the D input have active inputs.

Dynamic Power: Dynamic power is power consumed while the inputs are active. When inputs have ac activity, capacitances are charging and discharging and the power increases as a result. The dynamic power includes both the ac component as well as the static component.

Rise Time: Time taken by a signal to rise from 10% to 90% of its final value.

Fall Time: Time taken by a signal to rise from 10% to 90% of its final value

Minimum Pulse Width: It is the interval between the rising edge of the signal crossing 50% of VDD and falling edge of the signal crossing 50% of VDD.

Leakage Power: Leakage power is the result of unwanted sub-threshold current in the transistor channel when the transistor is turned off.

Average Power: Average power is the average amount of work done or energy transferred per unit time.

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III. DESIGN

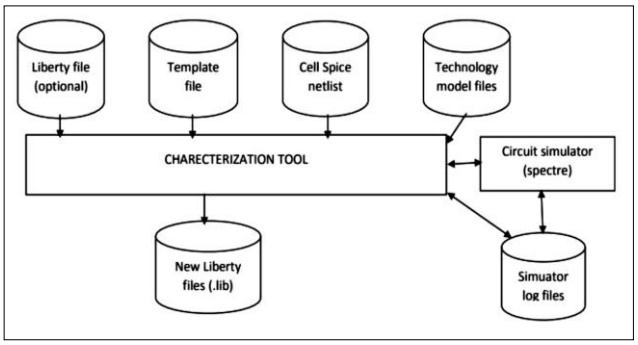

Figure 1. Block diagram

Library characterization requires only the foundry device models and the extracted cell netlist from which it will create all the required electrical views. The layout for the cell to be characterized is designed using layout editor for a specific technology and the netlist is generated. After extraction of netlist, some process and design dependent parameters such as temperature, voltage are defined. Different models are selected
depending on their accuracy, complexity and requirements. The technology model files consists of different parameters which are to be characterized. The simulation is done using spectre simulator and the outputs are measured to extract the required characterization parameters. Using these parameters, the model for the standard cell is prepared.

IV. TESTING

The spectre code for the D flip-flop schematic shown in fig.6.1 is given below. Spectre is an advanced circuit simulator that simulates analog and digital circuits at the differential equation level. Cadence provides a library characterization flow centred on the Cadence Virtuoso Characterization Suite. This Simulator provides fast, accurate Spice-level simulation. The simulator uses improved algorithms that offer increased simulation speed and greatly improved convergence characteristics over Spice. It is tightly integrated with the Cadence Virtuoso custom design platform and provides detailed transistor-level analysis in multiple domains. Its superior architecture allows for low memory consumption and high capacity analysis. Besides the basic capabilities, the spectre circuit simulator provides significant additional capabilities over Spice. The characterized parameters are given in table 1.

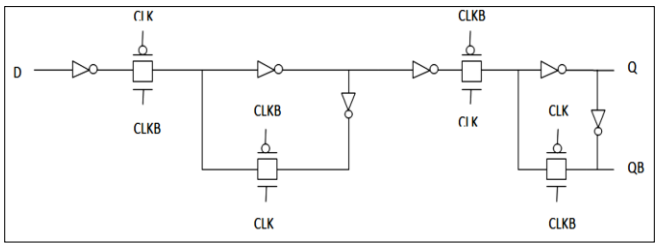

Figure 2. Schematic of D flip-flop

V. RESULT

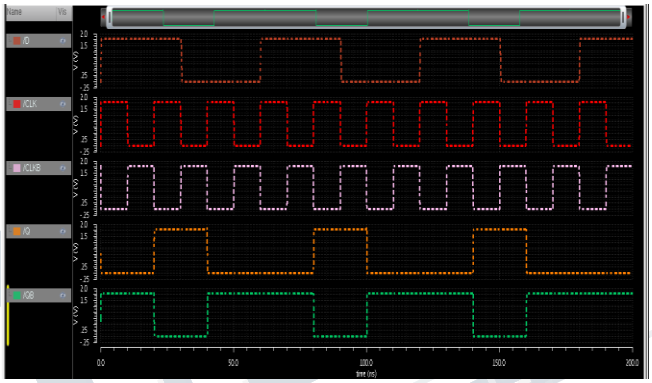

Figure 3. Output waveform of D flip-flop

Table 1. Characterized Parameters

PARAMETER	VALUE
Rise Time	64.58E-12s
Fall Time	39.13E-12s
Average Power	540.4E-3W
D to Q Delay	19.98E-9s
Clock to Q Delay	20.08E-9s

VI. CONCLUSION

In this paper, D flip flop is used for accurate and efficient modeling of cell library characterization. Parameter like rise time, fall time, average power, D to Q & clock to Q delay are characterized using Cadence Virtuoso Custom design platform this methodology helps in reducing the power extraction time and increasing the total number of library corners.

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