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Development Of Universal Verification Methodology Verification Component For Near Field Communication Type 5 Tags

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Abstract- **In the recent years, radio frequency identification has come a long way from anonymity into mainstream applications that help speed up the access control, authentication, ski ticketing etc. As a finely-honed version of high frequency Radio Frequency Identification, Near Field Communication devices have taken benefits of the shorter read range boundaries of its radio frequency i.e. 13.56MHz. NFC facilitates short range exchange between attuned devices; which implies that they only operate when the two devices are brought closer to each other or they touch. One of the devices must be powered on for a two-way exchange to take place. The second device saves its battery for other things, or it may not have a battery at all. This paper is based on building a Universal Verification Methodology Verification Component based on ISO/IEC 15693 protocol i.e. Type 5 NFC tags. The methodology used to build the verification component was Universal Verification Methodology. This UVM Verification Component developed can be reused in any application of NFC tag which is based on the ISO/IEC 15693 protocol with little modifications to the test bench architecture.**

Index Terms— Near Filed Communication, Radio frequency identification, Universal Verification Methodology.

I.INTRODUCTION

Near Field Communication is a standard for short range communication technology that makes life simpler, enhanced and more convenient for users around the world by making it simpler to put together transactions, exchange digital messages, and connect electronic gadgets with a touch or by bringing them nearer to each other [1]. It is a subset of radio Frequency Identification technology which operates on standards such as ISO/IEC 14443 and 15693.

NFC interface can work in various modes. These modes are differentiated on whether the device produces its own field or the device uses the power from the field generated by another device [2]. If the device produces its own RF field, it is called an active device otherwise it is called a passive device. Active devices normally have a power supply of their own while passive devices normally do not.

Five basic tag types are available with designation 1 to 5 each with different format and capacity. NFC Type 1 and 2 operate based on ISO/IEC 14443-A protocol, Type 3 tags are based on JIS 6319-4 standard, Type 4 tags are based on ISO/IEC 14443 –A/B standards. All the above-mentioned types of tags operate on standards for proximity cards. Type 5 tags are based on ISO/IEC 15693 protocol which is a standard for vicinity cards. The vicinity cards can operate at range of 10cm to 1.5 meters from the reader i.e. the Vicinity Coupling Device (VCD). A VICC can operate in various modes like addressed, non- addressed or selected mode. In the addressed mode the Unique ID of the VICC is sent in the request so that only the address VICC will respond back. In the non-addressed mode, no unique ID is sent in the request. So, all the cards in the field will respond back.

II. LITERATURE REVIEW

From its very first marketable application, RFID-systems have reached an elevated level of development and have been used in different applications such as transportation, logistics, access control, tagging, and work-in-progress during manufacturing steps, electronic identification, etc. [3]. This gave way to the advancement and the implementation of universally accepted ISO standards.

RFID uses radio waves for communication between electronic tags attached on objects and a reader [4]. RFID tag chip based on IS0/IEC15693 [5] standard is passive tag of NFC type 5. A passive RFID tag system needs very low power utilization to enhance the recognition distance. ISO/IEC 15693 is a protocol for vicinity cards, with operating range of up to 1.5 m.

UVM (Universal Verification Methodology) used in this paper is based on the System Verilog hardware verification language. It is a well-established approach for verification of the SOC and IP [6]. Since UVM is based on object oriented programming, all the blocks of it are characterized as objects that are derived from the already present classes; This methodology allows the reuse of verification components. Since the reuse of verification components is

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possible, a lot of time to verify components like it is reduced. Large numbers of verification engineers have started using UVM to verify various parameterized designs at both System on Chip level and Module-level. In these cases, how to build a parameterized test bench founded on UVM to verify parameterized design is a major worry. A highly parameterized test bench with good reusability can be configured flexibly to accomplish parameterized verification of the DUT, or it can divide the same parameter with the parameterized DUT, which helps it make the test bench and DUT to be of high consistency [7]. This greatly decreases the effort of verification for verifying a parameterized DUT and increases the chances of reusability of the test bench. Besides, a reusable parameterized test bench normally greatly reduces the verification time and improves the quality of verification. The verification plan gives us a platform for the complete design team to describe what first-time success is. It is a procedure that ensures all vital functionalities are properly verified. If we want first-time success, we must point out which functionalities must be exercised under what conditions and what the response to them should be. The verification plan documents which functionalities are of importance and which ones are elective [8]. The substitute is to subsist with anything that happens to operate when the judgment to send the design. This cuts off the effort required for verification like a guillotine. Some of the specs which are essential for the market acceptance might come in the basket.

III. METHODOLOGY USED TO DEVELOP THE UVM VERIFICATION COMPONENT

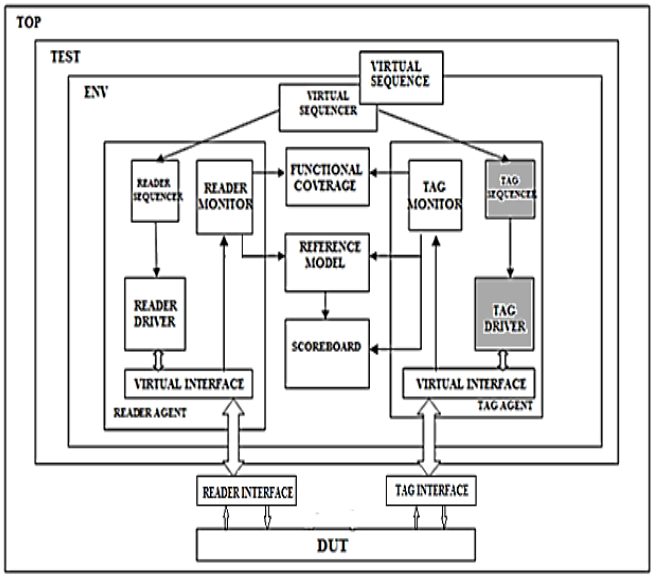

Fig 1: UVM architecture developed

The methodology used to develop the UVC is Universal Verification Methodology. The top block of the architecture shown in Fig 1 will generate instances of the test bench and the DUT. Two interfaces from the DUT; the tag interface and the reader interface. These act as a bridge between the two-corresponding tag and reader agents with the help of the virtual interfaces of the tag and the reader respectively. A sequence (test) is generated and run on the reader sequencer. The reader sequencer sends these transactions obtained from the sequence to the reader driver. The driver then pulls these transactions from the reader sequencer and transfers them repetitively to the signal-level interface (by converting them into pin wiggles) i.e. the DUT. The tag and reader monitors monitor these transactions. The packets from reader monitor (request) are then transferred to reference model where it formulates the response based on the request. Reference model is built based on the ISO/IEC 15693 standard and it is used as a reference against the DUT. Here, since we are verifying the tag, the tag driver and sequencer do not come into picture because the DUT is itself the tag that we are verifying. The packets observed by the tag monitor are transferred to the scoreboard. The response from the model once formulated is sent to the scoreboard. The scoreboard now compares both the tag and model response. If both the responses are the same then it gives a positive response otherwise it will give an error response. The output and inputs packets from the corresponding monitors are also transferred to a model that determines functional coverage. This model contains cover groups and cover points which gather coverage information related to which all functionalities are covered during a sequence.

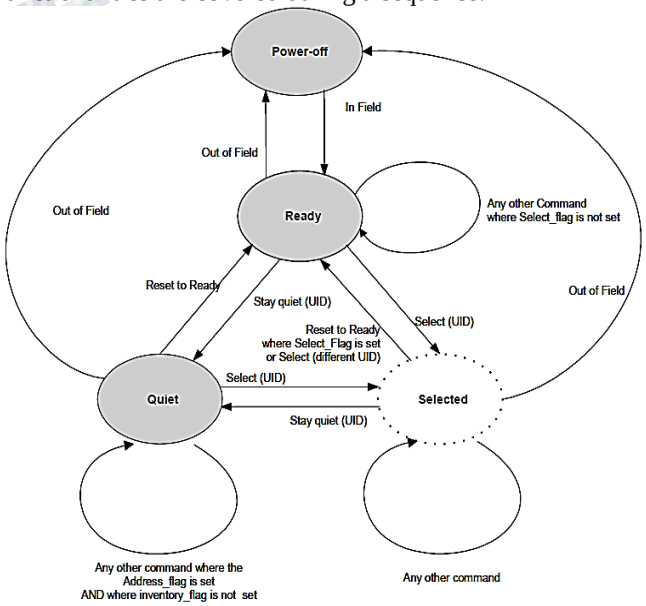

Fig 2: State diagram of the various modes of the tag

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The tag according to ISO/IEC 15693 standard can operate in three states as shown in Fig 2: Power off, ready and quiet state. There can be one more state which is optional called as selected state. Only one tag or the VICC (Vicinity Integrated Circuit Card) can be present in the selected state. When a request is sent to the card in the selected state, it need not contain the Unique ID but the select flag should be set high. Ready is like the default state. When a tag comes in the field of the reader it is in ready state. The tags present in Quiet state only answer to addressed requests. In the Power Off state the card is outside the field of the reader.

IV. RESULTS

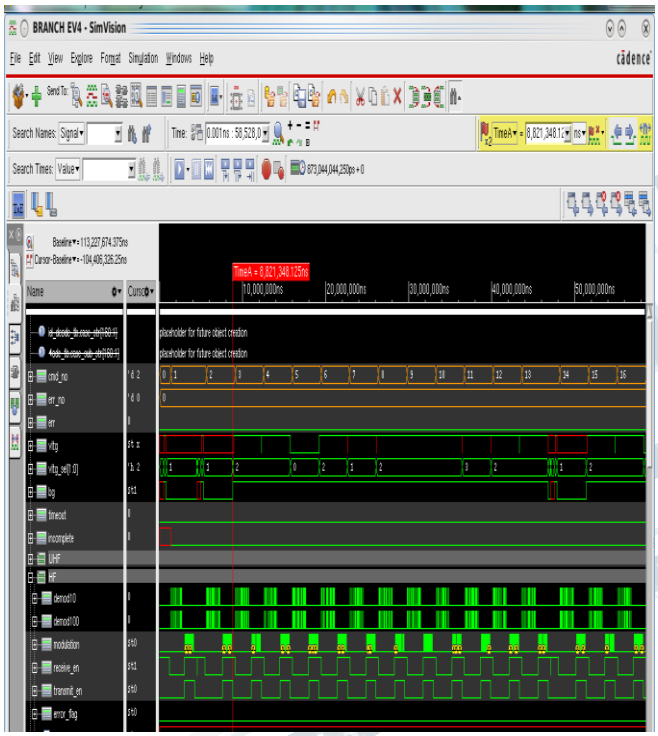

Fig 3: A Verilog testcase run on Ncsim

Some verilog testcases were written to verify the design during the initial stages. But these testcases could not cover much functionality since verilog is not a verification specific language. Thus, it does not support all the features that we need while verifying a design. The Fig 3 shows the modulation, demodulation and some of the voltage levels. This testcase was written to verify certain feature of a specific command.

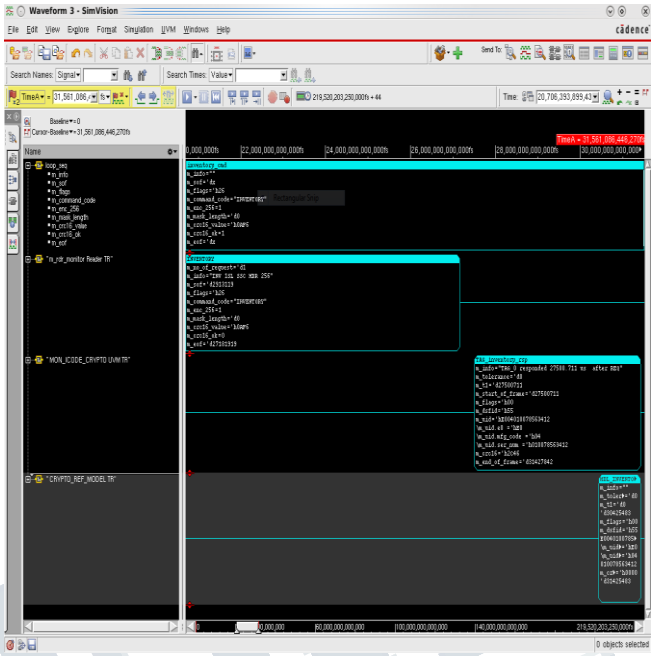

Fig 4: UVM sequence run on Ncsim

Many UVM sequences were written to verify the test bench architecture. Fig 4 shows the result of a UVM sequence run, in which one of the command sent was inventory. It describes the request sent to the tag, the reader monitor transactions, the tag monitor transactions and the response from the reference model respectively.

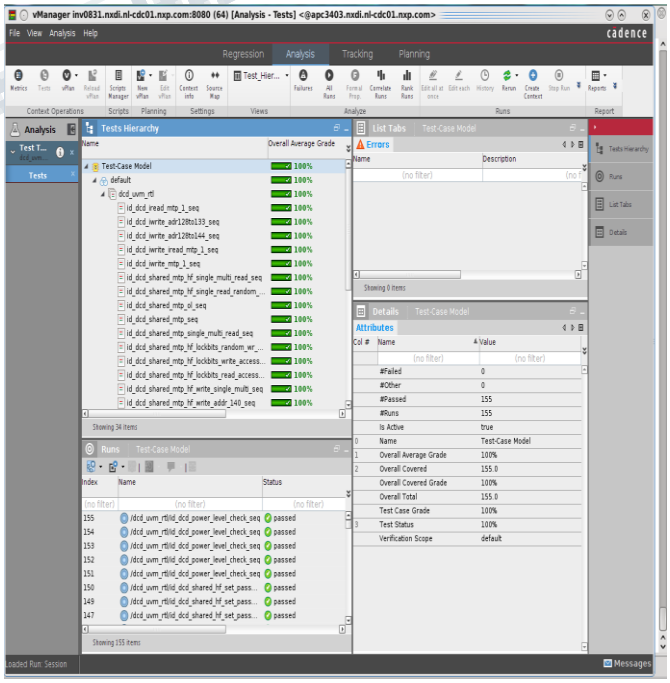

Fig 5: Regression run on vManager

Fig 5 shows the result of the regression of various sequences run on a tool called vManager. The regression consisted of various UVM sequences targeted to verify the design for various flag combinations, configurations, states, modes etc. Each sequence present in the regression was run multiple numbers of times with a random seed each time.

V. CONCLUSION

The increasing complexity of the modern designs and the resultant production prices explain the need for verifying the DUV efficiently. The design used in realizing this paper uses the ISO/IEC 15693 protocol which is a vicinity communication protocol for contactless cards, thus making it very intricate architecture. Verifying such a complex design by writing Verilog test bench programs consumes a lot of time and requires a lot more effort. This paper totally focuses on building an UVC component for NFC tags based on ISO/IEC 15693 protocol.
Universal Verification Methodology which was used for verification is the need of the hour. This methodology is usually compatible with any architecture; thus, making it easy for reuse and hence reducing the verification advancement environment effort. The usage of this methodology to verify the design resulted in increased performance. Every component of the UVM test bench architecture was built such that it can be reused to verify any SOC based on ISO/IEC protocol.

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