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A 12nm FinFET Level Shifter for near threshold circuits

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Abstract- **Power has turned into the essential plan imperative for chip designers today. While Moore's law perpetuates to provide additional transistors, power related constraints have started to preclude those devices from being utilized. These days, low power designs, particularly multi-voltage designs turn into a well-known and proficient approach to reduce both dynamic power and static power consumption. A key parameter in designing of effective multiple supply circuits is limiting the cost of the level transformation between diverse voltage domains while keeping up the overall robustness of the design. To such a reason, level shifter (LS) circuits can be used. In order to achieve reduction in power consumption, a proposed level shifter topology has been used in this paper which uses a low contention between PMOS and NMOS transistor due to which dynamic energy consumption is reduces, speed is also increased due to the use of a feedback loop and also due to the near-threshold computing its energy efficiency is more. As 12nm technology node delivers better density and a performance boost over Global Foundries' current-generation 14nm FinFET, which satisfies the processing needs of the most demanding compute-intensive applications from artificial intelligence and virtual reality to high-end smart-phones and networking infrastructure, the proposed level shifter has been scaled down to 12nm technology node which is capable of converting near-threshold voltage signal to above threshold voltage signal(i.e. from 250mV to 500mV) with 284.1229nW of power dissipation.**

Index Terms— FinFET's, level shifter, low power, near threshold.

I.INTRODUCTION

With the developing interest of handheld gadgets like mobile phones, mixed media gadgets, individual note pads and so on., low power consumption has turned out to be important design thought for VLSI circuits and systems. Power consumption in VLSI circuit comprises of dynamic and static power consumption[8]. Dynamic power has two segments i.e. switching power because of the charging and discharging of the load capacitance and the short circuit power because of non-zero rise and fall time of the input waveforms[8]. The static power of CMOS circuits is determined by the leakage current through each transistor. Power consumption of VLSI circuits can be reduced by scaling supply voltage and capacitance. With the decrease in supply voltage, issues of little voltage swing, leakage current etc. begins. With the advancement of innovation towards submicron region leakage power has turned out to be noteworthy part of aggregate power dissemination. Static power part of power consumption must be given due thought if current patterns of scaling of size and supply voltage should be sustained.

Fabrication of different components like analog, digital, passive component is done on a single chip in a system on chip(SoC) design which needs different voltages in order to achieve an optimum performance. The level shifters are acclimated to convert the logic signal or voltage from one voltage level to another and form the most consequential circuit component in VLSI systems. Level shifters are mainly used in some multi voltage systems and can be utilized in between core circuits and I/O circuit.

As of now, sundry level shifter designs have been proposed in recent years. Fundamentally the level shifter circuits can be predicated on following three approaches: (i) Differential cascade voltage switch(DCVS) level shifter, (ii) Wilson current mirror[3]-[4] and (iii) A specialized circuit topology used in [2].

A Differential cascode voltage switch (DCVS) logic is a CMOS circuit technique which has potential advantages over conventional NAND/NOR logic in terms of circuit delay, layout density, power dissipation, and logic flexibility[9].

The main focus of this brief is to have a power efficient level shifter topology which operates over a wide voltage range and fortifies voltages ranging from a low voltage VDDL near the threshold voltage i.e approx. 250mV to a high voltage VDDH i.e approx. 500mV.

A circuit topology of proposed level shifter from [1] has been scaled down to 12nm in this brief and has been simulated in Cadence virtuoso with Spectre Simulator for checking the level shifting of voltage from VDDL to VDDH.

The paper follows as: In section II, a concise explication of the circuit topology followed by engendering the symbol of the same at 12nm Channel Length of the FinFET has been described in section III. Later, in section IV the simulation result of the same has been briefed.

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II. PROPOSED WIDE VOLTAGE RANGE LEVEL SHIFTER FOR NEAR THRESHOLD CIRCUITS

The proposed level shifter is predicated on DCVS, homogeneous to the standard level shifting circuit depicted in Section II. Instead of than incrementing the size of the NMOS transistors, however, the proposed circuit dynamically transmutes the current sourced by the pertinent PMOS pull-up transistor (PL/PR) to ascertain that the impotent NMOS pull-down transistor (NL/NR) sinks more current than the PMOS pull-up (PL/PR) network sources. The proposed low voltage level shifter is as appeared in Fig. 1.

A. Structure of the Proposed Wide Voltage Range Level Shifter.

The oddity of this circuit topology is the feedback loop. The feedback loop comprises of a delay element that associates the output node D (high voltage domain) to the input of two multiplexers, MUXL and MUXR. The delay element is predicated on two least sized serially connected inverters. These inverters are provided with a high voltage (500 mV) and get a high voltage signal D as an input. This delay element does not influence the delay of the proposed level shifter, since the delay element is inside the feedback loop that sets up the circuit for the next transition. The MUXs are predicated on two sets of pass gates, as shown in Fig. 1. The output of MUXL (high voltage domain) is connected to the gate of the PMOS pull-up transistor PL. At the point when select is high (high voltage domain), the gate of PL is connected to the intermediate voltage Vddm, which ephemerally enervates PL[1]. At the point when select is low, the gate of PL is connected to node D, which preserves the differential operation. Likewise, the output of MUXR is connected to the gate of the PMOS pull-up transistor PR. At the point when select is high, the gate of PR is connected to node D, which preserves the differential operation. At the point when select is low, the gate of PR is connected to the intermediate voltage Vddm, which ephemerally emasculates PR. A case of this activity is portrayed in Section III-B.

This arrangements eliminates the desideratum for the immensely colossal NMOS pull-down transistors, NL and NR, because the germane PMOS pull-up transistor is kept up at a low voltage bias for the upcoming transition. This approach withal extraordinarily brings down the transition time as compared with other level shifters.

Symmetric activity of the proposed level shifter is safeguarded over the extreme operating range. Just a minor adjusting of the differential branches and the input inverter is required due to the low dispute between the pull-up PMOS transistors and the pull-down NMOS transistors. Amid the falling transition, the input signal proliferates through a skewed inverter with a wider PMOS transistor to limit the charge time of the NL gate. Node D is discharged with low conflict from PL, which expeditiously turns on PR (rather than a standard high dispute level shifter) to charge the output. Then again, the elevating input engenders a more expeditious transition, since the elevating input does not have an inversion delay.

This inversion delay is applied amid the elevating transition by sizing NR more minute than NL (to look after symmetry). Symmetric task of the proposed level shifter is shown generally while operating proximate to the extreme voltage range. With more diminutive voltage ranges (e.g., 0.5 to 0.79 V and less), the symmetry debases. The low conflict between PMOS what's more, NMOS transistors additionally contributes to the higher dynamic vitality efficiency of the proposed circuit as compared with the other level shifters.

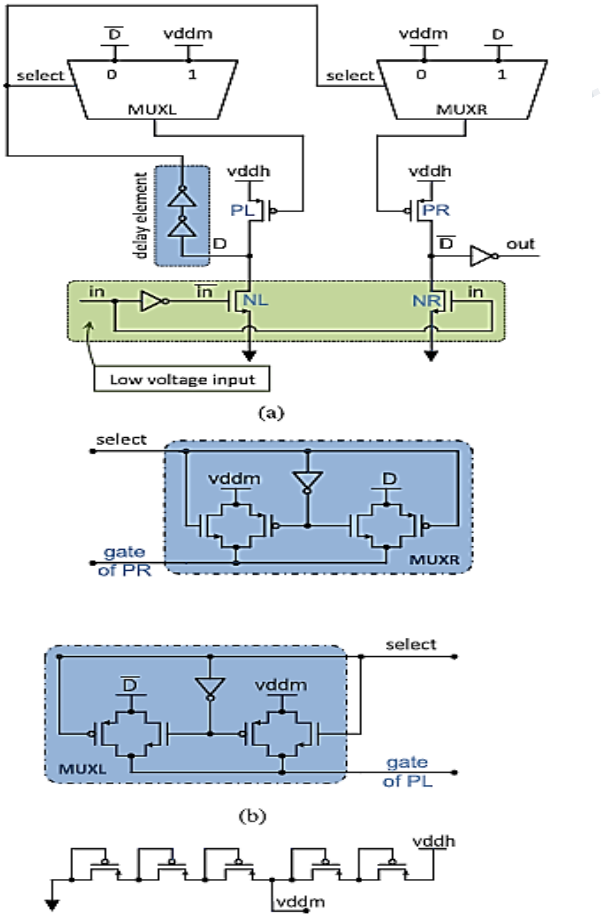

Fig. 1. Structure of the proposed wide voltage range level shifter, including

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(a) level shifter circuit, (b) internal MUX structures, and (c) intermediate
voltage generator.

The intermediate voltage Vddm is engendered by a voltage divider, as shown in Fig. 1, which comprises of five least sized diode connected PMOS transistors. In this setup, a stable partialness voltage of 350 mV is engendered to debilitate, as required, the pull-up PMOS transistors.

The area overhead is commensurable with the reference level shifters because of the more minute area of the pull-down NMOS transistors. While the additament of the MUXs, delay elements, and intermediate voltage engenderer presents supplemental transistors, this area is akin to the area required by the more intricate pull-up network of the reference level shifters.

As depicted in this section, the proposed level shifter displays higher performance as compared with the other level shifters.

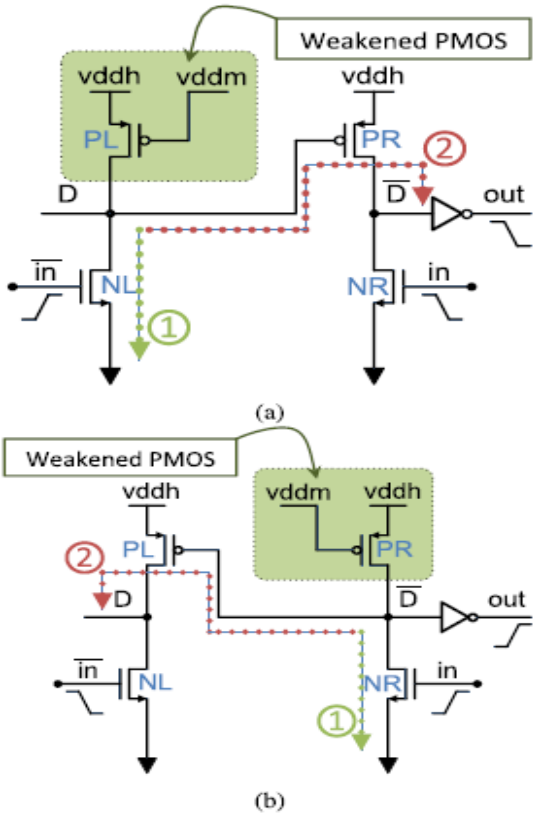

Fig. 2. Operation of proposed level shifter when (a) output is high and the

next transition is falling, and (b) output is low and the next transition is rising.

The haste amelioration is due to the feedback loop that sets up the circuit for the next transition. The dynamic vitality utilization is less because of the low dispute between the PMOS and NMOS transistors.

B. Case of Operation

The accompanying case is expected to further elucidate the previously mentioned circuit operation. Only two conceivable state change subsist for this level shifter, when the output is high and the following transition is falling, or when the output is low and the following transition is elevating.

1) For the main case, when the output is high, the following progress is falling transition is shown in Fig. 2. To setup this transition, the gate of PL is connected to the intermediate supply voltage Vddm and the gate of PR is connected to node D. This connection biases PL into the near cutoff region of operation, which degrades the drive vigor of PL. Without conflict from PL, as shown in the figure, node D discharges through the pull-down network NL. As shown in Fig. 2, node Db is charged to the full voltage by the pull-up network PR. After a delay, the feedback signal from node D propagates to the select input of MUXL and MUXR (the feedback path shown in Fig. 1), which is connected to the gate of PL and PR. This occasion establishes the state of the level shifter for the next transition.

2) The second case is introduced in Fig. 2. In this transition, the level shifter works similarly, as portrayed in the in the first case; in any case, every task is reflected to the other differential branch.. Node D is discharged through NR, while the current provided by transistor PR is less due to the intermediate supply voltage Vddm (connected to the gate of PR).

III. SIMULATED RESULTS

The circuits from Fig. 1 are scaled down to 12nm with reference to [5] and [6] for scaling from 16nm to 12nm is as follows: (i)With the help of a verilog-A coding, a 12nm FinFET symbol was generated, (ii)Basic components required for the proposed level shifter such as inverter, voltage divider and two multiplexers(MUXL and MUXR) were generated using 12nm FinFET's[7], and (iii)Finally, the level shifter circuit was constructed using the basic components as shown in Fig.4. This was launched with ADE L and simulated for DC analysis as shown in Fig. . From Fig.5., we can observe that the low input voltage was shifted from 250mV to 500mV. Fig.6. shows the power dissipation of Fig.1.a topology when simulated in Cadence Virtuoso at 12nm technology node which is 284.1229nW. This is around 23nW lesser compared with 16nm technology node topology from[1].

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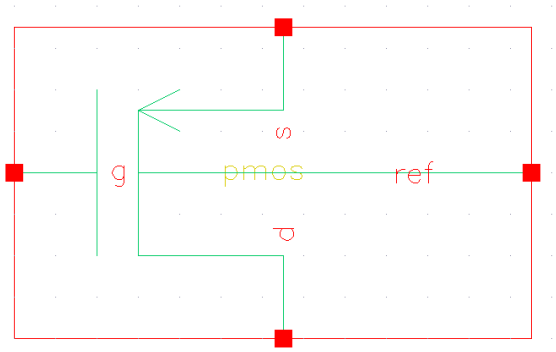

Fig.3. 12nm FinFET symbol generated using verilog-A coding.

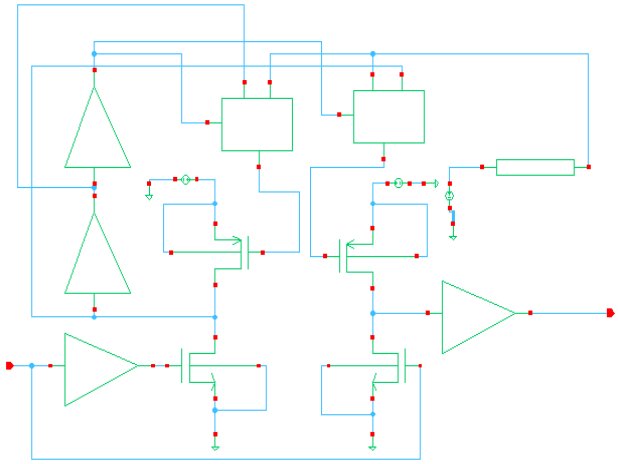

Fig.4. Level shifter circuit in Cadence Virtuoso for Fig.1a.

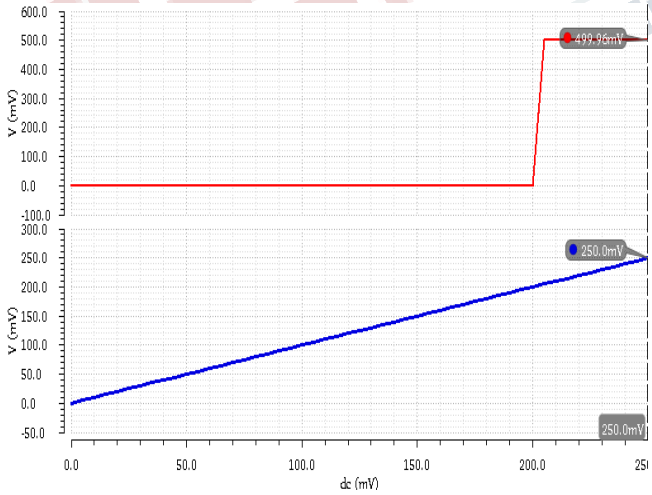

Fig.5. Simulated Output for level shifter of Fig.4. in Cadence Virtuoso Spectre simulator.

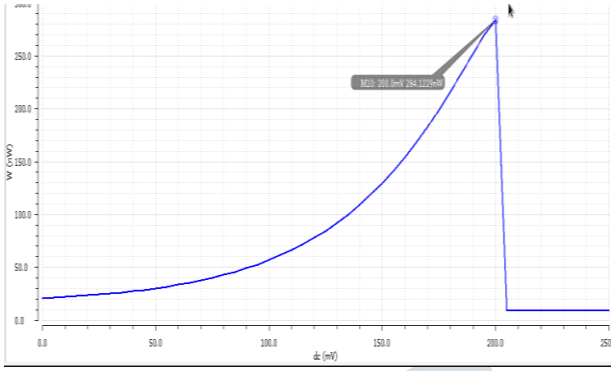

Fig.6. Power dissipation of Fig.1.a topology in Cadence Virtuoso.

Table I Comparison table for 16nm [1] and 12nm level shifter topology

Sl. No	Technology node	Level shifting		Power
		From	To	
1	16nm[1]	250mV	790mV	307nW
2	12nm	250mV	500mV	284.1229nW

IV. CONCLUSION

The proposed level shifter has appeared to be reasonable for coordination in sub-30-nm multi-voltage area microprocessors when scaled down to 12nm. The simulations show that the level shifter shifts the low input voltage domain from 250mV to 500mV with power dissipation of 284.1229nW(around 23nW less than the 16nm topology). The proposed converter, consequently, bolsters close edge circuits notwithstanding the expanded affectability to process varieties i.e The proposed converter, therefore, supports near threshold circuits despite the increased sensitivity to process variations.

V. FUTURE SCOPE

The converter must keep up symmetric rise and fall change times over the greatest voltage change at different temperatures. Also, the proposed converter must display critical enhancements in speed, vitality, and power proficiency.

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