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Implementation of Scan And Atpg Based Low Power Dft Techniques

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Abstract- **In contemporary era of technology, minimizing power consumption during functional as well as during testing has become one of the crucial requirements for semiconductor industries. Design-for-Testability (DFT) and low-power issues are greatly associated with each other. The trouble of test power reduction could be addressed at different stages of test-generation for logic designs. Switching activity reduction is the main area to concentrate on during low power testing. This paper provides comprehensive analysis on various novel low-power ATPG and DFT techniques such as Q-gating, EDT, X-filling techniques etc. Shift/Capture power as well as switching activities are calculated for these approaches on logic designs. By means of PowerArtist, a power analysis tool, power numbers are captured for these techniques and comparative analysis of results are made to find optimal techniques which could meet design specifications with not much loss of test and fault coverage. This paper reports on DFT methods which can aid for achieving comprehensive low power through commercial DFT tools in testing phase of VLSI design cycle.**

Index Terms— Automatic Test Pattern Generation- ATPG, Design-For-Test (DFT), Embedded Deterministic Test, Value Change Dump.

I.INTRODUCTION

Design-for-test(DFT) has become an inseparable consideration for testing microelectronic designs in this promising era of fast growing VLSI technologies, as it takes the significant responsibility in enhancement of the test quality and also in minimizing the test application time. DFT includes IC design practices which add testability features to the design so that it provides better access to internal circuit nodes such that internal states could be controlled (controllability) and/or observed (observability) easily. A thrust towards improved performance, tight integration, rigid timing constraints, low operating-voltages, portability, battery-based devices, and robustness with endurance for electronics has led to characterize power consumption, as a key metric in the design of Integrated circuits (IC). Test-power has become a serious bottleneck since excess power dissipation makes negative effect on reliability of the chip. Scan-based approaches of DFT cause rippling transitions all along the scan chains because of the shifting of the test patterns. Sometimes this would spuriously bring in huge switching activities inside combinational logic which may possibly create severe problems in Circuit-Under-Test. Hence test-power in DFT must be addressed at various stages of test generation, by employing power-aware test designs such as effective scan techniques, low-power automatic-test pattern-generation, test compaction, vector reordering, X-filling techniques and so on. A few methods based on scan and ATPG are implemented and impact on test-power is summarized and made a note of best possible
techniques which can be used in commercial tool based DFT flow in semiconductor industries. The real motivation for considering test-power as a prime factor in integrated circuits is because of the fact that, power consumption during testing will be greater than that of in functional [1] mode. Parallel testing in SOC to minimize test time and huge switching activity because of highly uncorrelated test vectors cause great power dissipation in testing stage which would lead to increased temperature and disproportionate current densities. Elevated power dissipation during testing may create structural damages (hot spots) to silicon, to the bonding wires, and to the package which can result in permanent damage to the Design-Under-Test. High-power values in testing can have an effect on the performance of the circuit and turns out in low reliability, high yield loss. Even packaging becomes cost intensive. In view of these factors it is necessary to adopt effective low-power techniques not just in functional mode but also in testmode. Structural testing which includes scan & ATPG stages is a complex field in which several significant factors such as test vector count, fault coverage, test time, flow modification must be considered carefully in addition to test-power reduction. Therefore, it is very necessary to assess and implement correct low-power test strategies to meet the power constraints in the design. Inserting scan chain alongside the combinational part and automatic-test-pattern-generation (ATPG) are some of the areas where low-power techniques can be adopted for DFT in digital circuits. Distinctive methods can be adopted for low-power designs.

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One such method is to insert test points to a subgroup of scan design elements to hold output of FF at a fixed value in shifting. Injecting control-0 &control-1 [6] test-points at the output of a mux-D scan portions. Set of scan chains are disabled with an extra disable pin [7] which will disable clock for subset of scan chains. When disable pin is activated, particular scan chains set is disabled with no clocking. This reduces switching activity and also clock power is minimized. Scan chain segmentation [21] is another move toward avoiding unnecessary toggling. Smart way of generating patterns in ATPG to achieve low power is great challenge. Some methods [8] take test sets and generate vectors of the same or lesser size with reduced switching activity without any alteration to the hardware. Selective [9] scan-chain reordering to reduce shift switching activities with minor flow constraints can also be adopted. Vector reordering needs scan chains to be reordered. A novel DFT compression architecture [11] Embedded Deterministic Test (EDT) helps reducing test data volume and test time by a great amount.

II. PROPOSED LOW POWER DFT METHODOLOGIES

Design-for-Test is performed to enable design for post-production testing. To reduce the switching activity during shift in DFT, automatic test pattern generation (ATPG)-based approach and DFT-based approach can be used. The main advantage of ATPG based solutions is that they do not alter the original design, but modification is made on test vectors and hence power cutback can be seen. DFT-based solutions either partition the conventional scan chains architecture or inserts extra hardware into the design. This paper gives an insight on implementation of new techniques such as Q-gating, X-filling, EDT adaptations, and thresholds setting for shift/capture operations. Analysis on these techniques is made taking industry standard approaches into account.

A. Q-gating

This method involves logics to be inserted to hold the outputs of selected scan cells at constant values during scan shifting thereby preventing switching activity in the combinational portion of the DUT. This minimizes the average scan shift power, and also avoids peak power hazards during scan shifting. Thus gating or blocking the Q output values of D-FF to the combinational blocks of the design during scan shifting is termed as Q-gating. The scan cell modification consists of adding an extra gate such as OR gate, AND gate, NOR gate or MUX. Two implementations of gating the scan cell output to be 0 and 1 are shown where AND gate or an OR gate is included for blocking. By asserting Block_Enable signal, the transition occurred in the scan cells is blocked. During normal operation, this signal is de-asserted. To reduce the area overhead due to additional gates, care must be taken to Q-gate for the selective cells only. Q –gating is implemented by inverting shift enable pin and taking it as control signal for the AND gate. When shift enable is high during scan, AND gate is disabled and changes in Q value is blocked to 0 and thus value is gated to propagate into the combinational block. The shift path is unaffected as shift output is directly taken from the Q without gating it. Gating was done selectively on few cells which have more toggling to reduce area overhead.

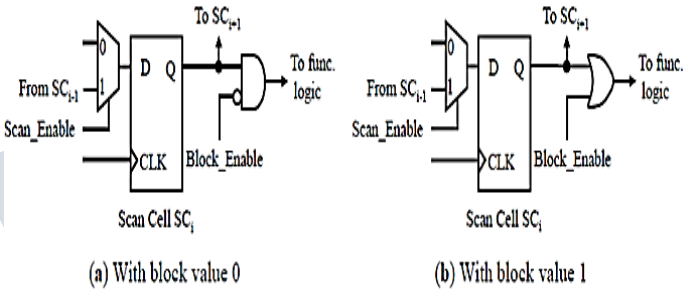

Figure 1: Different Q-gating Structures

B. X-fill Strategies

The technique that can be used to reduce test power is to make use of power-aware X-filling heuristics that do not modify the overall ATPG process. For a known set of deterministic test cubes, the primary goal of these techniques is to assign values to the don't care bits of each test cube so that the number of transitions in the scan cells is reduced. Minimized number of transitions in the scan cells during scan shifting reduces overall switching activity in the DUT. Thus power consumption during test is diminished. The majority of the time, X's are assigned with the help of the following classical non-random filling heuristics:

♦ Minimum transition filling (MT-filling), also called Adjacent filling: The don't care bits in a test cube are assigned with the value of the last encountered care bit. That is, when applying MT-filling, the most recent care bit value is used to fill successive X values until a care bit is reached.

♦ 0-filling: All don't care bits in a pattern are set to '0'.

♦ 1-filling: The don't care bits in patterns are set with '1'.

MT-filling results in the fewest number of transitions in the scan chains which generally correspond to the lowest switching activity in the overall circuit, and are thus the preferred approach. Consider the test cube <0XXX01XX0XX0XX1>. By applying the above three non-random filling heuristics, the resulting patterns become:

♦ 000001110000001 with MT-filling heuristics.

♦ 000001000000001 with 0-filling heuristics.

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♦ 011101110110111 with 1-filling heuristics

The ATPG flow followed is depicted in the figure 2. Compared to other methods, X-filling techniques have an added advantage of being applicable at the end of the design process without imposing any impact on the design flow and also do not need any modification to the circuit such that it does not incur any area overhead. These methods lessen test power but sometimes at the cost of increased pattern count due to the fact that they may not be effective in detecting additional faults as random filling there by requiring incrementally additional patterns to attain the target fault coverage.

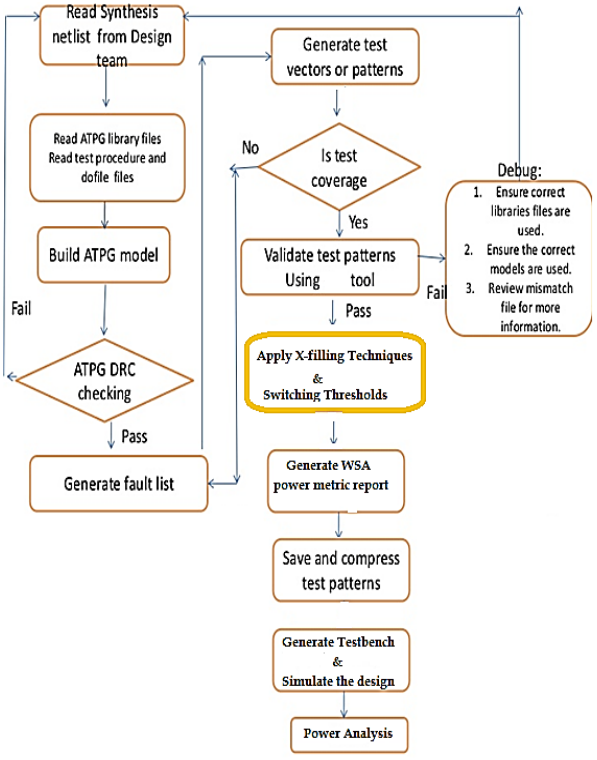

Figure 2: Automatic Test Pattern Generation Flow

C. Low Power Embedded Deterministic test

The Embedded Deterministic Test structure consists of logic which is embedded on a chip with a new technique for deterministic test pattern generation. The EDT logic is inserted along the scan path but outside the design core, and consists of two main blocks as shown in Figure 3.On-chip decompressor is sited between the external and internal scan channel inputs. On-chip selective compactor between the internal scan chain outputs and the external scan channel outputs is inserted. Optionally, the EDT architecture may include logic to bypass the decompressor and the compactor, thus make the internal scan chains directly accessible from the Automatic Test Equipment. EDT is mainly used for its benefits like lesser data test volume, less test time and memory, and less number of external IC pins etc.

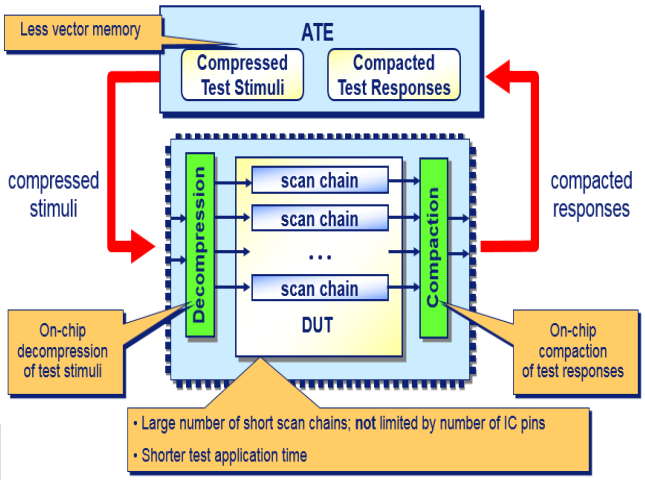

Figure 3: General EDT structure

The modification of EDT for low power is generated using Power controller. An additional test pattern (edt_setup) is added for every test pattern set. This will sets up the low-power mask registers before the load of the every first real test pattern. The power controller logic is configured or inserted during EDT logic creation based on the – Minimum Switching threshold percentage value specified in edt power controller. For example suppose for 40% threshold, if we have 300 scan chains, the maximum percentage of scan chains that will switch is 120, which is 40% of 300.The switching threshold can also be set for the shift and capture procedure so as the patterns contain only specified number of transitions to reduce toggling. This way of modifying EDT has great impact on power and has only less hardware modification. Switching threshold percentage value specified in edt power controller. For example suppose for 40% threshold, if we have 300 scan chains, the maximum percentage of scan chains that will switch is 120, which is 40% of 300.The switching threshold can also be set for the shift and capture procedure so as the patterns contain only specified number of transitions to reduce toggling. This way of modifying EDT has great impact on power and has only less hardware modification.

III. EXPERIMENTAL RESULTS

The Q-gating and X-filling techniques was applied on the design having nearly hundreds of scan-DFF and Low Power EDT was implemented for a design having around lakhs of gates count. The above methods are implemented using

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cadence Genus tool for Scan insertion and Mentor Graphic'sTessent Shell for ATPG and Ansys PowerArtist tool for power estimation. Q-gating results are simulated with cadence simvision and we can observe that there is reduced toggling in the specified scan cells outputs. One scan cell output is highlighted in the figure 4 with reduced switching activity.

Table 1.Comparison Table

	Total Power(Shift)	Total Power(Capture)	Coverage(%)	Pattern_Count	No of Gates
Original Design	42.6uW	47.3uW	93.62	147	3332
0-fill Technique	40.8uW	45uW	93.62	147	3332
1-fill Technique	40.79uW	41.3uW	93.62	147	3332
Q-gating	40.9uW	42.4uW	93.58	141	3343

Testbenches are generated for X-filling techniques and waveforms are dumped and Value Change Dump (VCD) file is generated that includes toggling activities data which is fed to the PowerArtist tool for power calculation. Based on the shift and capture timings specified, power values for different operations can be found.

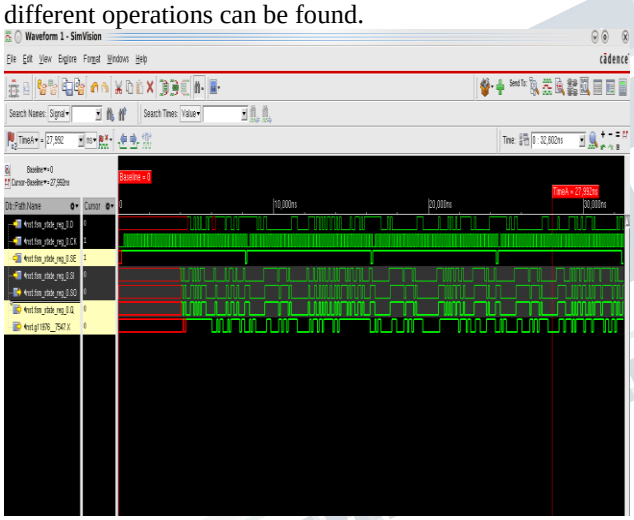

Figure 4(a): Without Q-gating

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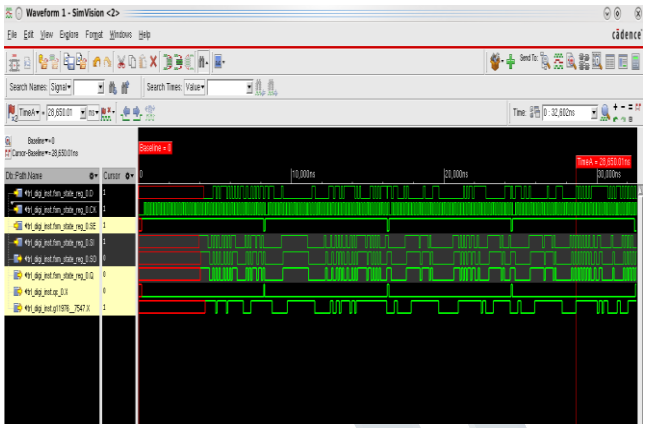

Figure 4(b): Reduced activity With Q-gating technique.

Comparison of different X-fill techniques and shift/capture thresholds are tabulated, Table 1.Note X-fill techniques basically account for shift power and not capture power. Low Power EDT was modeled for Stuck at faults was simulated and coverage report was analyzed to meet the required coverage. Number of Faults detected and pattern count, coverage was resulted in below figure. Faults coverage of around 98% was maintained. Results showing comparison with and without LP-EDT is shown in figure 5 (a) and (b).

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1. Total power consumption
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                                          Power(Watts)
Power contribution                  Static  Dynamic    Total
----- ------------                  ------  -------    -----
Internal power                      4.29mW  4.78mW   9.08mW
   Internal register power          5.82uW  27.3uW   33.1uW
   Internal latch power                 0W      0W       0W
   Internal memory power            2.61mW  4.47mW   7.09mW
   Other internal power
   Total internal power             6.91mW  9.28mW   16.2mW
Pad power                               0W      0W       0W
Clock power                         27.9uW   194uW    222uW

Total power                         6.94mW  9.48mW   16.4mW
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Figure 5: (a) Without LP_EDT

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1. Total power consumption

Power contribution	Power(Watts) Static	Dynamic	Total
Internal power			
Internal register power	3.73mW	1.9mW	5.63mW
Internal latch power	4.67uW	7.86uW	12.5uW
Internal memory power	0W	0W	0W
Other internal power	2.42mW	487uW	2.9mW
Total internal power	6.15mW	2.4mW	8.55mW
Pad power	0W	0W	0W
Clock power	27.9uW	195uW	223uW
Total power	6.18mW	2.59mW	8.77mW

(b) With LP_EDT

IV.CONCLUSION

Of the various heuristics that could be considered practical, X-fill techniques seem to hold decent promise on lowering switching activity while keeping pattern count in check i.e. not much increase in pattern count. The proposed X-fill technique requires no additional hardware overhead for the circuit-under-test. One more method which is for used for Low-power is enabling low-power EDT which has shown to reduce around 40-50% of power during test but at the cost of slight increase in pattern count and modification to the hardware. And Q-gating method which is implemented to block switching activity in combinational part of the design during shift shows to reduce toggling activity and thus lessen the shift power. But the challenge that remains here is to identify selective scan-cells for q-gating so that there is less area overhead. Minimum switching thresholds set for shift and capture can also reduce the power to great extent but with the tradeoff between patterns count and toggling activity. All these methods if implemented in combined form in an effective way would lead to great power reduction during testing.

REFERENCES

1. K. M. Butler, J. Saxena; A. Jain; T. Fryars; J. Lewis; G. Hetherington, "Minimizing Power Consumption in scan testing: pattern generation and DFT techniques", International Conference on Test, 2004.

2. BrionKeller; TomJackson, AnisUzzaman,"A Review of Power Strategies for DFT and ATPG", 16th Asian Test Symposium", IEEE Conference Publications,2007.

3. Hossein Sabaghian- Bidgoli, Majid shtari, Zainalabedin Navabi, "A Probabilistic and Constraint Based Approach for Low Power Test Generation", IEEE 21st Asian Test Symposium, 2012.

4. E.Corno, P.Prinetto, M.Rebaudengo; M. S. Reorda, "A test pattern generation methodology for low power consumption", 16th IEEE VLSI Test Symposium (Cat. No.98TB100231), 1998.

5. R.Sankaralingam, N.A.Touba,"Inserting test points to control peak power during scan testing", 17th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems, DFT Proceedings.,2002.

6. R.Sankaralingam, N.ATouba,"Reducing test power during test using programmable scanchain disable Electronic Design, Test and Applications", 2002. Proceedings. The First IEEE International Workshop on Year, 2002.

7. M.Hirech; J. Beausang; Xinli GU, "A new approach to scan chain reordering using physical design information", Proceedings International Test Conference, 1998.

8. ShrayKhullar,SwapnilBahl,"Power Aware Shift and Capture ATPG Methodology for low Power Designs ",Asian Test Symposium, IEEE conference,2011.

9. Lung Jung-Jen Lee, Chia-Cheng He, Wang-Dauh Tseng," Deterministic ATPG for Low Capture Power Testing", 2012 13th International Workshop on Microprocessor Test and Verification (MTV) .

10. Yu Huang, Mark Kasab, Jay Jahangiri, Janusz Rajski, Wu-Tung Cheng, Dong kwan Han ,Chung" Test Compression Improvement with EDT Channel Sharing in SoC Designs", IEEE 23rd North Atlantic Test Workshop, 2014.

11. D. Czysz, M. Kassab, X. Lin, G. Mrugalski, J. Rajski, J.Tyszer,"Low Power Scan Shift and Capture in the the EDT Environment," IEEE International Test Conference, 2008.

12. JakubJanicki, MarkKassab, Grzegorz rugalski, NilanjaMukherjee, JanuszRajski, Jerzy"EDT Bandwidth Management in SoC Designs",IEE

E Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012

13. S. Chen, B. Mulgrew, and P. M. Grant, "A clustering technique for digital communications channel equalization using radial basis function networks," IEEE Trans. on Neural Networks, vol. 4, pp. 570-578, July 1993.

14. J. U. Duncombe, "Infrared navigation—Part I: An assessment of feasibility," IEEE Trans. Electron Devices, vol. ED-11, pp. 34-39, Jan. 1959.

15. C. Y. Lin, M. Wu, J. A. Bloom, I. J. Cox, and M. Miller, "Rotation, scale, and translation resilient public watermarking for images," IEEE Trans. Image Process., vol. 10, no. 5, pp. 767-782, May 2001s