ISSN (Online) 2394-2320

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)

Volume 7, Issue 5, May 2020

Design of XOR/XNOR circuits for Hybrid Full Adder

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***Abstract:*-- Increased usage of battery-operated compact devices such as notebooks, Smart phones, e-readers, MP3 players and many other devices are designed with built-in storage, smaller silicon area, longer battery life, higher speed and more reliability. Full adder is being dominant block in arithmetic operations. The main block of the full adder circuit is the XOR/XNOR gate, as the XOR/XNOR gate consumes more power. The power consumed by the full adder is therefore reduced by optimizing the design of the XOR / XNOR gates. These can be used in a variety of multipliers, such as Vedic, Wallace, Array, etc. Simulation results are performed in Cadence Virtuoso tool 45-nm CMOS technology with 0.45V supply voltage. The novel structures of XOR / XNOR gate are proposed for the design of hybrid full adders with low power, high speed and less PDP. The proposed HFA-14T has superior speed against other full adder cells with less number of transistors. Therefore, Area of the proposed HFA's is also reduced.**

Index Terms:- full ladder, hybrid full adder, low power, XOR/XNOR circuits.

INTRODUCTION

In Contemporary days, increased usage of battery-operated compact devices like notebooks, Smart phones, e-readers, MP3 players and any other devices with inbuilt accessible storage with surpassed power- delay characteristics. The dictate and vogue of compact devices is driving designers to endeavor for smaller silicon area, longer battery life, higher speed and more reliability. These compact devices comprise large part of digital circuits. Efficiency of many digital applications appertains to performance of arithmetic circuits like adders, multipliers, MAC unit. Due to primordial role of addition in all the arithmetic operations, full adder being most dominant block in arithmetic operations and many efforts have been made to explore efficient adder structures. Full adder is being most crucial block of researchers for years. Over last decade, many full adders with different logic styles, with excellence and dereliction, have been implemented. Present day ever-increasing number of compact applications requires low power. Power is one of the superior assets a designer tries to rescue when designing a system. Each full adder circuit has its own excellence regarding speed, power consumption, PDP (power delay product). PDP exhibited by full adder would affect the system's overall performance. The main block of the full adder circuit is XOR/ XNOR gate, because XOR/ XNOR gate consumes more power. So, the power consumed by the full adder is reduced by optimum design of XOR/ XNOR gates. These can be used in a variety of multipliers, such as Vedic, Wallace, Array, etc. When more than one logic style, are used for their implementation, this is called as hybrid CMOS logic style[1]. Examples of such design are hybrid pass logic with static CMOS[2] (HPSC), NEW-14T. Such designs take advantage of the features of various logic styles [3][4][5][6][7] to enhance the efficiency of the designs using a single logic type. All hybrid designs use the best possible modules implemented using different logic types or improve the available modules in an attempt to create a low power full adder cell. Generally the main pivot in such efforts is to diminish the number of transistors in adder cell and inevitably diminishing the number of power dissipating nodes. Many circuits have been implemented XOR/ XNOR designs or simultaneous XOR- XNOR designs, with some of the most successful examples are DPL XOR/ XNOR gate[8], PTL XOR/ XNOR gate[1], CPL XOR-XNOR gate[8], Goel's XOR- XNOR gate[9], Radhakrishnan's XOR- XNOR gate[10], Chang et al' s XOR- XNOR gate[11], M. A. Valashani's XOR- XNOR gate[12], H. Naseri's[1] XOR/ XNOR gate and XOR- XNOR

ISSN (Online) 2456-1290

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)

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gate. A variety of Hybrid Full Adder[1] designs have been introduced, with some of the most successful examples being HFA-20T, HFA-17T, HFA-B-26T, HFA-NB-26T, HFA-22T and HFA-19T.

In this paper, several circuits for the XOR/ XNOR and simultaneous XOR-XNOR gates are evaluated and new circuits are offered. All the circuits have been simulated and power, delay and PDP values are calculated for the comparison. Among these, efficient XOR/ XNOR gate is further used to offer new low-power hybrid full adder. Proposed XOR/ XNOR gate is efficient in terms of high speed and less PDP. It is further used to design high speed and low PDP hybrid full adder.

The remaining chapters of the paper are structured as follows: Section II mentions the proposed XOR- XNOR gate and two novel hybrid full adder circuits. Section III briefs on simulation results of proposed XOR- XNOR gate and hybrid full adders. Section IV shall conclude this paper.

NOVEL XOR- XNOR AND FULL ADDER DESIGNS

XOR- XNOR circuit operation and analysis

The proposed simultaneous XOR - XNOR gate is composed of 6 transistors and shown in Fig. 1. In this circuit, Q1, Q2 are PMOS transistors and Q3, Q5 are NMOS transistors. XOR output is inverted by a static CMOS inverter that produces XNOR output.

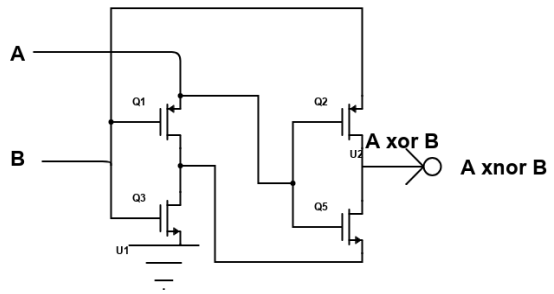

Fig. 1 Proposed XOR- XNOR gate

Truth table

Table I Truth table of proposed XOR- XNOR gate

A	B	Q1	Q2	Q3	Q5	XOR	XNOR
0	0	ON	ON	OFF	OFF	Weak 0	1
0	1	ON	ON	ON	OFF	1	0
1	0	OFF	OFF	OFF	High-Z	Weak 1	0
1	1	OFF	OFF	ON	ON	0	1

When AB=00, Q1, Q2 turns on, Q3 turns off, there is no GND path. Q5 is turning off. As Q2 turns on, Q2 (PMOS) turns weak 0 to XOR output. By static CMOS inverter, weak 0 is inverted to strong 1; logical 1 is achieved at XNOR output. When AB=01, Q1, Q2, Q3 turns on, there is a GND path.Q5 turns off. Since Q2 switches on, VDD passes to XOR output. The static CMOS inverter inverts logic 1 to 0 and the logic 0 are generated at the XNOR output. As AB= 10, Q1, Q2, Q3 turns off, Q5 turns on, but Q5 is at high impedance. Due to parasitic capacitance, Q5 (NMOS) produces weak 1 so there is a slight voltage swing reduction at XOR output. But this weak 1 is inverted to a strong 0 by a static CMOS inverter. Logic 0 is therefore obtained from the XNOR output. And if AB=11, Q1,Q2 Turns off, Q3 Turns on, there is a path from GND, Q5 Turns on, and logic 0 Turns on to XOR output. The output of XNOR is inverted XOR output i.e., logic 1 is obtained at the output of XNOR.

The results show that the performance of this XOR- XNOR gate in terms of low power and low PDP is better than that of the compared structures. This gate is also used for developing low power, high speed and low PDP hybrid full adder.

Novel full adders

These new full adders have been used in a hybrid logic style and are both designed using the above XOR- XNOR circuits. The well-known 4 transistor 2-1 MUX gate are used to implement the proposed hybrid full adder cells. This 2-1 MUX is generated in TG logic form, without dissipation of static and short circuit power.

1. HFA-14T-1

The novel hybrid full adder, consisting of 14 transistors and shown in Fig. 2. This full adder consists of two 2-1 MUX gates and the Radhakrishnan's XOR- XNOR gate[10]. This is a full-swing XOR- XNOR gate with only six transistors and it is low- power XOR- XNOR gate. The XOR- XNOR signals are connected to the inputs of 2:1 MUX as select lines.

ISSN (Online) 2456-1290

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)

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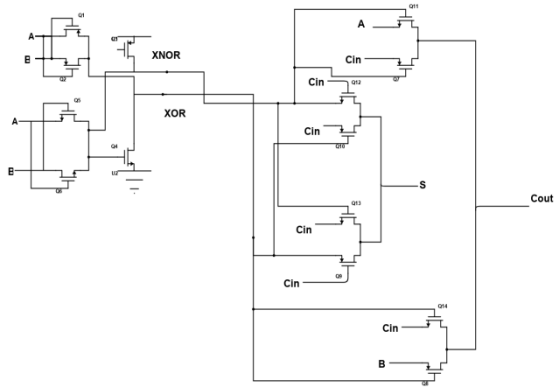

Fig. 2 novel hybrid full adder-1

This XOR- XNOR gate is designed with an additional feedback structure. Here A, B, Cin are the inputs that add three input numbers and generate Sum and carry i.e. S and $Cout$. The output S is an EX- OR between the input A and the half adder SUM output B. The $Cout$ will be high only if any of the 2 inputs out of 3 are high or at logic 1. Since there is a slow response problem in the XOR-XNOR gate of Radhakrishnan when input passes from 10 to 00, there is also a slow response problem in this proposed hybrid full adder when input passes from 100 to 000. However, the results show that, in terms of low-power, the performance of this full adder is better than that of the comparable structures, and the novel hybrid full adder also has less number of transistors than all the other comparable structures. The advantages of this structure are full swing performance, dissipation with low power.

2. HFA-14T-2

Another possible hybrid full adder consists of 14 transistors and shown in Fig. 3. This HFA consists of novel XOR-XNOR gate and two 2:1 MUX gates. The new XOR-XNOR gate is made of 6 transistors. This XOR-XNOR gate decreases the voltage swing from 10 to 00, but it is a low-power XOR-XNOR gate. This voltage swing reduction also reduces the voltage swing when used in full adder from 100 to 000 inputs.

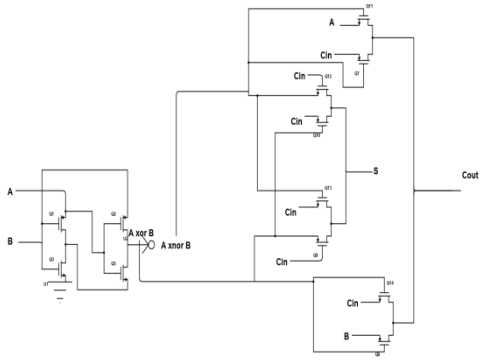

Fig. 3 proposed hybrid full adder-2

This is hybrid full adder featuring hybrid logic designs. The inputs here are A, B,Cin which adds three input numbers to produce Sum and carry signals. This full adder has the advantages of low power, high speed and low PDP with less number of transistors.

Table II Comparison of XOR/ XNOR designs

The results show that the performance of this full adder is better than that of the comparative structures with regard to low power, high speed and low PDP.

SIMULATION RESULTS

The simulation results are based on the standard 45-nm CMOS technology, cadence software virtuoso tool with 0.45V voltage power supply. The values of delay are considered at critical circuit paths. The PDP is determined by multiplying the power and the delay values at the circuit's critical paths.

Novel XOR- XNOR gate

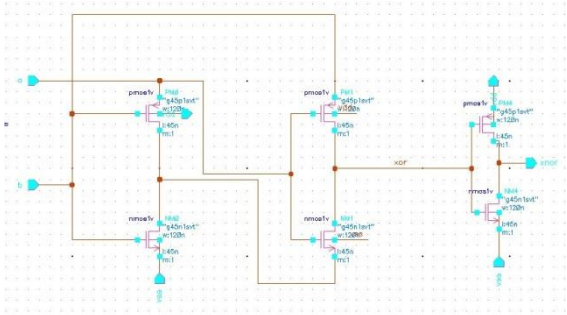

Fig. 4 novel XOR- XNOR gate schematic

ISSN (Online) 2456-1290

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)

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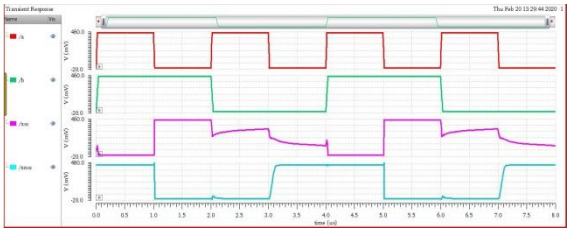

Fig. 5 novel XOR- XNOR gate output

Novel hybrid full adders

1. *HFA-14T-1*

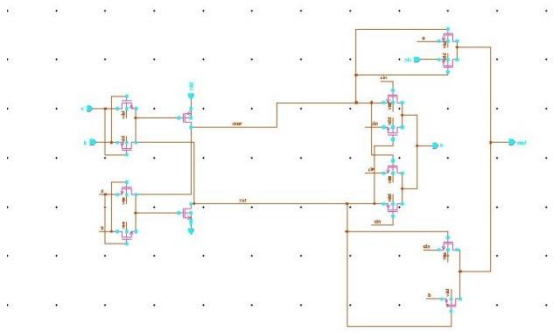

Fig. 6 proposed HFA-1 schematic

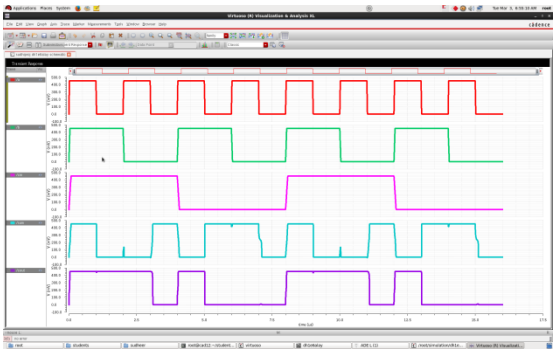

Fig. 7 proposed HFA-1 output

2. *HFA-14T-2*

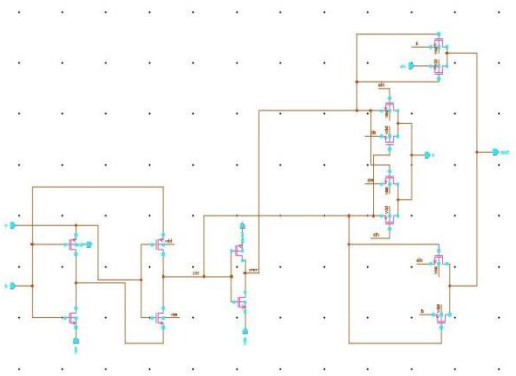

Fig. 8 novel HFA-2 schematic

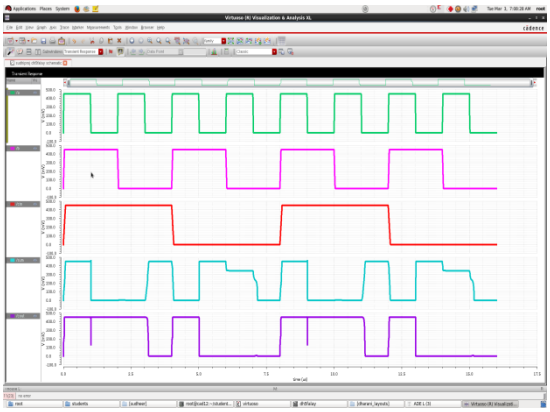

Fig. 9 novel HFA-2 output

XOR/XNOR design	No. of transistors	Power (nW)	Delay (ns)	PDP (nJ)
DPL	12	0.128	2009	257.15
PTL	10	0.086	3008	258.6
CPL	10	0.108	3009	324.9
Goel	8	3.344	3145	10516
Radhakrishnan	6	0.062	3013	186.8
Chang et al's	10	0.088	3010	264.8
M.A.valashani	10	0.114	3010	343.1
H. Naseri's	12	0.080	3007	240.5
H. Naseri's XOR-XNOR	12	0.081	3007	243.5
Novel XOR-XNOR	6	0.070	3026	211.8

ISSN (Online) 2456-1290

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C. Layout of new full adders

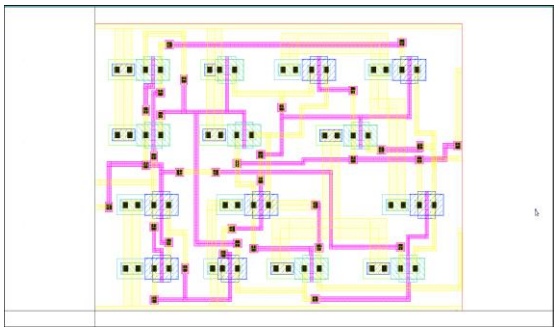


Fig. 10 Circuit layout of HFA- 14T-1

Therefore, the occupied area of proposed HFA- 14T-1 is 17.41545μm^2

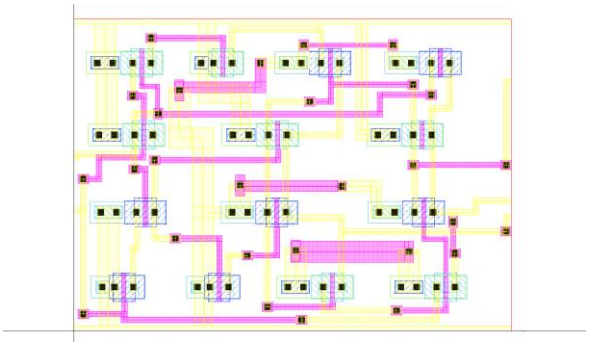


Fig. 11 Circuit layout of HFA- 14T-2

Therefore, the occupied area of proposed HFA- 14T-2 is 16.8989μm^2.

Table II shows, Comparison of Existing XOR/ XNOR designs with novel XOR- XNOR design i.e., Radhakrishnan' s XOR- XNOR design and proposed XOR- XNOR design, with less transistor numbers, have less power than the other structures compared. The results indicate therefore that the efficiency of the proposed XOR- XNOR gate is better than that of the comparative structures. Those XOR- XNOR gates are also included in the proposed full adder.

Table III shows, comparison of full adder designs with new Full adder i.e., HFA-14T-1 and HFA-14T-2 indicate less transistor counts than other Full adders compared. HFA-14T-1 has less power and HFA-14T-2 has less power, high speed and low PDP. Consequently, the results indicate that the performance of proposed Full adders is better than that of comparative structures.

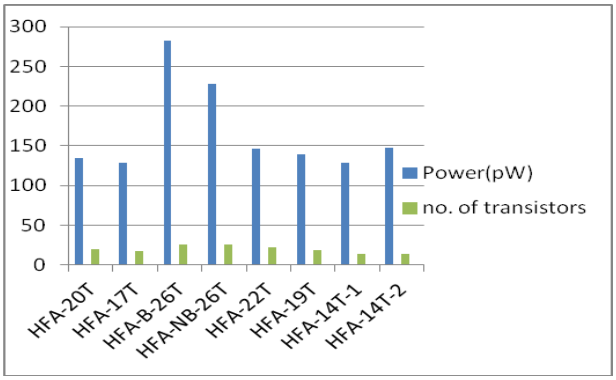
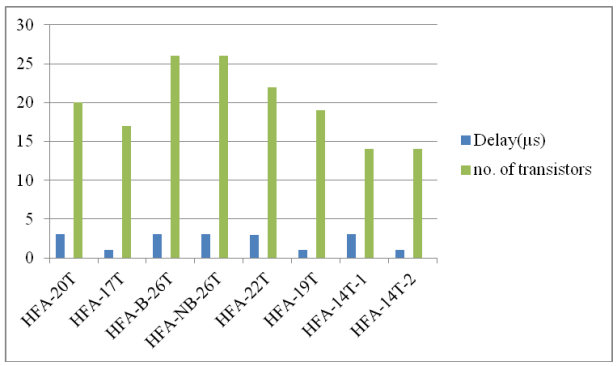


Fig. 12 simulation results: No. of transistors vs. Power

From fig. 12, HFA-17T and HFA-14T-1 have less power among all the compared structures with the new full adder structure, but HFA-14T-1 has less transistor number than HFA-17T. The findings show that in terms of power, HFA-14T-1 is better than any other comparable framework.

Table III Comparison of Full Adder designs

Full adders	No. of transistors	Power (nW)	Delay (ns)	PDP (nJ)
HFA-20T	20	0.134	3010	403.3
HFA-17T	17	0.129	1011	130.4
HFA-B-26T	26	0.283	3012	852.3
HFA-NB-26T	26	0.228	3010	686.2
HFA-22T	22	0.146	3000	438
HFA-19T	19	0.139	1010	140.3
HFA-14T-1	14	0.129	3087	398.2
HFA-14T-2	14	0.147	1011	148.6



ISSN (Online) 2456-1290

International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE)

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Fig. 13 simulation results: No. of transistors vs. delay

From fig. 13, Among all the structures compared with the proposed full adder structure, HFA-17T, HFA-19T and HFA-14T-2 have less delay, but HFA-14T-2 has less transistor number than both. The findings suggest that HFA-14T-2 is better than all other comparable constructs in terms of delay. HFA-14T-2 thus has a superior speed than other comparable frameworks.

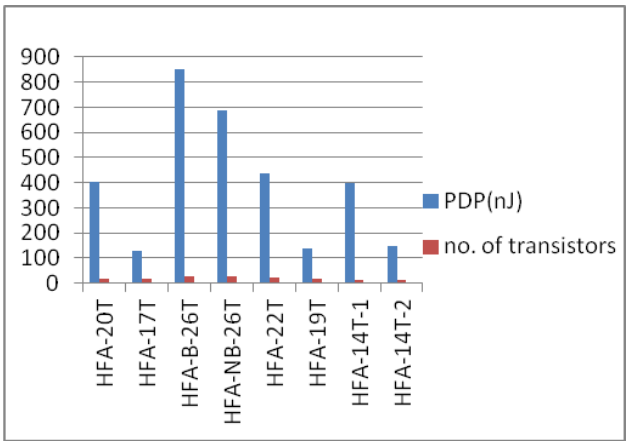

Fig. 14 simulation results: No. of transistors vs. PDP

From fig, 14, Among all the compared structures with the proposed full adder structure, HFA-17T, HFA-19T and HFA-14T-2 have low PDP but HFA-14T-2 has less transistor in number than both. The results show that HFA-14T-2 is better than all other comparative structures in terms of PDP.

From the above results, HFA-14T-2 has low power; high speed and higher PDP with lower transistor number and HFA-14T-1 has low power with lower transistor number. Consequently, the results indicate that the performance of proposed full adders is better than that of comparative structures and also, as the number of transistors is reduced, the Area of the proposed hybrid full adders is also reduced.

CONCLUSION

In this paper, several XOR/ XNOR and XOR- XNOR circuits are evaluated. If the more of the transistor number, the more power and delay, the more of the dereliction So, XOR / XNOR gate with less transistor number ensuring less power, delay and PDP is proposed. Finally two new Full hybrid adders using this latest XOR- XNOR gates are introduced. These two hybrid full adders have fewer transistors than full adder structures compared. Consequently, the results indicate that the performance of proposed hybrid full adders is better than that of comparative structures.

Simulation results show that, compared to its best equivalent, the proposed HFA- 14T-2 cell saves PDP up to 82.56%, respectively. This cell also saves up to 66% delay and 48.05% power as compared to other full adders. The proposed HFA-14T-1 cell also saves up to 54.4% power over its strongest counterpart, respectively. The proposed HFA-14T-1 has superior speed compared to other full adder cells with fewer transistor numbers. Also, as the number of transistors is reduced, the Area of the proposed hybrid full adders is also reduced.

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