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Design Of Shift Register Using Current Mode Logic D Flip Flops

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Abstract: Over past few years, the surpassing advancements in Integrated system technologies is; there is a major solid growth in using micro circuitry devices. In this digital world, electronic devices like computers, mostly use registers for multi purposes. Theme of the paper is to Design a Shift Register using CML technique D-Flip Flops. This idea is used for low voltage supply and speed improvement. D flip-flop is designed using D-latches. To satisfy the speed requirements, D-latches are usually designed in current-mode logic (CML). The CML is itself a MOS differential pair. In this paper, D latches are designed using conventional method, triple-tail method, folded method and their performance is compared in terms of Power (Reference Current ISS over 500µ A) and delay. The folded D latch gives best results in terms performance and delay. This folded D latch is used for the design of d flip-flops. With the help of D Flip-Flops, the proposed Shift Register is implemented.

Index Terms— Current Mode Logic(CML); Folded, low voltage, Shift register, nanometer

INTRODUCTION

From last few decades, the attentiveness towards high data rate communications and speed performance is widened. IC's are adopted largely, accrediting semiconductor and telecommunication technologies. The microprocessor and memory chips are VLSI circuits. These electronic devices may contain CPU, ROM, RAM etc., These all are integrated on a single chip through VLSI designs. Usually the problems arose whenever the complexity of the circuit increases. The complex devices like computer depends on the speed and performance.

Registers are constructed using Flip flop. Register is a group of flip flops that are used to store various bits of data. For storing 8 bit of data in a computer, then set of 8 flip flops is used. On basis of our requirement, the input data and output data of a register is serial or parallel. Storing series of data bits by register is called 'Byte' or 'Word'. Storing 8 bits of data is called Byte, where as Word is the storage if 16 bits or 2 bytes.

The arrangement of number of flip flops in series connection is called Register. The transferring of information stored is done with in the registers in an efficient manner; these are called 'Shift Registers'. A shift Register is a sequential device that is used to store and shift the data towards output by every clock cycle. These are used as memory elements in electronic devices like computers. Various digital system operations are done by using registers.

traditional cml latch in 45 – nm cmos

For high speed and low power performances, CML is one of the worthwhile topology. The most desirable features we acquire by using CML technique is high speed switching, low supply voltages and output voltage swing. In mixed signal digital circuit applications such as optical transceivers and portable electronic devices, CML circuits seems to be very full of promise. This paper shows that, the use of CML topology is substitute to the static CMOS circuits. CML is the general term and applies to both bipolar and CMOS. With MOS transistors, it is known as MCML.CMOS rail to rail is used for low static power dissipation whereas for high frequencies CML is preferred. Due to the reduced output voltage swing, this topology can operate faster with lower power.

A latch is a device which has only two stable states. It is considered as an example of bi-stable multi vibrator. The two stable states are high-output and low-output states. The information can be retained by the latch as it has feedback path. So, the latches can also be called as memory devices. Latch can store one bit of information as long as the device is powered. Latches are used to 'latch onto' which means information and hold in place. Latches are similar to flip flops but are not synchronous devices as flip flops. Latches doesn't work on clock edges as flip flops do.

Latch design in Current Mode Logic

For the purpose of extreme speed requirements, latches are designed in current mode logic. The basic concept of

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CML is, circuit built with the MOS differential pair as main block as it tends to guard current mode and switching noise. In high power consumption devices, these parameters help in achieving fast switching modes. The problem arises with this topology is supply voltage reduction which in turn leads to the reduction of power supply. This low voltage problem controls the usage of stacked transistors in CML gated device as we will discuss further.

On using the nanometre technologies, there is the degradation in small signal parameters such as trans conductance which in turn leads to inflame analogue performance, gain and noise margins. CML latch is implemented in which transistors determining differential

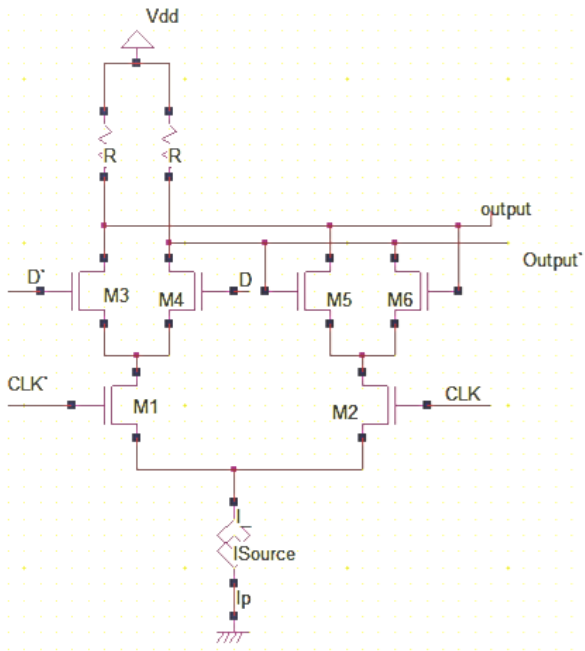

Fig. 1. Standard MOS CML D-Latch

pair's (M3-M4 or M5-M6) tail current are carried by clock pulse (M1 or M2) as shown in Fig. 1 To prove that designing

a CML D-Latch in 45-nm technology under 1-V, analysing gain of CML device must be done. To attain the full switching, the voltage gain must be greater than unity.

The gain is expressed as,

$$A_V = g_m \times [R_D]$$
$$= g_m(V_{SWING} \div 2I_{SS})$$

where V_{SWING} is output voltage swing, g_m is trans conductance of transistors of differential pair, A_v is the gain. To improve the gain, V_{SWING} should be increased. According to the CML topology implemented, data and clocking pulse is totally depending on common voltage. In this methodology, the common mode voltage of both input and output of latch should be equal to allow for further cascading. But under 1-v voltage supply, All the stacked transistors used are not biased. The drawback is that this topology does not work over the reference current 250µA. Therefore, latch could not be designed perfectly in 45 nm under low supply voltage. So, topologies are proposed to work under the required constraints.

low voltage cml latch designs in 45 – nm cmos

To deal with the unfavourable cases arose in previous topology, the methods with less stacked transistors and no extra circuitry design for steady output swing and delay is proposed. These possible topologies are considered by the power consumption parameter which is based on the biasing current and voltage supplied. But, reduction of I_{SS} surely effects the speed performance. Minimizing of voltage supply can be done by degrading the number of series gating levels. It is done by proposing triple tail cells approach.

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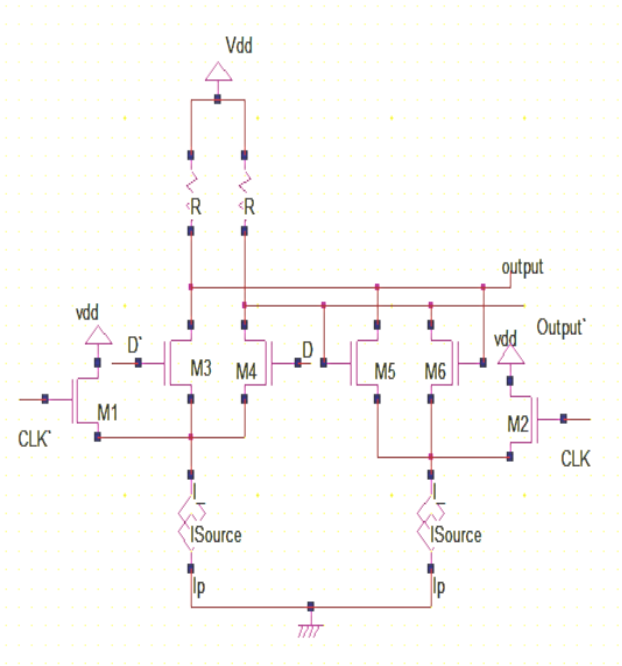

Fig. 2. Low Voltage Triple Tail D-Latch

CML latch by means of triple tail cell

In this topology, the D-latch is implemented (Fig. 2.) using two emitter coupled pairs and two current biasing sources

$I_{SS}/2$ in which one pair is driven by the differential signal and other one implements the memory element. On the basis of

clock pulse, one of the two coupled pairs is deactivated respectively by the transistors (M1, M2) possessing high emitter area than all other transistors present. The transistor M1 gets OFF and the cross coupled transistors M5, M6 holds previous logic value show that latch stays in the hold state, when CK is low. In the same way, when the CK is high, M2 gets OFF and M1 is ON and the cross coupled pair is deactivated. Thus the output value is set equal to the input value by the transistors M3, M4 and the latch is said to be in the transparent state.

The worst case scenario in logic swing is attained in the hold mode which leads to the low noise margin. This circuitry is very responsive to the common-mode voltage, voltage swing and aspect ratio of clock pulse transistors. To avoid the reduction of output swing voltage and minimizing the noise margin, aspect ratio must be greater than other devices. Increasing of aspect ratio leads to the raise of clock distribution network and emitter area is increased.

The method of using transistors with various threshold voltage levels is introduced that leads to lower the aspect factor. But, multi threshold option is not available in all CMOS technologies.

In the generic circuit shown in Fig 3., the activation of emitter coupled pair is done when it is biased. Biasing of series gate is done by the current steered by the lower level pair. Usually this requires two levels of the series gating. But a new strategy is proposed in which the gates are activated in the same level.to be more precise, series gate transistor is deactivated when its emitter is common with Q3. On applying the high base voltage, emitter couple transistors are turned off and current is steered to the ground point. The Q1-Q2 pair is

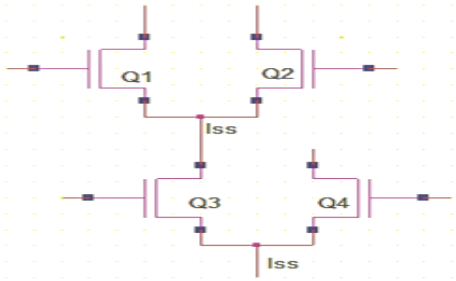

Fig. 3. Triple Tail cell

activated when the Q3 has low base voltage. This approach is known as the triple tail concept. By using this methodology, the use of the stacked emitter coupled pairs are degraded.

The problem arose using this topology i.e., when Q3 transistor is deactivated, Q1 and Q2 transistors does not

switch off completely. The impact of this case on performance and power-delay trade-off is discussed in further discussion with the help of D-latch design.

CML latch by means of Folded Current Mirror

A new topology considering low voltage supply and current mode D latch circuit is proposed which is called Folded CML D latch, Fig. 4. In this, the biasing current I_{SS} is steered by the p-type MOS transistors. The p-type MOS differential pair works depending on the current mirror values that are activated by the clock pulse. The differential pair M3, M4 is activated on turning the clock high i.e., M1 is ON, which in turn leads the latch to sample the differential signal. This is known as the

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sample phase. In the time of this phase, the input pair is activated and current I_{SS} flows across it. When clock is low i.e., M2 is ON, in presence of positive feedback in previous topology, the output pair M5-M6 holds the output signal. In the time of this phase, only output pair is activated and current I_{SS} passes through it.

The satisfactory thing of using this methodology is; it leads to save one level of stacked pair transistors which helps in minimizing the supply voltage to the circuit. The additional benefit observed by using this methodology is; common mode voltage of clock pulse is independent of the input signal.

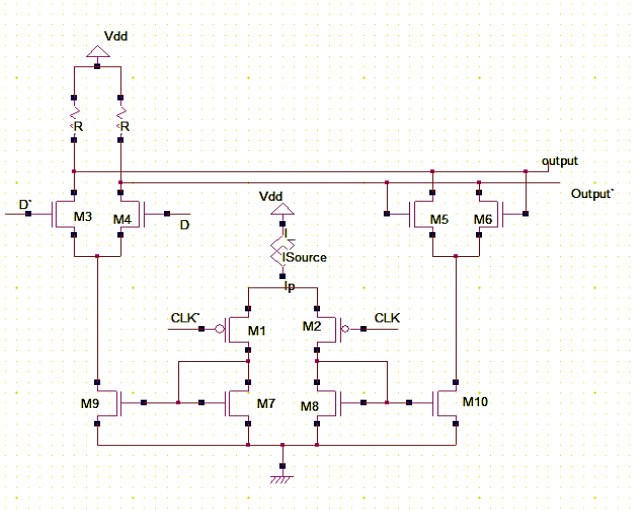

Fig. 4. Low Voltage Folded D-Latch

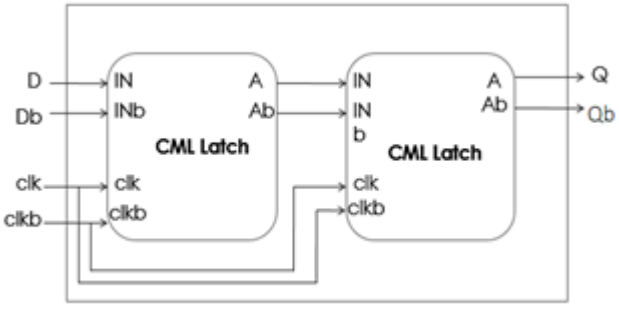

Fig. 5. Master Slave CML D- Flip Flop

design of low voltage flip flop and shift register

Low Voltage Folded Current Mirrored D flip flop

In order of merit, the considerable gain of implemented CML, triple tail and folded version D latches are helped for the design of master slave D flip flop as shown in the Fig. 5. The flip flop is designed in triple tail topology on using two complete illustrated d latch circuits. In case of designing in folded version, clock switching parameter is shared with in the used latches for designing DFFs. In this, the additional transistors are used to steer the current from other d latch.

With the help of this (Fig. 6.), tail current of differential clock pair and their aspect ratio imposed to minimize the power utilization and improves the speed performance.

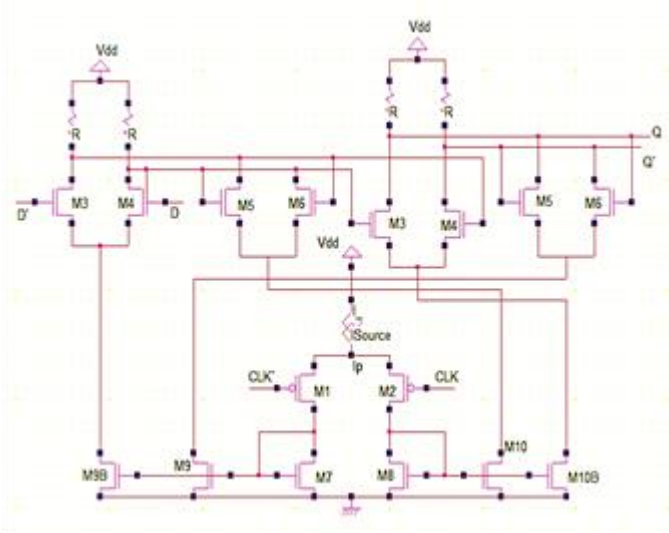

Fig. 6. Low Voltage Folded D- Flip Flop

Folded Shift Register

The 4-bit shift register is implemented using designed d flip flops. The designed flip flops are implemented with low voltage CML techniques and traditional in 45 nm technology by using cadence virtuoso GPDK models. The Shift register is designed on cascading the d flip flops (Fig.7.) and implemented in different techniques.

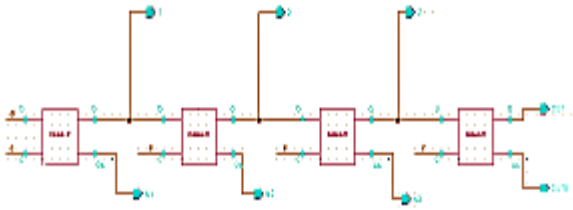

Fig. 7. Low Voltage 4-Bit Shift Register using D-Flip Flops

The specifications used in designing and parameters of the transistors used for circuitry design including I_{SS} are listed below in the TABLE 1.

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design specifications of triple tail and folded d latch.

Propagation Delay of D-latch(ns)		
	Triple tail	**Folded**
Reference current Iss	**45nm**	**45nm**
100µA	24.15	27.12
200µA	18.96	23.20
300µA	18.26	18.32
400µA	14.28	14.68
500µA	12.39	10.38

	Triple tail	**Folded**
Technology nm	45	45
V_{DD}	1V	1V
L(nm)	45	45
I_{SS}(µA)	500	500
R_D(KΩ)	2.25	2.25
Width of $M_{1,2}$(µm)	36	4.5
Width of $M_{3,4,5,6}$(µm)	4.5	4.5
Width of $M_{7,8,9,10}$(µm)	-	4.5

The above mentioned values are considered according to the gain and for required V_{SWING}. The analysis of propagation delay is done for latches, flip flops and shift registers over the range I_{SS} of 100µA to 500µA. This range of reference current is suitable for the high speed performances and low power efficient designs. The D-flip flops are cascaded in the way given in Fig. 7. The flip flops and shift register are implemented in three wa198i.e., conventional CML, MOS triple tail and MOS folded

results and comparison

The verified and proposed designs are simulated and analysed using Cadence. These designs are implemented using Cadence Virtuoso tool and mapped in 45-nm technology libraries. The circuitry design is implemented with comparison of three different topologies. The propagation delay is calculated by simulating the designed circuits of latch over different biasing current I_{SS}. Their performance analyses are presented in the TABLE Ⅰ.

TABLE I. propagation delay of triple tail and folded d-latch for i_{ss}

The comparison of propagation delay of the D-flip flops implemented in different types is tabulated in TABLE Ⅱ

propagation delay of triple tail and folded d-flip flop for i_{ss}

Propagation Delay of D-flip flop (ns)		
	Triple tail	**Folded**
Reference current Iss	**45nm**	**45nm**
100µA	48.3	54.24
200µA	37.92	46.42
300µA	36.52	36.64
400µA	28.56	29.36
500µA	24.78	20.76

The Shift register is implemented on using the Fig. 7. approach in two different topologies Triple tail and Folded. The analysis of propagation delay of these types is presented in TABLE Ⅲ

propagation delay of triple tail and folded shift register for i_{ss}

Propagation Delay of Shift Register (ns)		
	Triple tail	**Folded**
Reference current Iss	**45nm**	**45nm**
100µA	171.2	198.9
200µA	130.6	153.6
300µA	125.8	135.5
400µA	102.2	112.4
500µA	86.12	72.04

power consumption of 4-bit shift register

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From the above propagation delay of triple tail and folded shift register information, delay reduces with the variation in reference current variation from 100µA-400µA. With-in this range of applied reference current, the output is driven with less delay but produces the glitches on using the triple tail methodology. But using the triple tail logic, though the delay reduces, the logic gates degrades. Required decrease in the Folded topology is seen at 500µA than the triple tail topology with the full swing voltage. It is found that approximately 23 percent folded shift register is faster than the triple tail shift register. It is analysed, shift registers shows the high performance at high biasing currents i.e., above 400µA. from TABLE Ⅳ

TABLE II. power improvement of 4-bit shift register

Comparison	Power Improvement (Percentage)
Shift Register	
Folded vs CML	9.5
Folded vs Triple tail	20.83

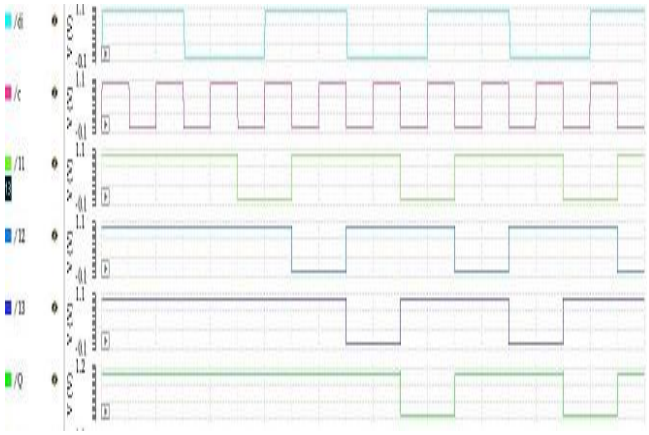

Fig. 8. Waveform of 4-Bit CML SIPO Shift Register using Folded D-Flip flops

Architecture	Total power consumption (m W)	Number of Transistors
I_{SS} = 500µA		
Shift Register		
CML Shift Register	5.45	50
Triple tail Shift Register	6.23	50
Folded Shift Register	4.932	68

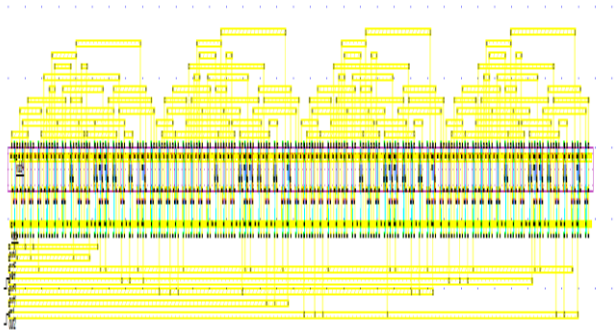

Fig. 9. Layout of 4-Bit CML Shift Register using Folded D-Flip flops in Micro Wind Software

The above shown layout (Fig. 9.) and the output waveform (Fig. 8.) is drawn from Serial-In Parallel-Out Shift Register(Fig.7.). The given data is shifted to the right for every clock pulse applied.

Conclusion

In this paper, 4bit shift register is implemented with the help of master slave D flip flops. The main objective of this implementation is to reduce consumption of power and delay. We scrutinized the issue of deigning high speed shift registers by CML topology in 45-nm with low voltage condition. The conventional CML topology is inappropriate to design with 1V voltage supply. The low voltage folded shift register is designed and analysed with triple tail and conventional topologies. With the help of simulation analysis, it is observed that the high range of trade off conditions like power consumption improved by 20.83%, speed improvement and delay product by improvement of 19.54% of Folded Shift Register is elevated against the triple tail and conventional topologies. The proposed circuitry is designed and layout

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is done in Micro wind software.

Through the work, it is observed that the proposed Shift register is efficient in terms of delay and power. In future work case, the design is used to improve the placement and routing algorithm which in turn used to optimize the device.2

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