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Design and Implementation of FIR Filter Using Hybrid Architecture

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Abstract: The paper present the design of hybrid FIR filter architecture for various filter applications. The combination of ripple carry adder, carry look-ahead adder and carry select adders is used for the designing of the core circuit components. The speed of the operation in the circuit is increased by the parallel generation of the carry by look ahead carry generation blocks and is propagated using modified carry skip adders. The radix-4 booth multiplier, which has a low-power-delay-product, is used as the multiplier in the design of the filter. The normal ripple carry adder in the booth multiplier is replaced by the modified hybrid adder for increasing the speed and performance of the multiplier unit. Thus the speed of the designed filter can be increased by the use of modified booth multiplier and lowers the propagation delay. The design and implementation is done using the cadence RTL compiler with gpdk of 45 nm technology.

Index Terms— Booth multiplier, FIR filters, Hybrid adders, PDP.

I. INTRODUCTION

Digital filters have bought a drastic change in the world. A filter is a frequency selective system. The digital filters are mainly classified into two; finite impulse response (FIR) and infinite impulse response (IIR), depending on the form of unit impulse response of the system. IIR filters mainly uses recursive structures and FIR filters uses non-recursive structures for implementation. FIR filter response depends on the present and past input values. But for IIR filter response depends on the present and past values of the execution as well as past values of the response. FIR filters has many advantages like linearity, bounded-input-bounded-output (BIBO) stability, and low sensitivity over IIR filters, which have made them suitable for many real time applications.

When converting an algorithm to hardware, addition and

multiplication is an inevitable operation. So as to improve the hardware efficiency, operations f these components has to be considered. The speed and power of these elements often dominates the overall system performance. Hence, a careful design optimization is required. For each module, multiple equivalent logic and circuit topologies exit, each of which has its own positives and negatives in terms of area, speed, or power. Reduction in area and path delays are the major challenges faced during the design of the compact circuit. Many works has been done in literature which focused on the design and implementation of filters using various adders and multipliers [1]. The system can be enhanced by replacing traditional/conventional adders with efficient adders in terms of delay, area and energy. The basic ripple carry adder (RCA) requires less area and low power compared to most other adder structures. But, its propagation delay is proportional to the bit width. The other high speed adders are carry-skip

adder, carry look-ahead adders (CLA) [2]– [7]. In [8] author improved the conventional carry skip adder (CSKA) by the using incrementation scheme. This it improved the speed of the operation, but it leads to higher power consumption. This idea has been used for the designing of the modular hybrid adder structure in [9].

The performance of a DSP system is mainly controlled by the multiplier performance. Multiplication is thus an inevitable part in digital system designing [10].hence its performance in terms of delay and power is of very much importance. Different multiplication methods are discussed in digital system designing. But high speed multiplication is achieved by the use of modified booth algorithm [12]. Modified booth algorithm has the advantage that it reduces the number of partial products by half. Three bits from the multiplicand is encoded to -2, -1, 0, 1 2 by appending a zero to the LSB bit.

S.Thakral in [11] introduced a high speed digital filter using

un-folding technique. FIR Filter has wide range of applications in different signal processing fields such as

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image processing, biomedical signal processing, high speed communication systems, noise elimination and many more.

II. IMPLEMENTATION ARCHITECTURE

The proposed filter is designed both in direct and transposed form structures. The input filter coefficients are given directly to the booth multipliers and are then added together using hybrid adders to obtain the output sequence. The delay is introduced by the use of a D flip flops.

A. Hybrid adders

The adder introduced in [9] is used for the addition of input sequence in the proposed filter. Two versions of adders are used with reduced critical path delays. The adder structure is achieved by the use of combined modified form of ripple carry adder, carry look ahead, and carry skip adder. The first form of adder consist of modified hybrid carry look ahead adder modules, final sum logic (FSL) stages and output fast carry logic (OFCL) stages. The improved version is obtained by replacing the final sum block with modified final sum block. Parallel generation of final carry by the modified look ahead carry generation blocks increased the speed of the addition. These end carries are transmitted through the modified carry skip logic performed by the OFCL blocks.

B. Booth multipliers

A traditional multiplier requires partial product proportional to the bit-width. A radix-4 Booth multiplier reduces the number of partial products to n/2. The modified booth multiplier proposed in [12] is used for the multiplication. It is a low PDP multiplier with less hardware complexity achieved through the elimination of unnecessary operations. The booth multiplier makes use of the 2's complement converter for the better performance. Also the 15-bit adder/subtractor is replaced with a 9-bit adder/subtractor. The partial products are taken out serially, which in turns increased the propagation delay of the circuit. As to reduce this propagation delay a modified version of booth multiplier is used. The partial products are generated in parallel and by performing tree addition of the partial products. The additions of partial products are carried out by the hybrid adders with reduced critical paths.

III. PROPOSED FILTER TOPOLOGY

A digital filter process the input response to give an output response. Mainly there are two types of digital filters; IIR and FIR. Any of these filters can be represented by using an impulse sequence (k). IIR filters, as the name indicates it has infinite duration. Whereas FIR filters have finite duration sequence. FIR filters are stable and have linear phase, ie. It will not introduce any face distortion, which made them commonly used filters. The output of an FIR filter is given in equation (1) below, where M represent the order or lengh, x[n] represent the input sequence and b[k]represents the coefficients of filter

$$y[n] = \sum_{K=0}^{M-1} b[k]x[n-k] \quad (1)$$

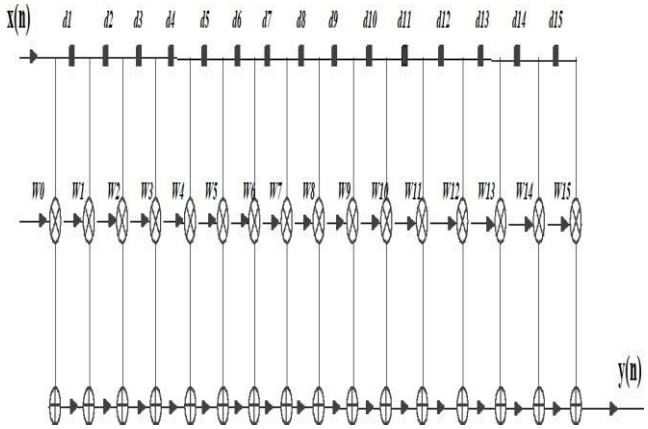

Fig. 2. Proposed direct form filter structure with modified adders and multiplier

FIR filters can be designed in mainly two structures: direct form and Transpose form. Direct form structure is the direct implementation of the equation 1 Whereas Transpose form can be constructed from direct form by exchanging the input and output and by inverting the direction of signal flow. FIR filters does not requires feedback therefore,is also known as non-recursive filters. The filter inputs are multiplied together with the filter coffecients and the output is obtained after the addition of this multiplied sequence with the delayed version of the sequence. Symmetric coeeficients are used to reduce the area, delay and the design complexities. Figure 2 and figure 3 shows the designed filter topology. It consists of 16 tap delay elements.

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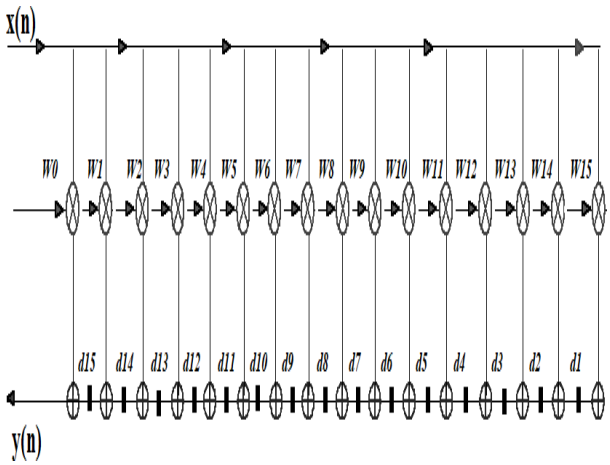

Fig. 3 Proposed transposed form filter structure with modified adders and multipliers

Direct form and transposed form filter structures are designed here. Delay elements are provided by using a D filp-flops.The filter designed using conventional multiplier and RCA consumes less area and power but more delay than the filter in which hybrid adders are used. Therefore, the first filter components are conventional booth multiplier, D flip-flop and RCA and the second filter is designed by using a modular adder with final sum logic block for the production of final output. The third filter is designed by using the modular adder with modified final sum logic and with modified booth multiplier which uses four input nand within b2c. These proposed designed has the lower delay compared to all other designs.

IV. RESULTS AND ANALYSIS

This section shows the cadence RTL simulation results of all the proposed FIR filters. The proposed designs have been developed using structural model VHDL. Cadence RTL compiler v11.10.with 45 nm technology libraries was used for the simulation. Sum of leakage power and the dynamaic power is reffered as the total power dissipated.total cell is reffered to s the designed area of the circuit. The result comparison in terms of area, delay and power is done for all the designed components. From the table it is clear that the filter which uses hybrid adders and multipliers has the less delay compared to others. These filters is used for the signal processig application for a set of frequncies.Filter coefficients were calculated in MATLAB filter designing toolbox. Both Direct form and transpose form filters were designed using these generated coefficients in Xilinx and model sim software.

TABLE I Performance analysis of designed filter

		Delay (ns)	Power (µw)	Area (sq.µm)	PDP (fJ)	ADP (sq.µm×ns)
Direct form	Filter 1	1.31	884.62	8622	1158.85	11294.82
	Filter 2	1.51	858.45	11143	1296.25	16825.93
	Filter 3	1.21	757.04	9419	916.01	11396.99
Transposed form	Filter 1	0.73	820.22	9810	598.76	7161.3
	Filter 2	0.69	667.98	13597	460.9	9381.93
	Filter 3	0.66	603.76	13368	398.48	8822.88

The different filters are: 1) FIR filter with ripple carry adders

2) FIR filter with modular adder 1 3) FIR filter with modular adder 2

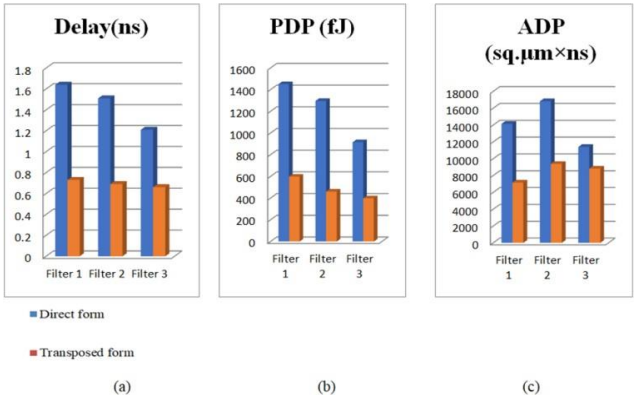

Fig. 4. Performance comparison for various filters at 45nm technology.

(a) Delay (b) PDP (c) ADP

The performance of designed filters in terms of delay, power, Area, PDP and ADP at 45nm after digital synthesis using Cadence RTL compiler is shown in the table.

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CONCLUSION

Most of the existing literature focused on the designing of filter using conventional adder and multiplier structure. Here the adder structure with least critical path is used. The advantage of the proposed architecture includes modularity, reusability, and short design time for higher width applications. The adder structures are obtained by modifying the conventional adders to hybrid form adders. The multiplier structure is obtained by modifying the conventional booth multiplier using novel b2c methods and by generating the partial products in parallel. Area, power and delay in terms of ADP and PDF for proposed filters for different combinations are studied. From results obtained it is clear that RCA with conventional multiplier is area efficient, compared others. Transposed form filter has the better performance than direct form structures as the critical path of the structure depends only on a single adder and a multiplier. It is observed that the

entire designed filter has maximum delay in direct form structure; it has the minimum delay in Transpose form structure. It is understood that the designed filter has minimum delay in the transposed form. The proposed hybrid modular adder with modified final sum logic unit is more efficient compared to all other designs. This filter is applicable for various signal processing applications such as in ECG and EEG signal denoising.

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