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Study of Dynamic Comparators on the basis of Energy Consumption

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Abstract*— This paper is aimed towards the comparison between different dynamic comparators on some parameters like noise produced, uses of area, power consumption and use of any external circuitry. In this paper mainly double tail latch comparator, cross coupled double tail latch comparator, strong arm latch (SA) and dynamic bias comparator is compared in which at the same input rms noise level and at similar area usages, the power consumption of cross coupled double tail latch comparator is reduced nearly one fourth because the energy consumption per comparison is also reduced.

Index Terms*— double tail latch comparator, strong arm latch comparator, dynamic bias, analog to digital converter (ADC), SNR, low noise, low power

I. INTRODUCTION

Comparators execute the essential action in the conversion of an analog signal to digital signal with the help of analog to digital converters, bridging the physical and digital worlds (ADC). Low noise and low power ADCs are essential in a variety of applications, including sensing devices and biomedical implants. The power efficiency of ADC improves dramatically as the technique scales down. In particular, SAR ADC benefits from its primary digital architecture and consumes very little energy.[9]-[12] Comparators serve a critical role in ADCs designed for very low power purposes. We can say that comparator accounts for 40-50 percent of overall SAR ADC energy usage [5]. Due to this many times we try to reduce power consumption of comparator. In many mixed signal circuits, dynamic comparators are a necessary component. Battery powered applications advocates the use of low power signal processing circuits, which has led to the use of dynamic comparators on a very large scale. Because of their low static power consumption, strong arm latch [7],[3] dynamic comparators and its derivatives are commonly employed. Over time, the double tail latch architecture [4] has been adapted for use in energy efficient ADCs [4,6]. In order for comparators to be used in data conversion circuits, input referred noise must be reduced enough for allowing the accurate comparisons at any input voltage level.

Outline: The remainder of this work is laid out as follows: Section II provides extensive literature survey for all the dynamic comparators which we are going to compared and we have also discussed their working. Section III introduces the performance of all the mentioned comparators and their comparison in Table 1. From the literature survey we have found these values. Section IV concludes this paper.

II. LITERATURE SURVEY

A. Double tail latch comparator [6]

Comparators play a very important role in the SAR ADCs which are targeted for very low power applications. Near about half of the energy ADC is consumed by the comparator alone. In the fig1, we can see the circuit of a commonly used double tail latch comparator. For every comparison, the output nodes intP and intN which is connected to capacitor Cp helps to discharge the capacitor completely to ground and again in next cycle Cp charges to VDD this continues. The time taken for discharging the capacitors Cp from VDD to the voltage Vlatch called as integration time and denoted by Tint. The voltage at which regenerative latch triggers is called Vlatch which is the low voltage that is enough to turn on the M11 and M12 transistors for providing the direct path for the latch. When the latch triggers, then there is no improvement in noise or conversion time if we continue to reduce the node voltages but it uses more energy to charge these nodes to VDD again. So, for reducing the power consumption, the most ideal condition is to cease the discharge of these nodes as soon as latch activates. Conventional circuits are not able to do so due to this Cp discharges completely to ground and then again charging to VDD.

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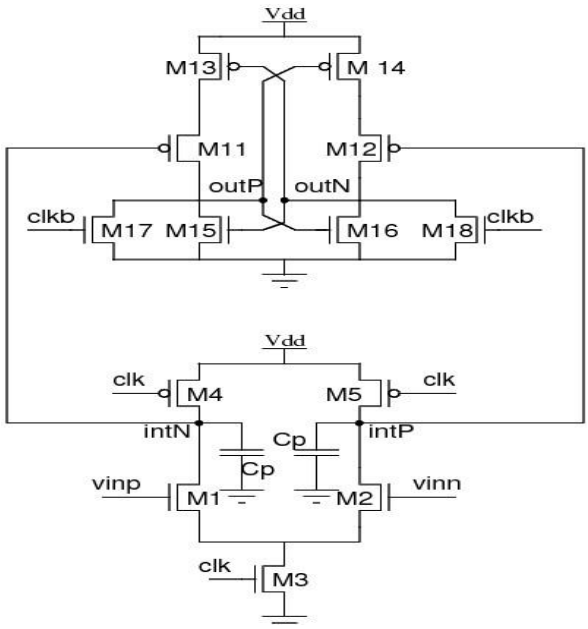

Fig.1 Circuit of double tail latch comparator [4]

The working of this type of comparator can be divided into two parts i.e., reset state when the applied clock is low and amplification state when the applied clock is high. In reset state, the transistor M4, M5 is switched on and directly connect the Vdd to the nodes intN, intP which charged them to Vdd. The transistor M3 will be switched off due to this there is no direct connection of Vdd to ground so that the current does not flow from supply to ground. The transistors M17 and M18 switched on and the output nodes of regenerative latch is directly connected to ground hence their values will be reset.

In amplification phase the transistor M4, M5 is switched off and due to this nodes intP, intN stopped charging and cutoff from Vdd. The transistor M3 will be switched on due to this M1 is directly connected to ground which provided a discharge path for the capacitor. The moment at which amplification starts, as M3 is on then the node intN started to quickly get discharged to a low voltage via M1 which is known as voltage drop. The intP node behaves in the same way. Fixed charge required for each node intN and intP is Cp*VDD and hence the consumption of energy per comparison is 2*Cp*VDD^2. Due to this, 70-80 percent of the comparator's overall energy is consumed by the preamplifier.

B. Cross coupled double tail latch comparator [1]

The cross coupled comparator design is shown below in the Fig2. In this architecture there is not change much in comparison to conventional comparator we just modified the preamplifier part and there is no change in regenerative latch part. The modification we have done in the preamplifier is that we have added a cross coupled device near the input differential pair and the transistor used in cross coupled device is denoted by M21 and M22.

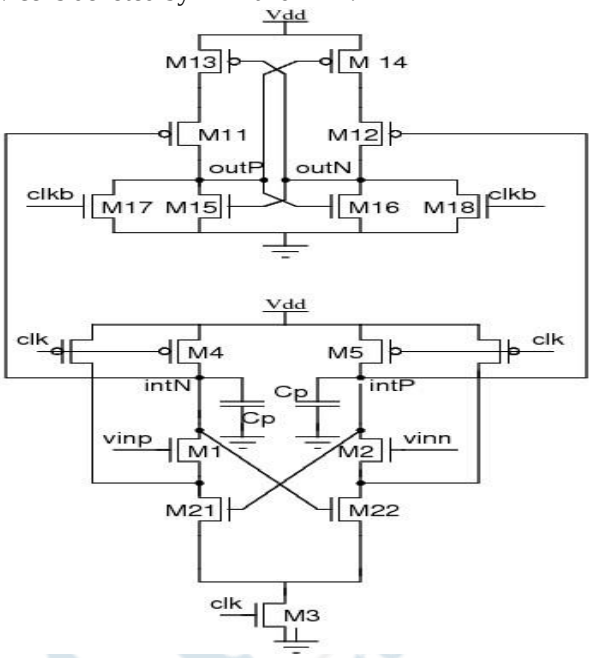

Fig.2 Cross coupled double tail latch copmparator[1]

There is not much different in the working of this circuit in reset phase but there are slight changes in the working of amplification phase due to addition of cross coupled device in preamplifier part. In reset phase, transistor M4, M5, M6 and M7 is switched on and directly connects Vdd to nodes intn, intp, N1 and P1 which charged them to Vdd. Transistor M3 will be switched off due to this there is no direct connection of Vdd to ground so that the current does not flow from supply to ground. The transistors M17 and M18 switched on and the output nodes of regenerative latch is directly connected to ground hence their values will be reset. In amplification phase, transistor M4, M5, M6 and M7 is switched off and due to this nodes intp, intn, P1 and N1 stopped charging and cutoff from Vdd. The transistor M3 will be switched on due to this M3 is directly connected to ground which provided a discharge path for the capacitor. This amplification phase on the basis of discharging the capacitor faster can be divided into two subphases named as sub pahse-1 and sub phase-2. The equivalent circuit of first and second sub phase is as shown in the below Fig.3. The moment at which amplification starts, as M3 is on and the gate of M21 is connected to Vdd from node intp, then node N1 began to rapidly discharge to a low voltage via M21 and M3 which is known as voltage drop. The node P1 works in the same manner and get discharged through M22 and M3. M21 and M22 operate as resistors when transistors M1 and M2 are turned on. The voltages at nodes N1 and P1 slowly grow as the voltage at nodes intP and intN, which is controlled by applied input voltage, declines. The Vgs of the input differential pair is changed during the entire operation which is going to reduce the trans-conductance. Rate of

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reduction of voltages at node intN and intP completely based on the input voltage (applied on differential pair) which we have applied earlier ie. vinp>vinn, due to this the rate of decrement of voltage of the node intn is greater than the node intp. When the node intn gets close to the transistor M22's threshold voltage, the rate of voltage decrement at the node intp slows down, and after a while, the node voltage at intp becomes static as M22 enters the cut off area and turns off altogether.

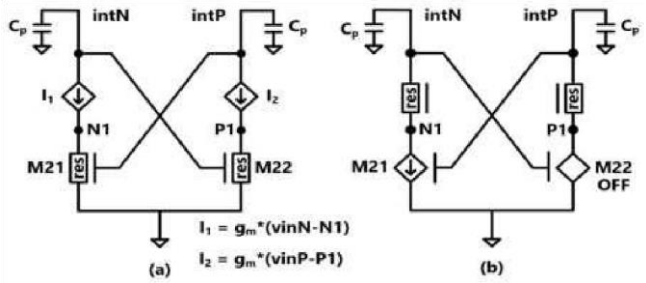

Fig.3 sub phases in amplification state[1]

When the node intp becomes static, the circuit's operation changes. Figure 3 depicts the equivalent circuit for this state. The M22 transistor is turned off in the subphase 2 of amplification state and the M1 and M21 transistors serve as a cascoded current source. When the node voltage of intp stop decreasing that is intp become static, the gate voltage of the M21 transistor is constant. Due to this the node intn discharge at a decreased rate. With the decrease in voltages of the node (intp and intn), we can see that the voltages at node P1 and N1 increase this is due to the increment in the ON resistance of the transistors M21 and M22 when the potential voltages at the gate of M21 and M22 decreases. The working behaviour of the proposed comparator make sure that the intP and intN only decreases to VD1 and VD2 which is greater than ground. This is totally opposite to the conventional comparator in which both nodes entirely discharge to the ground for every comparison [13].

C. Dynamic bias double tail latch comparator [3]

First to suggest dynamic bias or energy bias is [13] and recently this method is used in some low energy applications. So, the same concept of dynamic bias is used in this comparator so that energy consumption per bit comparison is reduced on a given SNR. The circuit of this comparator is shown in the fig.3.

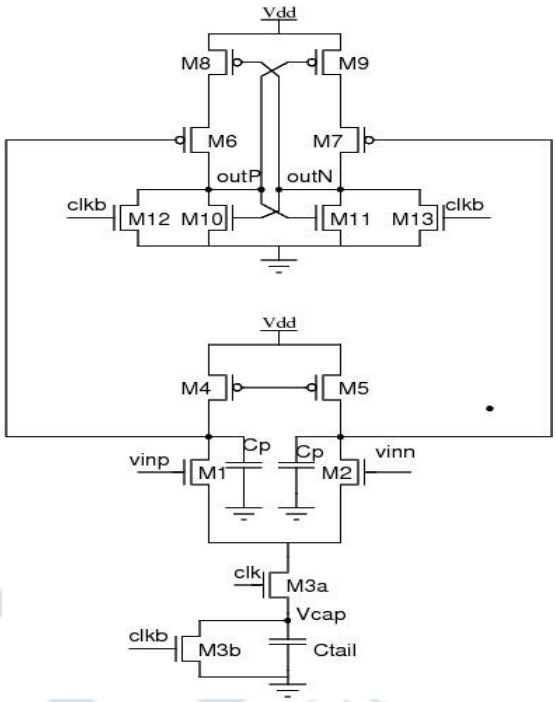

Fig.4 Dynamic bias double tail latch comparator [3]

The working of this comparator is basically defined in two parts i.e., reset state and comparison state. In the reset state when the applied clock is low then transistor M4 and M5 will be switched on and due to this the node Di- and Di+ will be directly connected to the VDD and hence charged the nodes. When clock is low then M3b is also turned on which connects the node Vcap directly to the ground and Ctail get a discharged through this path. M12 and M13 will be turned on and hence rest the latch. In the comparison phase, when applied clock is high then M3b will be turned off so that the discharge path gets disconnected and M3a will be on so that Ctail is connected to Vs. M4 and M5 will be switched off in this phase due to this Di- and Di+ nodes are started to getting discharged through capacitor Cp which in turn charges the capacitor Ctail. Due to charging the capacitor Ctail the Vcap node is also charged due to this the input differential pair is dynamically biased. The gate source voltage of M1/M2 began to decline as the Vcap increased and this will happen till it reaches the first point of quenching Vs= min (vinp-Vth1, vinn-Vth2). When we reach this point then any one of the transistors in between M1 and M2 will be turned off and its drain voltage will cease dropping but the other transistor continues to discharge till we achieved the second point of quenching Vs= max (vinpVth1, vinn- Vth2).

This is the difference from the comparator using double tail latch because in this the drain of both the transistor completely discharges to ground for every comparison. The voltage VD1/VD2 at Di+/Di- nodes the amount of charge transferred to Ctail during the comparison time determines the dynamic bias comparator's end-of-comparison state. Hence the energy consumption of dynamic bias for per comparison is 2*Cp*Vdd^2-Cp*Vdd (VD1+VD2) which is

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less than the energy consumption 2*Cp*Vdd^2 in double tail latch comparator.

D. Classic strong-arm latch

A comparator is made up of a latch and pre amplifier. By reducing the static current, dynamic comparators, which replace traditional preamplifiers with dynamic integrator-based ones, save energy. The SA latch comparator shown in fig.5 is first one in this category and one that is commonly utilized. The strong-arm latch has a high energy economy and its comparison speed is very fast because of the built-in regenerative latch and dynamic pre-amplifier, making it ideal for energy constrained applications [14].

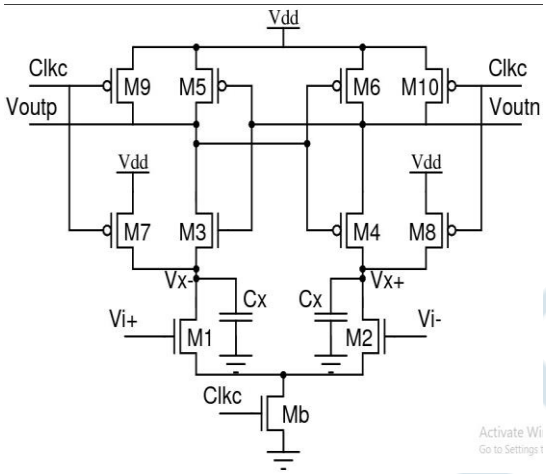

Fig.5 Classic Strong-Arm latch [3]

The above shown fig is conventional SA latch. The working can be classified into two states which are latch regeneration sate and integration state. The two states can be divided by switching on the cross coupled pair of pmos. The comparator acts as a dynamic integrator throughout the integration phase. On the integration capacitor Cx, integration of input signal takes place on a continuous basis. M3 and M4 is gradually turned on during the integration procedure. The comparator enters the latch phase when the output nodes fall below (Vdd-Vthp), where Vthp is the M5/M6 threshold voltage. During this phase, positive feedback supplies gain that grows quickly and dominates the comparator's behavior.

III. PERFORMANCE ANALYSIS

In this paper we have discussed about different dynamic comparators and the energy consumption per comparison. From the above working and energy consumption we can see that there is only dynamic bias comparator uses external capacitor and other comparators uses their internal circuitry. In cross coupled comparator there is a cross coupled device which is added to preamplifier due to this there is slight increase in the circuit's surface area. But it helps in the reduction of energy consumption per comparison. On the basis of extensive literature survey, we have drawn some data for above mentioned comparators which we have written in the table 1.

Table 1 Performance and Comparison summery in between Dynamic Comparators

	Solid state circuit, 2020 (1)		ESSCIRC, 2017 (3)		VLSI, 2019 (4)
Architecture	Cross coupled	Double tail	Dynamic bias	Double tail	Strong-arm
Process (nm)	65	65	65	65	180
Supply (V)	1	1	1.2	1.2	1.2
Noise (µVrms)	220	210	400	450	62
Energy (pJ)	0.192	0.26	0.034	0.088	4.1
Clock (MHz)	25	25	25	25	
Use of additional capacitors	No	-	Yes	-	-
Increase in Area (%)	6.7	-	38.8	-	-

As we can see from the above table that when we try to stop the complete discharging operation of capacitors then the energy consumption per comparison is reduced. When we use any external component for partial discharge of capacitor the area increased so for low area operation try to minimize the use of any external circuitry.

IV. CONCLUSION

As we all know when we try to reduce one parameter then other parameter increases so when we try to use comparator on very low noise level the energy consumption increases which is not very beneficial. So, we have to control both the parameters. As we can see from the table 1 there is comparison in between all the mentioned comparator architectures and from there we can conclude that we can use cross coupled dynamic latch comparator at low energy level for lower power consumption while using very low area. There is near about 30% reduction in the power consumption for every comparison. This type of comparator can be used for low power application and can also be used where we need both low power and less area.

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